Phase Locked Loops for High-Frequency Receivers and Transmitters–Part 3

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The first part of this series introduced phase-locked loops (PLLs), described basic architectures and principles of operation. It also included an example of where a PLL is used in communications systems. In the second part of the series, critical performance specifications, like phase noise, reference spurs, and output leakage, were examined in detail, and their effects on system performance were considered. In this, the last part of the series, we will deal with some of the main building blocks that go to make up the PLL synthesizer. We will also compare integer-N and fractional-N architectures. The series will end with a summary of VCOs currently available on the market and a listing of the Analog Devices family of synthesizers.

PLL Synthesizer Basic Building Blocks

A PLL synthesizer can be considered in terms of several basic building blocks. Already touched upon, they will now be dealt with in greater detail:

Phase-Frequency Detector (PFD)
Reference Counter (R)
Feedback Counter (N)

The Phase-Frequency Detector (PFD)

The heart of a synthesizer is the phase detector—or phase-frequency detector. This is where the reference frequency signal is compared with the signal fed back from the VCO output, and the resulting error signal is used to drive the loop filter and VCO. In a digital PLL (DPLL) the phase detector or phase-frequency detector is a logical element. The three most common implementations are :

Exclusive-or (EXOR) Gate
J-K Flip-Flop
Digital Phase-Frequency Detector

Here we will consider only the PFD, the element used in the ADF4110 and ADF4210 synthesizer families, because—unlike the EXOR gate and the J-K flip flop—its output is a function of both the frequency difference and the phase difference between the two inputs when it is in the unlocked state.

Figure 1 shows one implementation of a PFD, basically consisting of two D-type flip flops. One Q output enables a positive current source; and the other Q output enables a negative current source. Assuming that, in this design, the D-type flip flop is positive-edge triggered, the states are these (Q1, Q2):

11—both outputs high, is disabled by the AND gate (U3) back to the CLR pins on the flip flops.

00—both P1 and N1 are turned off and the output, OUT, is essentially in a high impedance state.

10—P1 is turned on, N1 is turned off, and the output is at V+.

01—P1 is turned off, N1 is turned on, and the output is at V–.

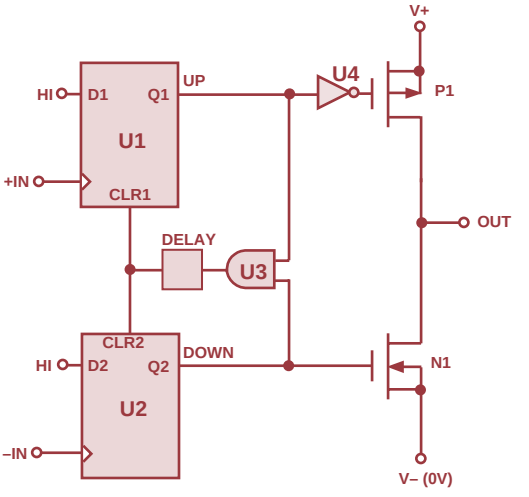

Figure 1. Typical PFD using D-type flip flops.

Consider now how the circuit behaves if the system is out of lock and the frequency at +IN is much higher than the frequency at –IN, as exemplified in Figure 2.

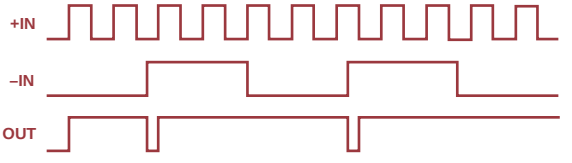

Figure 2. PFD waveforms, out of frequency and phase lock.

Since the frequency at +IN is much higher than that at –IN, the output spends most of its time in the high state. The first rising edge on +IN sends the output high and this is maintained until the first rising edge occurs on –IN. In a practical system this means that the output, and thus the input to the VCO, is driven higher, resulting in an increase in frequency at –IN. This is exactly what is desired.

If the frequency on +IN were much lower than on –IN, the opposite effect would occur. The output at OUT would spend most of its time in the low condition. This would have the effect of driving the VCO in the negative direction and again bring the frequency at –IN much closer to that at +IN, to approach the locked condition. Figure 3 shows the waveforms when the inputs are frequency-locked and close to phase-lock.

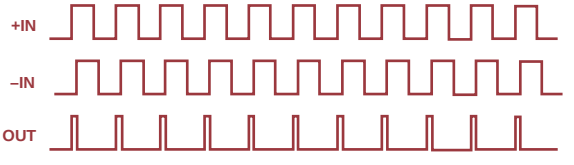

Figure 3. PFD waveforms, in frequency lock but out of phase lock.

Since +IN is leading –IN, the output is a series of positive current pulses. These pulses will tend to drive the VCO so that the –IN signal become phase-aligned with that on +IN.

When this occurs, if there were no delay element between U3 and the CLR inputs of U1 and U2, it would be possible for the output to be in high-impedance mode, producing neither positive nor negative current pulses. This would not be a good situation. The

VCO would drift until a significant phase error developed and started producing either positive or negative current pulses once again. Over a relatively long period of time, the effect of this cycling would be for the output of the charge pump to be modulated by a signal that is a subharmonic of the PFD input reference frequency. Since this could be a low frequency signal, it would not be attenuated by the loop filter and would result in very significant spurs in the VCO output spectrum, a phenomenon known as the *backlash* effect. The delay element between the output of U3 and the CLR inputs of U1 and U2 ensures that it does not happen. With the delay element, even when the +IN and –IN are perfectly phase-aligned, there will still be a current pulse generated at the charge pump output. The duration of this delay is equal to the delay inserted at the output of U3 and is known as the *anti-backlash pulse width*.

The Reference Counter

In the classical Integer-N synthesizer, the resolution of the output frequency is determined by the reference frequency applied to the phase detector. So, for example, if 200-kHz spacing is required (as in GSM phones), then the reference frequency must be 200 kHz. However, getting a stable 200-kHz frequency source is not easy. A sensible approach is to take a good crystal-based high frequency source and divide it down. For example, the desired frequency spacing could be achieved by starting with a 10-MHz frequency reference and dividing it down by 50. This approach is shown in the diagram in Figure 4.

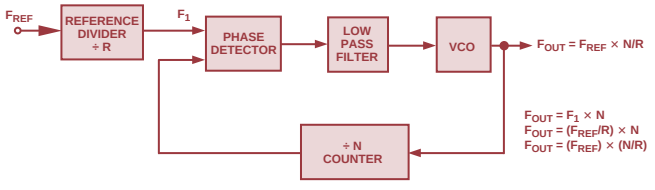

Figure 4. Using a reference counter in a PLL synthesizer.

The Feedback Counter, N

The N counter, also known as the N divider, is the programmable element that sets the relationship between the input and output frequencies in the PLL. The complexity of the N counter has grown over the years. In addition to a straightforward N counter, it has evolved to include a prescaler, which can have a dual modulus.

This structure has grown as a solution to the problems inherent in using the basic divide-by-N structure to feed back to the phase detector when very high-frequency outputs are required. For example, let's assume that a 900-MHz output is required with 10-kHz spacing. A 10-MHz reference frequency might be used, with the R-Divider set at 1000. Then, the N-value in the feedback would need to be of the order of 90,000. This would mean at least a 17-bit counter capable of dealing with an input frequency of 900 MHz.

To handle this range, it makes sense to precede the programmable counter with a fixed counter element to bring the very high input frequency down to a range at which standard CMOS will operate. This counter, called a *prescaler*, is shown in Figure 5.

However, using a standard prescaler introduces other complications. The system resolution is now degraded ($F_1 \times P$). This issue can be addressed by using a dual-modulus prescaler (Figure 6). It has the advantages of the standard prescaler but without any loss in system resolution. A dual-modulus prescaler is a counter whose

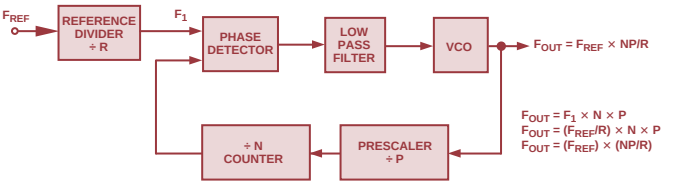

Figure 5. Basic prescaler.

division ratio can be switched from one value to another by an external control signal. By using the dual-modulus prescaler with an A and B counter one can still maintain output resolution of F_1. However, the following conditions must be met:

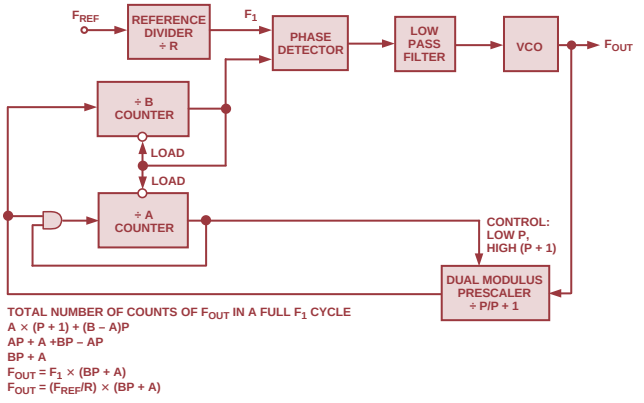

Figure 6. Dual-modulus prescaler.

1. The output signals of both counters are High if the counters have not timed out.
2. When the B counter times out, its output goes Low, and it immediately loads both counters to their preset values.
3. The value loaded to the B counter must always be greater than that loaded to the A counter.

Assume that the B counter has just timed out and both counters have been reloaded with the values A and B. Let's find the number of VCO cycles necessary to get to the same state again.

As long as the A counter has not timed out, the prescaler is dividing down by P + 1. So, both the A and B counters will count down by 1 every time the prescaler counts (P + 1) VCO cycles. This means the A counter will time out after $((P + 1) \times A)$ VCO cycles. At this point the prescaler is switched to divide-by-P. It is also possible to say that at this time the B counter still has $(B - A)$ cycles to go before it times out. How long will it take to do this: $((B - A) \times P)$. The system is now back to the initial condition where we started.

The total number of VCO cycles needed for this to happen is :

$$N = (A \times (P + 1)) + ((B - A) \times P)$$

$$= AP + A + BP - AP$$

$$= A + BP$$

When using a dual-modulus prescaler, it is important to consider the lowest and highest values of N. What we really want here is the range over which it is possible to change N in discrete integer steps. Consider the expression N = A + BP. To ensure a continuous integer spacing for N, A must be in the range 0 to (P – 1). Then, every time B is incremented there is enough resolution to fill in all the integer values between BP and $(B + 1)P$. As was already noted for the dual-modulus prescaler, B must be greater than or equal

to A for the dual modulus prescaler to work. From these we can say that the smallest division ratio possible while being able to increment in discrete integer steps is:

$$N_{MIN} = (B_{min} \times P) + A_{min}$$
$$= ((P - 1) \times P) + 0$$
$$= P^2 - P$$

The highest value of N is given by

$$N_{MAX} = (B_{max} \times P) + A_{max}$$

In this case A_{max} and B_{max} are simply determined by the size of the A and B counters.

Now for a practical example with the ADF4111.
Let's assume that the prescaler is programmed to 32/33.
A counter: 6 bits means A can be $2^6 - 1 = 63$
B counter: 13 bits means B can be $2^{13} - 1 = 8191$

$$N_{MIN} = P^2 - P = 992$$
$$N_{MAX} = (B_{max} \times P) + A_{max}$$
$$= (8191 \times 32) + 63$$
$$= 262175$$

ADF4110 Family

The building blocks discussed in the previous sections are all used in the new families of integer-N synthesizers from ADI. The ADF4110 family of synthesizers consists of single devices and the ADF4210 family consists of dual versions. The block diagram for the ADF4110 is shown below. It contains the reference counter, the dual-modulus prescaler, the N counter and the PFD blocks described above.

Fractional-N Synthesizers*

Many of the emerging wireless communication systems have a need for faster switching and lower phase noise in the local oscillator (LO). Integer N synthesizers require a reference frequency that is equal to the channel spacing. This can be quite low and thus necessitates a high N. This high N produces a phase noise that is proportionally high. The low reference frequency limits the PLL lock time. Fractional-N synthesis is a means of achieving both low phase noise and fast lock time in PLLs.

The technique was originally developed in the early 1970s. This early work was done mainly by Hewlett Packard and Racal. The technique originally went by the name of "digiphase" but it later became popularly named fractional-N.

In the standard synthesizer, it is possible to divide the RF signal by an integer only. This necessitates the use of a relatively low reference frequency (determined by the system channel spacing) and results in a high value of N in the feedback. Both of these facts have a major influence on the system settling time and the system phase noise. The low reference frequency means a long settling time, and the high value of N means larger phase noise.

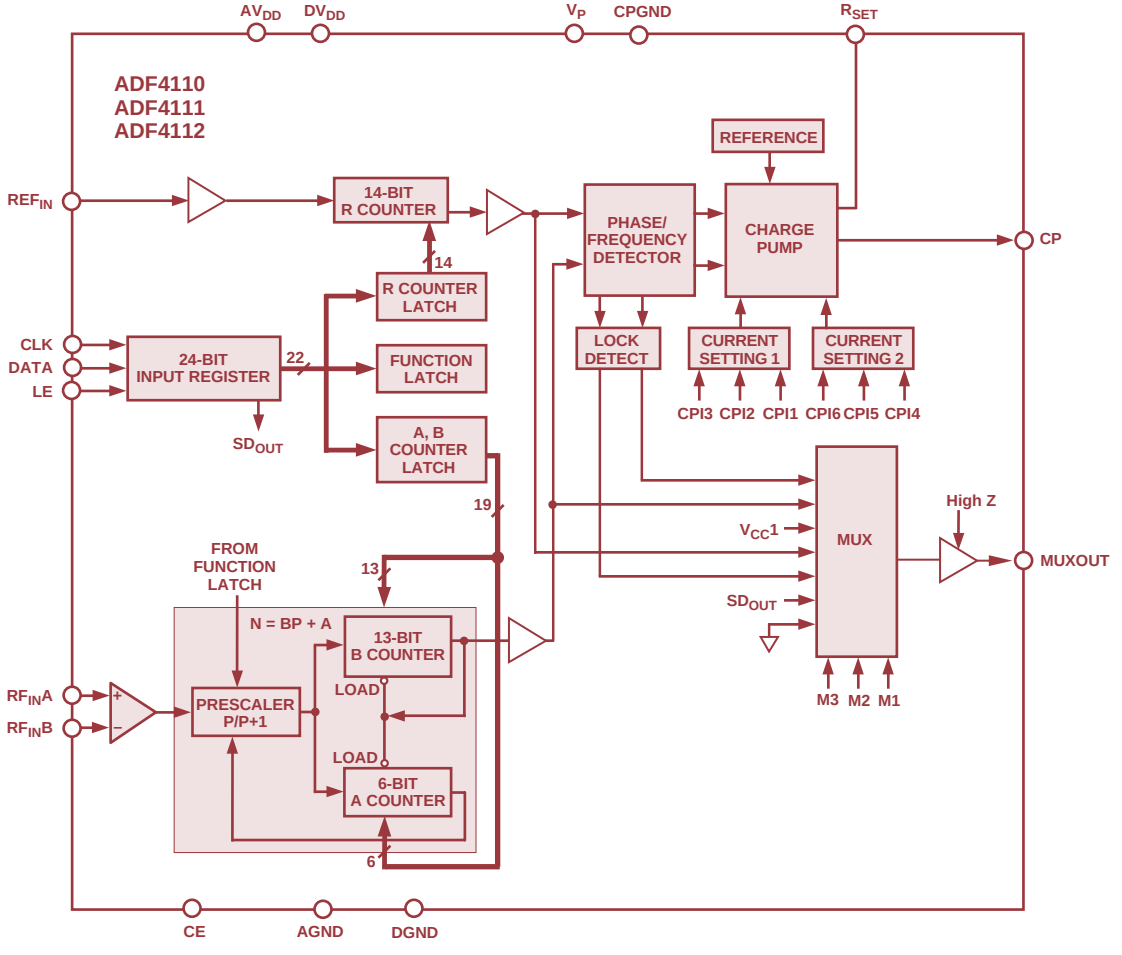

Figure 7. Block diagram for the ADF4110 family.

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If division by a fraction could occur in the feedback, it would be possible to use a higher reference frequency and still achieve the channel spacing. This lower fractional number would also mean lower phase noise.

In fact it is possible to implement division by a fraction over a long period of time by alternately dividing by two integers (divide by 2.5 can be achieved by dividing successively by 2 and 3).

So, how does one divide by X or (X + 1) (assuming that the fractional number is between these two values)? Well, the fractional part of the number can be allowed to accumulate at the reference frequency rate.

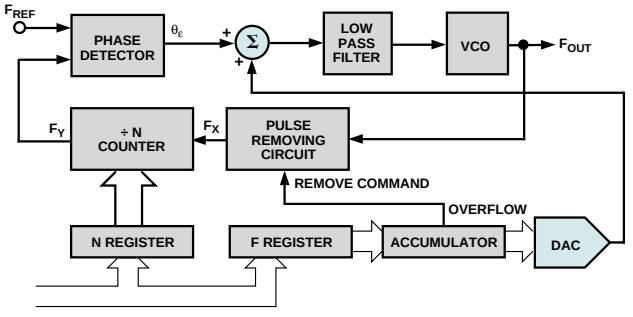

Figure 8. Fractional-N synthesizer.

Then every time the accumulator overflows, this signal can be used to change the N divide ratio. This is done in Figure 8 by removing one pulse being fed to the N counter. This effectively increases the divide ratio by one every time the accumulator overflows. Also, the bigger the number in the F register, the more often the accumulator overflows and the more often division by the larger number occurs. This is exactly what is desired from the circuit. There are some added complications however. The signal being fed to the phase detector from the divide-by-N circuit is not uniform in real time. Instead it is being modulated at a rate determined by the reference frequency and the programmed fraction. This is turn modulates the phase detector output and goes to the VCO input. The end result is a high spurious content at the output of the VCO. Major efforts are currently under way to minimize these spurs. One method uses the DAC shown in Figure 8.

Up to now, monolithic Fractional-N synthesizers have failed to live up to expectations but the eventual benefits that may be realized mean that development is continuing at a rapid pace.

Summary of VCO Manufacturers

With the explosive growth in wireless communications, the demand for products like synthesizers and VCOs has increased dramatically over the past five years. Interestingly, until now, the markets have been served by two distinct sets of manufacturers. Below is listed a selection of players in the VCO field. This list is not meant to be all-inclusive, but rather gives the reader a feel for some of the main players.

VCOs

Murata	Murata has both 3-V and 5-V devices available. The VCOs are mainly narrowband for wireless handsets and base stations. Frequencies are determined by the wireless frequency standards.
Vari-L	Vari-L addresses the same market as Murata. 3-V and 5-V devices are available.
Alps	Alps makes VCOs for wireless handsets and base stations.
Mini-Circuits	Mini-Circuits offers both narrowband and wideband VCOs.
Z-Comm	Z-Communications has both wideband and narrowband VCOs. The wideband VCOs typically have an octave tuning range (1 GHz to 2 GHz, for example) and operate from a supply voltage of up to 20 V. They offer surface-mount packaging.
Micronetics	Micronetics offers both narrowband and wideband VCOs. Their strength lies more in the wideband products where they can go from an octave range at anything up to 1200 MHz. Above these output frequencies, the range is somewhat reduced.

The Analog Devices Synthesizer Family

The following table lists current and future members of the ADF4xxx synthesizer family. It includes single and dual, and integer-N and fractional-N devices.

Acknowledgements

The ADF4xxx Family of synthesizers is designed at the Analog Devices facility in Limerick, Ireland. The product line team includes: Mike Tuthill, Leo McHugh, Bill Hunt, Mike Keaveney, Brendan Daly, Paul O'Brien, Paul Mallon, Ian Collins, Sinead O'Keefe, Liam McCann, Patrick Walsh, Cristoir O'Reilly, Paul Laven, Samuel Landete, Niall Kearney, and Mike Curtin. The group would like to acknowledge the valuable contributions of Jon Strange and Ashish Shah at Analog Devices, Kent (U.K.), and of Fred Weiss at Analog Devices Northwest Labs (Beaverton, OR).

References

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2. L.W. Couch, *Digital and Analog Communications Systems*, Macmillan Publishing Company, New York, 1990.
3. P. Vizmuller, *RF Design Guide*, Artech House, 1995.
4. R.L. Best, *Phase Locked Loops: Design, Simulation and Applications*, 3rd Edition, McGraw-Hill, 1997.

Device	Integer-N Frequency Range	Fractional-N Frequency Range	Single/ Dual	Pin Count	Second Source
ADF4110	≤550 MHz		Single	16	
ADF4111	≤1.2 GHz		Single	16	
ADF4112	≤3.0 GHz		Single	16	
ADF4113	≤3.8 GHz		Single	16	
ADF4116	≤550 MHz		Single	16	LMX2306
ADF4117	≤1.2 GHz		Single	16	LMX2316
ADF4118	≤3.0 GHz		Single	16	LMX2326
ADF4210	≤510 MHz/≤1.2 GHz		Dual	20	
ADF4211	≤510 MHz/≤2.0 GHz		Dual	20	
ADF4212	≤510 MHz/≤3.0 GHz		Dual	20	
ADF4213	≤1.0 GHz/≤2.5 GHz		Dual	20	
ADF4216	≤510 MHz/≤1.2 GHz		Dual	20	LMX2332L
ADF4217	≤510 MHz/≤2.0 GHz		Dual	20	LMX2331L
ADF4218	≤510 MHz/≤2.5 GHz		Dual	20	LMX2330L
ADF4206	≤500 MHz/≤500 MHz		Dual	16	LMX2337
ADF4207	≤1.1 GHz/≤1.1 GHz		Dual	16	LMX2335
ADF4208	≤1.1 GHz/≤2.0 GHz		Dual	20	LMX2336
ADF4150		≤550 MHz	Single	16	
ADF4151		≤1.2 GHz	Single	16	
ADF4152		≤3.0 GHz	Single	16	
ADF4156		≤550 MHz	Single	20	
ADF4157		≤1.2 GHz	Single	20	
ADF4158		≤3.0 GHz	Single	20	
ADF4250	≤550 MHz	≤1.2 GHz	Dual	20	
ADF4251	≤550 MHz	≤2.0 GHz	Dual	20	
ADF4252	≤1.0 GHz	≤3.0 GHz	Dual	20	
ADF4256		≤550 MHz/≤1.2 GHz	Dual	20	
ADF4257		≤550 MHz/≤2.0 GHz	Dual	20	
ADF4258		≤1.0 GHz/≤3.0 GHz	Dual	20	