Digital Noise Reduction Techniques for COMBO II™

National Semiconductor
Application Brief TB- 02
October 1988

INTRODUCTION

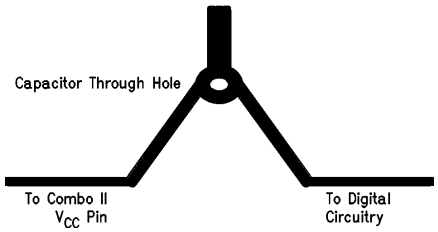
The COMBO II series of CODEC/Filter devices are highly integrated analog and digital systems on a single chip. Due to the high resolution and low noise requirements of the analog circuitry, care must be taken to minimize the effect of digital noise on analog performance. By understanding the potential problems and taking precautionary measures, the COMBO II will deliver the performance required for high quality voice transmission.

SOURCE OR NOISE

Digital noise is generated both externally and internally in a typical COMBO II application. Since this noise is at very high frequency, it may be under-sampled by the internal analog circuitry and show up as in-band noise or crosstalk.

EXTERNAL NOISE

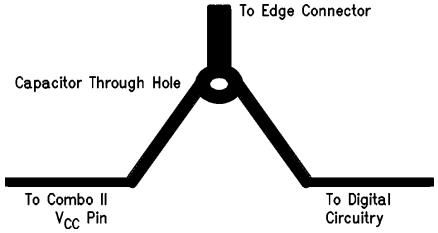
The use of high speed digital circuitry on the line card produces high frequency noise on the +5V supply which is coupled into the analog circuitry by parasitic capacitances, device non-linearities and finite power supply rejection ratios of the amplifiers. This noise is mixed with the switching frequency of the switched capacitor clocks or the encoder or decoder clocks and may produce frequency components which lie within the voice band. There are a number of ways to minimize external digital noise corruption. First and foremost, 0.1 μF ceramic capacitors must be connected from V_{CC} to GND near the COMBO II device and at each source of the digital noise. It is critical that the leads of the capacitors be kept to an absolute minimum. This means that the V_{CC} and GND board traces from the COMBO II pins and those from the source of the noise meet at the capacitor through holes or solder pads as shown in *Figure 1* below. Similar layout rules should be used for the bypass capacitors near the digital noise sources. Ideally the local bypass capacitor should supply all of the transient current required by its logic device.



TL/H/10021–1

FIGURE 1

Additionally, it can be useful to isolate the V_{CC} traces to the COMBO II devices from those of the digital circuitry. This is easily accomplished by connecting an electrolytic capacitor (>10 μF) shunted by a 0.1 μF capacitor from V_{CC} to GND near the card connector. The three V_{CC} traces and the three GND traces going to the COMBO II devices, digital circuitry and the card connector should all emanate from the through hole or solder pads of the 0.1 μF capacitors as shown in *Figure 2* below.



TL/H/10021–2

FIGURE 2

Another technique for reducing external digital noise on V_{CC} is to further decouple the V_{CC} by adding a small impedance, such as a resistor, in series with the COMBO II V_{CC} trace on the backplane side of the 0.1 μF capacitor. There are potential problems with this approach in that, if the impedance is too large, the COMBO II's supply may increase more slowly than that of the digital circuitry. This can result in COMBO II's inputs going more positive than it's V_{CC} potential, increasing the chances of triggering latch-up as described in Technical Bulletin TB-1. A second potential problem is the reduction in the supply voltage at the COMBO II pins as the resistance increases, especially under heavy loading conditions. Generally the series resistance should not exceed 10Ω.

Generally there is far less noise on the V_{SS} supply so simple bypassing with a 0.1 μF capacitor is sufficient. Decoupling V_{SS} with a series resistor is not recommended since the impedance reduces the effectiveness of the Schottky clamping diode which should be connected between V_{SS} and GND as described in TB-1. If decoupling is required, the Schottky diode must be connected on the device side of the impedance, in essence requiring a diode for each COMBO II device rather than one per board.

INTERNAL NOISE

The COMBO II CODEC/Filters are manufactured with National's high density, high speed M2CMOS process. One characteristic of this process is high digital speeds which induce large current spikes on the power supply and ground lines. In particular, the D_X0 or D_X1 digital output drivers produce V_{CC} and GND spikes when their outputs change state. These spikes may be sampled by internal analog circuitry and will produce in-band noise. For most parameters there is little effect, but *for crosstalk from transmit to receive (CTXR), the effect can be quite large*. Under worst case conditions, CTXR can be degraded to as low as 66 dB from a nominal 80 dB. In many applications this level of performance may be perfectly acceptable. In others, however, it may be marginal and methods must be considered for improving CTXR.

Three ways of reducing the effects of internally generated digital noise are: reduce the source of the noise, i.e., the

RRD-B30M115/Printed in U. S. A.

current spikes, reduce the resulting V_{CC} noise caused by the spikes and, reduce the sensitivity of the device to the V_{CC} noise.

REDUCING THE SOURCE OF THE NOISE

The D_X0 and D_X1 output buffers have the largest effect on device noise performance, and as may be expected, D_X0 and D_X1 loading also has a significant effect. The worst case 66 dB CTXR is experienced with 200 pF on the D_X pin. Therefore, National recommends that, if CTXR levels of 66 dB are not acceptable, the capacitive loading of D_X0 and D_X1 be limited to about 50 pF.

Another technique which can be used in cases where heavy capacitive loading is unavoidable, is to use a small resistor (100Ω) in series with the D_X0 and D_X1 outputs. This reduces the magnitude of the current spikes. The effect of this impedance on timing is minimal but should be taken into account.

In the future, National plans to modify the D_X0 and D_X1 output drivers to reduce the cross-over supply spikes and to control the output dV/dt to reduce the spikes due to capacitive loading.

REDUCING THE SUPPLY NOISE CAUSED BY THE SPIKES

To reduce the internally generated supply noise each COMBO II should have a 0.1 μF capacitor connected from V_{CC} to GND as close as possible to the device pins. This is essentially the same precaution as recommended for externally generated digital noise, except the focus is on minimizing the distance from the device to the 0.1 μF bypass capacitor. Ideally it should be placed physically on the pins of the COMBO II device. The use of sockets moves the bypass capacitor physically further from the device, and therefore should be avoided. If absolutely necessary, low profile sockets (i.e. Augat) may be used with minimal degradation.

As discussed above, it is critical to minimize the distance and inductance from the device to the bypass capacitor. It follows that larger packages force the capacitor further from the device in the same way that sockets do. Therefore, if CTXR is a critical parameter, it is advisable to use the TP3070V (28-Pin PLCC) or the TP3071J or TP3071N (20-Pin DIP) devices in place of the TP3070J or TP3070N (28-Pin DIP).

REDUCING THE SENSITIVITY TO SUPPLY NOISE

Beyond the precautions described above, additional steps can be taken to minimize performance degradation due to digital noise generated within the COMBO II device. The basic mechanism for the noise sensitivity is the sampling of spike noise produced by D_X0 and D_X1, referenced to BCLK, by analog switches which are referenced to MCLK. It would therefore be expected that the timing relationship between BCLK and MCLK would affect the sensitivity to spiking. This turns out to be the case and, unfortunately, the worst case relationship is when BCLK and MCLK are aligned or nearly aligned.

For best results the timing relationship between MCLK and BCLK should be such that MCLK precedes BCLK by 60 ns–80 ns. This ensures that the analog sampling is complete before digital spikes occur. Under this condition CTXR is typically greater that 80 dB while other timing can produce CTXR as low as 66 dB, expecially when MCLK and BCLK are aligned or are nearly aligned as described above.

Near the worst case condition, CTXR measurements vary dramatically with only a few nanoseconds change in the timing between BCLK and MCLK. This results in a severe production problem due to lack of correlation from one reading to the next or from one test system to the next. For correlation and repeatability reasons, the COMBO II devices are tested to a 75 dB CTXR limit with 70 ns delay from MCLK rising edge to BCLK rising edge. This guarantees that the worst case crosstalk will be 66 dB providing ''good'' supply bypass and mounting techniques are used as discussed above. In the future, National will continue to reduce the sensitivity of the COMBO II to internally generate digital noise.

SUMMARY

Several simple precautions were described which minimize the effects of digital noise on the transmission performance of the COMBO II family of CODEC/Filter devices. In most applications the performance far exceeds the requirements. In the future, improvements to the COMBO II family will further improve this performance.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408