

# Preventing Latch-Up in the COMBO II™ CODEC/Filter

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## INTRODUCTION

Despite the superior latch-up resistance already achieved, there are still conditions under which the COMBO II family of CODEC/Filter devices can be made to latch-up. These conditions are well understood and some simple precautions will prevent them from occurring.

## LATCH-UP MECHANISM

The latch-up mechanisms for CMOS circuits operating with single supplies such as logic devices are generally well understood and easily controlled. The situation is a more complicated with mixed signal analog and digital devices such as CODEC/Filters, which operate from dual supplies. *Figure 1* illustrates some of the parasitic transistors which have been found to play the most significant role in triggering latch-up in dual supply N-well CMOS devices. Once activated, the latch-up mechanism is essentially the same as for single supply devices.

## TRIGGERING LATCH-UP

The normal method of preventing latch-up in CMOS devices involves minimizing the gain of the parasitic transistors and insuring, through layout techniques, that a low value resistance is connected across the base-emitter junction of one or both of the parasitic transistors (PNP and NPN). In a single supply device,  $V_{SS}$  and GND in *Figure 1* would be connected together at frequent intervals through the device layout, insuring the  $R_{sub}$  is of sufficiently low value to shunt all injected current away from the base of Q2. In dual supply devices where  $V_{SS}$  and GND are separated by 5V, it would at first seem that any current injected by parasitic transistors such as Q1 would flow harmlessly to  $V_{SS}$ , maintaining the base-emitter junction of Q2 safely reverse biased. If however,  $V_{SS}$  were to momentarily become positive relative to GND, the base-emitter junction of Q2 would forward bias and the low value of  $R_{sub}$  would be of no benefit in shunting away base current. It would, in fact, become the path through which base current flowed to Q2. As will be explained, *this is the mechanism which triggers latch-up in COMBO II devices.*

## SUSTAINING LATCH-UP

Once Q2 turns on, its collector current provides the source of base current for Q1 and other PNP parasitic transistors not shown in the figure. Q1 then supplies additional base current to Q2, resulting in latch-up or at very minimum a high current operating state. At this point, there may be sufficient current flowing that connecting  $V_{SS}$  will not turn off Q2 but will turn on Q3, further intensifying the latch-up.

## LATCH-UP SENARIO

The fundamental trigger mechanism for latch-up in dual supply CMOS devices is  $V_{SS}$  going positive relative to GND. Several relatively common situations which can activate this mechanism will be discussed. Clearly, all of these situations deal in some way with  $V_{SS}$  "floating", at least momentarily, since  $V_{SS}$  being positive relative to GND is an essential element of the trigger mechanism.

## HOT INSERTION OF LINECARDS

In linecard applications, it is frequently necessary to insert the card into the line frame "hot", i.e., with power already on. *It is assumed that the GND pin on the card always makes contact before the supply pins or any signal pins as recommended in Application Note AN-370.*

## INPUT SIGNALS APPLIED BEFORE $V_{CC}$

AN-370 also recommends that the  $V_{CC}$  and  $V_{SS}$  pins make contact before any signal pins. But depending on the type of connector it may not be possible to have three pin lengths (for GND,  $V_{CC}$  and  $V_{SS}$ , and signal pins). In this case,  $V_{CC}$ ,  $V_{SS}$  and all signal pins may connect in any sequence depending on how the card is inserted. Another fairly common practice, which is *not* recommended, is to connect the inputs of the COMBO device directly to the backplane. Since power is on and the backplane is active, the following situation may arise:

- GND connects
- Signal inputs are connected and inputs are either at +5V or have active logic signals on them
- The  $V_{CC}$  and  $V_{SS}$  pins are not connected

In this situation transistor Q1 is turned on, since the  $V_{CC}$  pin is not connected yet and is therefore at a lower potential than the inputs. Since  $V_{CC}$  tends to have large filter capaci-

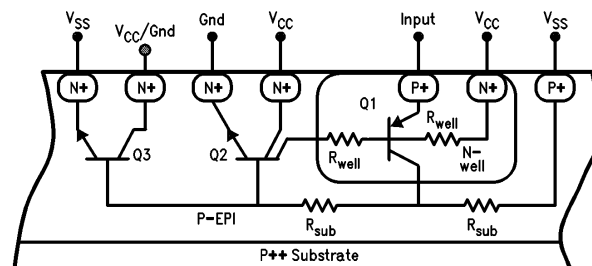


FIGURE 1

TL/H/10020±1

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tors connected to it, Q1 has an ample source of base current. Current flows from the emitter of Q1 through its collector to the  $V_{SS}$ . Since the  $V_{SS}$  pin is not yet connected,  $V_{SS}$  is pulled positive, forward biasing the base of Q2. Part of the collector current from Q2 provides additional base current for Q1, the rest of the collector current from Q2 flows to  $V_{CC}$ . If  $V_{CC}$  connects at this time, very large currents can flow because the gain of the vertical PNP Q1 is very high, and essentially none of its collector current is shunted away from the base of Q2. Even though only a portion of the Q2 collector current reaches the base of Q1, there may be a significant net gain around the Q1±Q2 loop. At this point sufficient current may be flowing such that connecting  $V_{SS}$  will not stop the latch-up and Q3 will turn on with similar results.

#### EXTERNAL CIRCUITS CONNECT FROM $V_{CC}$ TO $V_{SS}$

If the inputs to the COMBO device are buffered from the backplane by logic devices operating from the same +5V supply, the inputs cannot rise above  $V_{CC}$ , turning on Q1 and pulling  $V_{SS}$  positive. In some cases, however, external circuits such as operational amplifiers may provide a direct current path from  $V_{CC}$  to  $V_{SS}$ . In this case, the following situation may arise:

- GND connects
- The  $V_{CC}$  pin connects

Since  $V_{SS}$  is still floating, the external circuit may actually pull  $V_{SS}$  positive, turning on Q2. This situation is not as likely to cause latch-up unless the external circuit provides fairly large currents to  $V_{SS}$ , but it is something to watch out for none-the-less.

#### POWER SUPPLY SEQUENCING

Normally, power supply sequencing is not an issue. One special case where it is of concern is when separate supplies are used for digital circuitry on the linecard and the COMBO device. In this case, if the logic +5V supply is turned on before the COMBO +5V supply and  $V_{SS}$ , the situation may be essentially the same as described in **Input Signals Applied before  $V_{CC}$**  above. Another situation which can produce similar results arises when the same +5V supply is used but very heavy filtering is used on the

COMBO supply. This can cause the COMBO's  $V_{CC}$  voltage to rise slower than its input voltage with similar consequences.

#### PREVENTING LATCH-UP

There are a number of very simple precautions which if followed will insure that COMBO II will not latch-up.

The minimum solution is:

- Insure that the GND pin on the circuit board makes contact before the supply or signal pins.
- Connect a Schottky diode from  $V_{SS}$  to GND. We recommend a 1N5817 which provides excellent protection at low cost. No series impedance should isolate the Schottky diode from the device's  $V_{SS}$  pin.

The best solution is to follow the advice of Application Note AN-370. This means that in addition to the items above:

- Connect a Schottky diode (1N5817) from  $V_{CC}$  to GND.
- The COMBO inputs and outputs should be buffered from the backplane.

While the precautions above provide excellent protection at low cost, there are of course alternative ways to achieve the same goal. Two such approaches, either one of which will work are:

A Apply  $V_{SS}$  and then  $V_{CC}$  BEFORE any inputs, or . . .

B Use 1 k $\Omega$  series resistors to limit the current into device inputs that go directly to the backplane or to sources which can be active before  $V_{CC}$  is applied.

#### SUMMARY

The latch-up trigger mechanism in COMBO II has been explained and several simple, low cost precautions presented to insure safe and reliable operation of the device under real operational conditions. We at National will continue to work