National Semiconductor

Application Note OA-16

Wideband AGC Amplifier as a Differential Amplifier

January 1993

The CLC520 is a very flexible DC-coupled Automatic Gain Control amplifier (AGC). Unique features include two closely-matched differential inputs, a wideband gain-control channel (100MHz), and a ground referenced DC-coupled output signal driven from a low output impedance amplifier. Figure 1 illustrates the internal block diagram and pin assignments of the CLC520.

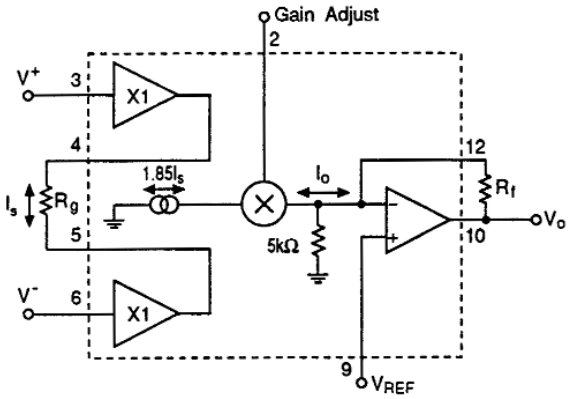


Figure 1: CLC520 internal block diagram

As shown in Figure 1, two unity-gain closed-loop input buffers on pins 3 and 6 are used to force the two input voltages to appear across the external resistor, R_g. The differential voltage across R_g generates a signal current which is amplified by a factor of 1.85 and fed into a two quadrant multiplier stage. The gain-adjustment voltage on pin 2 determines how much of this signal current makes it through the multiplier stage, with the remainder of the signal current being shunted to ground. The multiplier's output current then flows through the transimpedance amplifier formed by the external feedback resistor, R_f, and the internal amplifier. If the non-inverting input of this output amplifier, V_{ref}, is tied to ground then a ground-referenced DC-coupled replica of the differential voltage across R_g appears at the output of the op amp. The values of R_f and R_g, along with the gain-adjust voltage, determine the gain. Refer to the CLC520 data sheet for a more complete operational and performance discussion.

In order to implement a fixed-gain differential amplifier, the CLC520 will rely on R's very well-matched input buffers and it's differential-to-single-ended voltage conversion. For the purposes of this discussion, the gain-control input will be held at a fixed level to yield the maximum gain given by $1.85*R_f/R_g$. Thus, the differential signal gain depends only on the ratio of two external resistors and the internal current-mirror gain. Both R_f and R_g can be adjusted to yield a wide range of differential gains. As an example, the circuit of Figure 2 is used to demonstrate the performance of the CLC520 in a fixed-gain differential amplifier configuration.

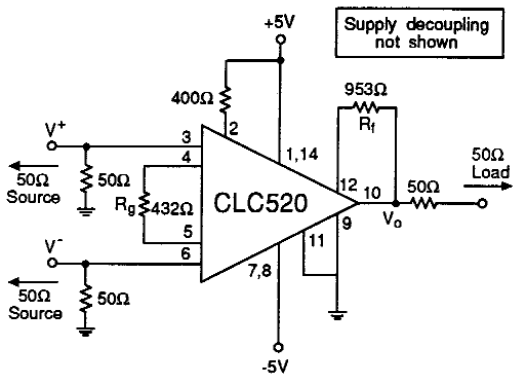


Figure 2: CLC520 Fixed-gain differential amplifier configuration

To demonstrate this application, the CLC520 is set up for a gain of 4.08V/V. The 50Ω impedance-matching resistor at the output effectively halves the differential gain to 2.04V/V (6.2dB) at the 50Ω load. Figure 3 shows the single-ended gain and phase response for both inputs on a linear frequency scale through 200MHz. Note the 180° phase offset for the inverting-signal gain, indicating signal inversion. The slightly quicker roll-off of the inverting-gain response is consistent from part to part. This broadband performance is maintained as the part is operated at higher gain settings. It is the close, broadband, gain match of the inputs that allows the CLC520 to provide this wideband differential amplifier with very good common-mode signal rejection.

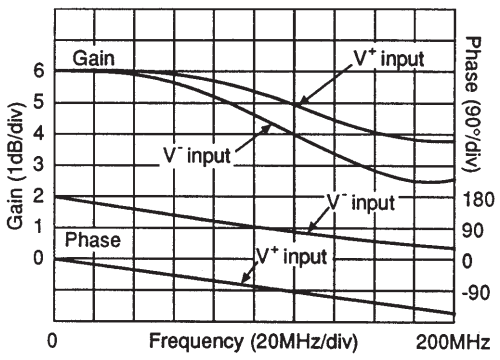


Figure 3: Single-ended gain and phase

One measure of a good differential amplifier is its ability to reject common-mode signals. The common approach in describing this rejection is as a Common Mode Rejection Ratio (CMRR). The definition of CMRR is structured to allow the common-mode input signal to be placed in series with one of the differential inputs, (divided by CMRR), as an equivalent error term. With the following definition of CMRR, an equivalent input error term is placed at one of the inputs as shown in Figure 4.

Ad: **Diff gain**
Ac: **Common-mode gain**

$$\text{CMRR} \equiv \frac{Ad}{Ac}$$

$$\text{CMRR} = 20\log(Ad) - 20\log(Ac) \qquad \textbf{Eq. 1}$$

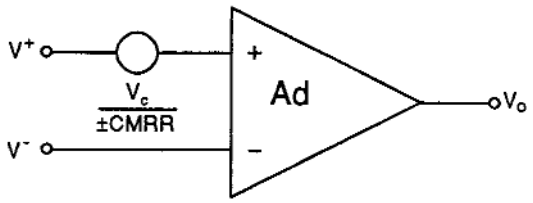


Figure 4: Input-referred common-mode error model

V^+, V^-: pure differential signals
Vc: common mode signal element

$$V_o = Ad(V^+ - V^-) \pm \frac{V_c}{CMRR} Ad$$

$$= Ad(V^+ - V^-) \pm \frac{V_c}{Ad / Ac} Ad$$

$$= Ad(V^+ - V^-) \pm VcAc$$

This definition of CMRR essentially input refers an output signal due to a common-mode input signal which effectively holds the common-mode gain constant as the differential gain is changed. In computing the actual input-to-output signal gain due to a common-mode input voltage, simply use Ac. Note, with Ac << 1, the logarithmic form of CMRR yields a large positive value. However, in computing the output common-mode signal, as shown in Figure 4, a linear (V/V) gain must be used and the error must be considered bipolar.

To measure the CMRR as defined in Figure 4, a measure of the pure differential gain must first be made. This measurement can be accomplished with the circuit of Figure 5. This circuit uses a transformer with a center tapped secondary to generate a pure differential input signal. The center tap also provides a DC path to ground supplying a DC-bias current to each of the inputs. It is necessary, in all cases, to carefully consider the source of these DC-bias currents. The transformer's frequency response was normalized prior to the gain and phase response measurement. Although using this transformer effectively AC couples the differential gain, it is important to recognize that the CLC520 is a truly DC-coupled device.

The measured gain and phase for the circuit of Figure 5 are shown in Figure 6. In order to maintain compatibility with the common-mode gain measurement, this figure is represented with a logarithmic frequency sweep from 100kHz to 100MHZ. This circuit offers an exceptional gain-flatness with only 0.5dB roll-off to 100MHZ.

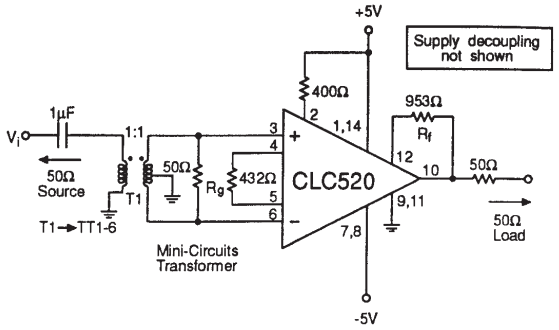


Figure 5: Differential gain test circuit

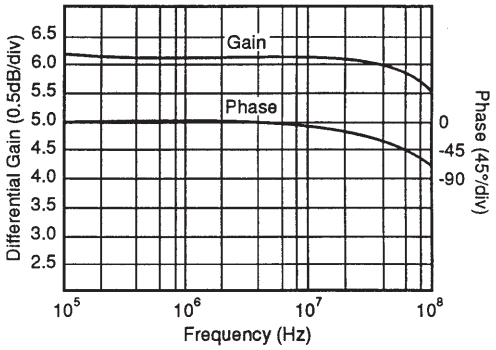


Figure 6: Differential gain and phase

The common-mode gain is measured by replacing each of the 50Ω input resistors of Figure 2 with 100Ω while connecting the two inputs together. Tying the inputs together forces the input signals to be exactly the same while the resistor replacement retains the 50Ω input impedance match. In an actual application, connecting the two inputs together is impractical. In most cases the common-mode gain is not set by the amplifier, but by the mismatch of signal attenuations arising from each signal-source's impedance into the single-ended input impedance of each of the differential amplifier's inputs. A careful attention to the signal-source impedance match is necessary in order for the CMRR performance to be dominated by the amplifier and not by the deleterious effects of signal-source impedance mismatches. The common-mode gain measurement made here sidesteps those issues by simply tying the two inputs together. Figure 7 shows the CMRR using the measured differential gain, the measured common-mode gain and the logarithmic form of CMRR (Eq.1).

The upper limit of CMRR at low-frequencies (below 100kHz) is approximately 70dB. This limit is set by the differential-to-single-ended conversion that takes place

internal to the CLC520 . At higher frequencies, the divergence in single-ended gains results in a 40dB roll-off of CMRR at 10MHz (shown in Figure 3). The CLC520's two high-impedance inputs with its internal wideband differential-to-single ended conversion combine to form a very wide-band, high CMRR, differential amplifier.

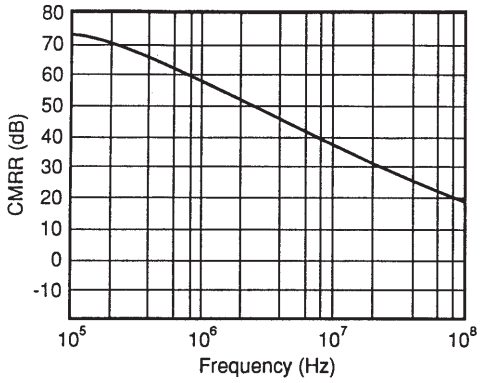


Figure 7: Common-mode rejection ratio of the circuit in Figure 2

Application Hints:

I. Improving CMRR

Several elements combine to set the frequency response of the CLC520. On the input side, parasitic capacitance to ground on either of the buffer outputs (pins 4 & 5) can cause high-frequency peaking. It is essential to keep the PC trace capacitance small and balanced when connecting R_g. For the tests shown here, R_g was soldered directly across the pins of the DIP while those pins were lifted from the board. On the output side, R_f will determine the frequency response of the output amplifier. Since this amplifier uses the current-feedback topology, R_f is the dominant element determining R_s frequency response. Increasing the value of R_f can be used to roll-off any peaking caused by parasitic capacitance on the output of the input buffers. However, it is preferable (from a noise standpoint)to minimize this parasitic on pins 4 & 5 and use lower values of R_f (and therefore lower values of R_g for any particular gain). The CLC520 is designed for use with a 1kW feedback resistor. Decreasing this value will cause the frequency response to peak, while increasing it will roll the response off. Most designs should start by first selecting a value for R_f and then determine the required R_g using the design equations found in the CLC520 data sheet. An additional constraint on lower values of R_g for good linear operation is that the maximum current supplied by the buffers through R_g should be kept within ±1.35mA. This will set a maximum differential input voltage based on this current limit and the value of R_g.

Once the parasitic capacitance to ground on pins 4 & 5 has been minimized, a frequency response similar to that shown in Figure 3 can be achieved for each of the two inputs separately. It is possible to take advantage of a parasitic gain imbalance in order to bring the inverting gain, at higher frequencies, into a closer match with the non-inverting gain. A closer gain match over a wider frequency range will improve the CMRR at high frequencies.

Although the equivalent circuit of Figure 1 shows an output that depends only on the current through R_g, any additional current driven in to or out of the buffers will also generate an output signal. Therefore, by adding an AG coupled path to ground on the output of the inverting buffer, its response can be matched to that of the non-inverting buffer. The circuit of Figure 8 shows the original test circuit with the addition of this frequency-response matching network (R_T and C_T).

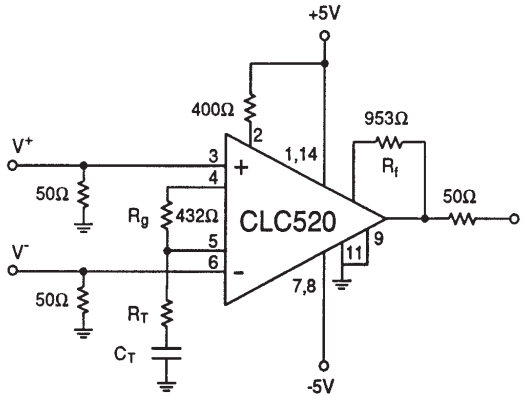


Figure 8: Differential amplifier with inverting response compensation

The single-ended frequency responses shown in Figure 3 show a lower bandwidth for the inverting gain path vs. the non-inverting. This bandwidth mismatch is consistent from part to part and is set by the internal gain path. The buffer bandwidths are considerably higher and do not play a role determining this response. The following analysis will show how to select the appropriate values for R_T and C_T such that the frequency response of the inverting gain path can be matched to that of the non-inverting gain path.

ω^+: Non-inverting response pole
ω^-: Inverting response pole

Non-inverting frequency response:

$$A^+ = Ad\left(\frac{\omega^+}{s+\omega^+}\right)$$

Inverting frequency

$$A^- = Ad\left(\frac{\omega^-}{s+\omega^-}\right)$$

Assuming $\omega^- < \omega^+$

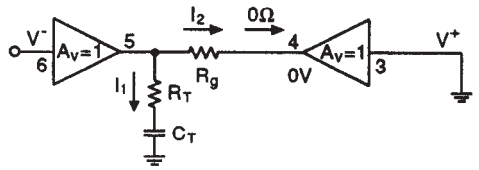
Compensate A^- to achieve the following

$$A^+ = Ad\left(\frac{\omega+}{s+\omega+}\right)$$

$$= Ad\left(\frac{\omega^-}{s+\omega^-}\right)\left(\frac{s+\omega^-}{s+\omega+}\right)\left(\frac{\omega+}{\omega^-}\right)$$

$$= Ad\left(\frac{\omega+}{s+\omega+}\right)$$

The single-ended gain response of either input may be analyzed by grounding one input in order to determine the current generated at the output of the active buffer channel. Adding the R_T-C_T series combination will then provide a means of canceling the internal inverting-path pole with a zero, and replacing it with a pole that matches that seen by the single-ended non-inverting gain path. Note, adding this network will not impact the non-inverting response as long as it is assumed the buffers have zero output-impedance. The following analysis provides a method for computing the required values of R_T and C_T given R_g and the initial single-ended frequency response of each input as shown in Figure 3. Note: the input-to-output gain from the current produced in the compensation path is 1/2 that of the gain of the current produced through R_g.



The output voltage due to an inverting input voltage is:

$$V_o = -\left[\left(1.85(I_2)R_f + \frac{1}{2}(1.85)I_1R_f\right)\right]\left(\frac{\omega^-}{s+\omega^-}\right)$$

$$I_1 = \left(\frac{V^-}{R_T + \frac{1}{sC_T}}\right) \text{ and } I_2 = \frac{V^-}{R_g};\quad \omega^- \equiv \text{single-pole response}$$

Solving this for the gain to the output:

$$\frac{V_o}{V^-} = -1.85\frac{R_f}{R_g}\left(1+\frac{\frac{1}{2}R_g}{R_T}\right)\left(\frac{s+\frac{1}{\left(R_T+\frac{R_g}{2}\right)C_T}}{s+\frac{1}{R_TC_T}}\right)\left(\frac{\omega^-}{s+\omega^-}\right)$$

The non-inverting path has a gain of:

$$\frac{V_o}{V^+} = 1.85\frac{R_f}{R_g}\left(\frac{\omega^+}{s+\omega^+}\right),\ \omega^+ \equiv \text{single-pole response}$$

Equating these two gains requires a cancelling of the ω^- pole with the zero developed by the R_TC_T network while placing the R_TC_T pole at ω^+.

Solving for R_T and C_T

$$R_T = \left(\frac{\frac{1}{2}R_g}{\frac{\omega^+}{\omega^-}-1}\right),\quad C_T = \left(\frac{1}{R_T\omega^+}\right)$$

Estimating ω^+ and ω^- from the -1dB roll-off frequencies of figure 3 and using

$\omega_{-3dB} = 1.97\ \omega_{-1dB}$ for a 1-pole response roll-off

$\omega^- = 2\pi(176\text{MHz})$

$\omega^+ = 2\pi(240\text{MHz})$

R_T and C_T therefore,

$$R_T = \left(\frac{216}{\frac{240}{176}-1}\right) = 595\,\Omega$$

$$C_T = \frac{1}{(595\Omega)2\pi(240\text{MHz})} = 1.12\,\text{pF}$$

Figures 9 &10 show the resulting single-ended frequency responses and the CMRR achieved through this compensation. Comparing Figure 9 to Figure 3 shows a much closer match over frequency. A significant improvement in the high-frequency CMRR has been achieved with this simple approach. C_T should be tuned for best CMRR at these higher frequencies. Note: when using different values of R_f and R_g, a remeasurement of the single-ended gains is required in order to provide the single-ended gain poles necessary for this compensation analysis.

II. Setting the Differential Gain

To use the CLC520 at a fixed gain, it is best (from a temperature stability standpoint) to operate at its maximum gain, determined by R_f and R_g. The adjustable portion of the CLC520's gain is set by a two-transistor internal differential stage which compares the voltage seen on pin 2 to an internal reference voltage developed as a resistor divider from the positive supply to ground. With approximately 750W internally to ground on pin 2, the 400Ω external resistor shown on the circuits above will develop approximately 3.3 volts at pin 2, insuring the internal gain stage is fully switched to maximum gain.

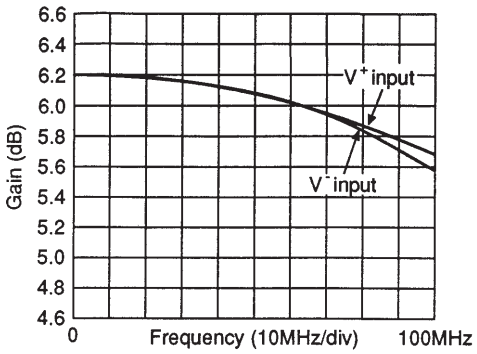


Figure 9: Single-ended gains with inverting path compensation

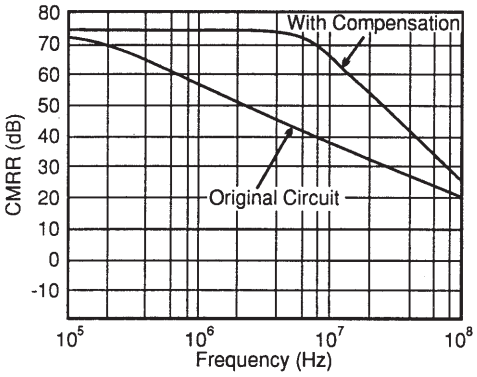


Figure 10: Improved CMRR with better response-match over frequency

Note that the signal gain is also dependent on an internal current-mirror gain from the current developed in R_g to the multiplier stage. This nominal 1.85 factor will show some part-to-part tolerance and a slight temperature dependence. A ±3% part-to-part tolerance in this current gain along with a +80ppm/°C temperature drift over 0°-70°C may by used in the design of the CLC520 circuits.

III. Using the Gain Adjust Pin

The fixed-gain differential amplifiers shown above can also be disabled with an open-collector pull-down device on pin 2. Once pin 2 is pulled below 0.4 volts, the gain will be attenuated by greater than 60dB. Again, refer to the CLC520 data sheet for a full discussion of signal attenuation vs. gain-adjust voltage. Although the forward path can be shut down in this fashion, the output pin remains a low-impedance driver: it will not be tri-stated. However, when driving several of these differential stages into an n:l MUX, shutting down the CLC520's gain will significantly improve the overall signal isolation at the MUX output.

An adjustable-gain differential amplifier can also be implemented with the CLC520.As discussed in the data sheet, the CLC520's gain adjustment is intended for operation inside an AGC loop. The gain-adjust accuracy and temperature stability of the CLC520 does not support open loop operation. A companion part, the CLC522, should be used if absolute gain accuracy and gain temperature stability is desired in an open loop (no feed-back to the gain adjust pin), adjustable-gain differential-amplifier application.

IV. Input Noise

The equivalent input noise of the CLC520 is set largely by the value of R_g. As shown in the data sheet, a model for the input noise voltage due to R_g is simply R_g*I 8pA/√Hz For any given gain setting, scaling down the values of R_f and R_g will reduce this input noise. Since Rf controls the output-amplifier stability, it cannot be made too small. For a fixed R_f, decreasing R_g will increase the signal gain. Since the input noise decreases at the same rate as the gain increases, the output noise remains nearly constant as R_g is decreased.

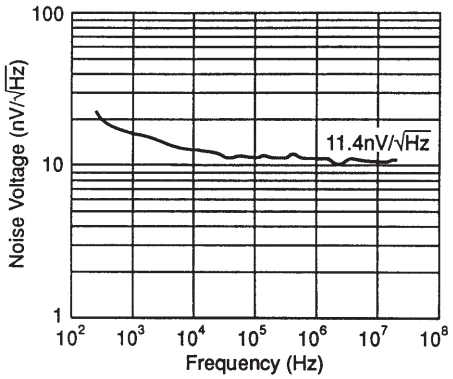


Figure 11: Input noise voltage

Figure 11 shows the measured input-referred spot noise voltage for the differential amplifier circuit of Figure 5.

Application Suggestion:
Wideband Differential Coax Line Receiver

It is often necessary to transfer high-speed signals from point to point via a matched-impedance coaxial line. Figure 12 illustrates one receiver implementation using the CLC520 at a fixed gain. Since both buffers have high-impedance inputs, a simple termination across the center conductor and properly terminate the cable allowing the differential signal to be picked-off and amplified by the CLC520. This circuit ties the coax shield into the local ground through a high-frequency blocking ferrite bead. This will help prevent coupling of high-frequency common-mode noise from the coaxial line onto the local

ground, while at the same time setting the DC voltage and current operating point for the CLC520 inputs. This will also act to break high-frequency ground loops between different pieces of equipment.

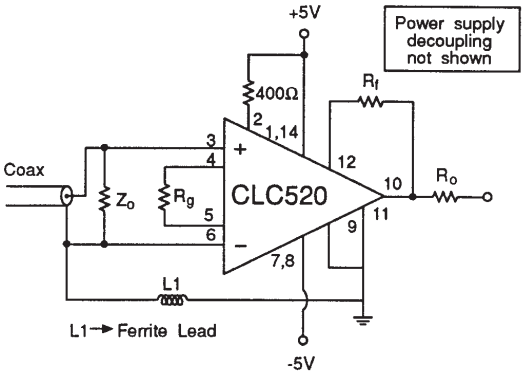


Figure 12: Differential coax line receiver

Application Suggestion:
Video Loop-Through Amplifier

The loop-through connection is one alternative to the impedance-matching approach of high-speed signals. For this approach, a high-input-impedance differential amplifier is simply placed across the center conductor and shield with minimal loading and no characteristic impedance-matching. Good high-frequency common-mode rejection and good wideband differential amplification are essential for this application. The final destination of this daisy-chained connection terminates the cable in it's characteristic impedance.

An implementation of this loop-through connection using the CLC520 is shown in Figure 13. This circuit is a replication the circuit of Figure 2 with some additional input resistors and a shutdown control gate.

The 20Ω resistors to ground will insure a DC-bias path for the input-stage bias currents. If it is absolutely certain that a DC path through both the center conductor and the shield will be maintained, the 20kΩ resistors can be eliminated with an overall improvement of VSWR. With only the 20kΩ termination, the CLC520's input offset-current drift will generate a nominal input offset-voltage drift of 100mV/°C. It is desirable considering common-mode rejection and offset-current drift, to keep these input termination resistors as large as possible. Ideally, the termination resistors should be eliminated if the bias current can be supplied by the cable. Remember, any mis-match in the single-ended attenuations from the center conductor's and shields source impedances into the CLC520's input impedances will degrade the CMRR.

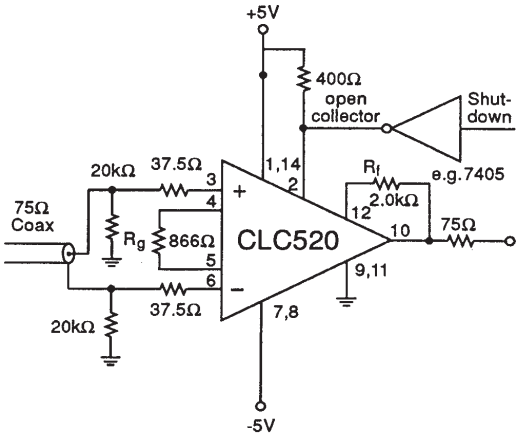


Figure 13: Video loop-through connection using a wideband differential amplifier

The two series 37.5Ω resistors into pins 3 and 6 act to isolate the inputs from the cable reactance helping to maintain high-frequency input stability. These resistors, included with the parasitic input-capacitance to ground, will also form a matched-impedance termination for the cable at very high frequencies (>500MHz): well beyond the signal frequencies of interest. The full signal level would be available to downstream stages using this wide-band differential amplifier as a loop-through connection.

Application Suggestion:
A Very Wideband Pulse-Differencing Amplifier

With the addition of several frequency-response trims, the basic circuit Figure 2 can be used to implement a very wideband pulse-differencing amplifier. Targeting a gain of +1V/V into a matched 50Ω load, bandwidths in excess of 300MHz are achievable. Figure 9 shows a typical single-sided pulse response. The input rise time for this test is approximately 800ps. With a 1.15ns output rise time and a 08ns input rise time, the amplifiers actual rise time is approximately 0.8ns for this 0.9Vstep at the load. Very similar and well-matched results can be achieved for both the inverting and non-inverting inputs.

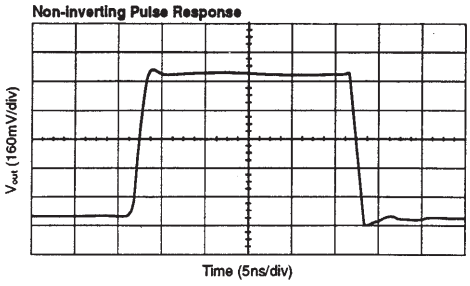


Figure 14: Very wideband single input pulse response

Application Suggestion:

Alternative Wideband Differential Amplifiers

Although the classical single op amp differential amplifier has found wide usage, several intrinsic problems limit it's performance. Both signal inputs are looking into relatively low and not necessarily well-matched impedances causing unbalanced signal-source attenuation, having the effect of degraded CMRR. Most simplified analysis assume a 0W source impedance in order to circumvent this problem. Furthermore, resistor inaccuracies, instead of the amplifier itself, will typically dominate the CMRR. These resistors and the amplifier's open-loop gain will determine the differential-to-single ended conversion carried out so well by the CLC520.

However, a classical single-amp differential amplifier combined with a pair of wideband, low-output-impedance buffers can be made to approach the performance of the CLC520. This approach may be preferred if lower input noise, lower power dissipation and improved DC-drift characteristics are worth a higher number of parts, lower differential bandwidth and the necessary precise resistor-matching. Figure 15 provides an example of a single-amp differential amplifier using two buffers from a CLC114 quad buffer and a low-gain op amp with a differential gain of +1V/V.

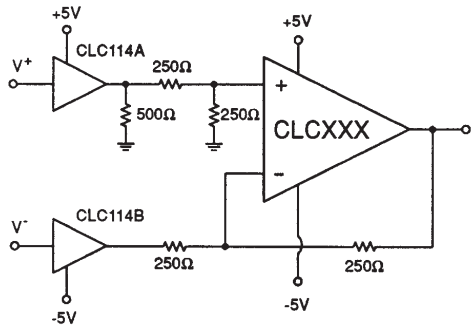


Figure 15: Single amplifier differential amplifier with input buffering

The two input-barriers provide many of the same advantages found with the CLC520 inputs. Any of the input terminations described for the CLC520 may be used here as well. The optional 500Ω resistor to ground on the output of the non-inverting buffer provides a means of matching the loads seen by both buffer outputs. This load matching will improve the high frequency response-match. The four 250Ω resistors should be matched as closely as possible since any mis-match will degrade the CMRR. The recommended low-gain differencing amplifier may be chosen from the following selection of National's wideband low-gain amplifiers.

CLC402 Low-gain high-accuracy current-feed back amplifier
Lower CMRR than the CLC420 with wider bandwidth and better fine-scale, pulse-settling accuracy.

CLC409 Very wideband, low-gain, current-feed back amplifier.

CLC410 Intermediate performance, low-gain, current-feedback amplifier. This part also includes a shutdown feature and provides the best dG/d_ for composite video applications.

CLC420 Unity-gain stable voltage feedback amplifier
This part will provide the best CMRR and DC accuracy

CLC502 Similar to the CLC402 but with an output-clipping feature

All of these parts are optimized for the 250Ω feedback resistor shown in the circuit of Figure 15.

Conclusion

As operating speeds have increased, the need for a wide-bandwidth high-CMRR differential amplifiers has increased. National's CLC520 & CLC522 provide all of the required building blocks integrated into one part. Although intended for adjustable gain requirements, operating the CLC520 at a fixed gain is perfectly acceptable and preferable in a differential receiver application. Signal bandwidths in excess of 150MHz over a wide range of gains, along with CMRR exceeding 60dB through l0MHz,and two matched high-impedance inputs provide all the essential requirements for wideband differential amplification. In some applications using wideband, low power buffers and a standard single op amp differential amplifier topology offers certain advantages over the CLC520 approach.

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National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507