Applying Dual and Quad FET Op Amps

National Semiconductor
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The availability of dual and quad packaged FET op amps offers the designer all the traditional capabilities of FET op amps, including low bias current and speed, and some additional advantages. The cost-per-amplifier is lower because of reduced package costs. This means that more amplifiers are available to implement a function at a given cost, making design easier. At the same time, the availability of more amplifiers-per-dollar means that relatively self contained and sophisticated functions can be designed around a single FET dual or quad package. In addition, duals and quads require less board space, fewer bypass capacitors and less power supply bussing. An inventive designer can capitalize on all of these advantages to produce complex circuit functions at low cost. An example is shown in *Figure 1*.

HIGH EFFICIENCY PRECISION OVEN TEMPERATURE CONTROLLER

In this circuit, a complete, high efficiency pulse width modulating temperature controller is built around a single LF347 package. In *Figure 1*, A1 functions as an oscillator whose output (Trace A, *Figure 2*) periodically resets the A2 integrator output (Trace B, *Figure 2*) back to zero volts. Each time A1's output goes high, a large positive current is forced into A2's summing junction, overcoming the negative current that flows through the 100 kΩ resistor into the LM129 reference. This forces A2's output to head in a negative-going direction ultimately limited by the diode feedback-bound. Another diode provides bias at A2's "+" input to compensate the bound diode and A2's output settles very near zero volts. When the positive output pulse from A1 ends, the positive current into A2's summing junction ceases and A2's output ramps linearly until the next reset pulse.

A3 functions as a current summing servo-amplifier which compares the currents derived from the LM135 temperature sensor and the LM129 reference. In this example A3 operates at a gain of 1000 with a 1 μF capacitor providing 0.1 Hz servo response. A3's output represents the amplified difference between the LM135's temperature and the desired control setpoint, which may be varied by altering the 21.6k value. In this circuit the 21.6k resistor provides a setpoint of 49°C. A3's output is compared to the ramp output of A2 and A4, which is set up as a comparator. A4's output will only be high during the time A3's output is greater than the ramp voltage. The ramp reset pulse is diode-summed with the ramp output (Trace C, *Figure 2*) at A4 to prevent A4's output from going high during the period of the reset pulse. A4's output biases the LM395 power transistor which switches power to the heater (Trace D, *Figure 2*). If the LM135 sensor is tightly coupled to the heater and the oven is well insulated, this controller will easily hold 0.05°C over wide excursions of ambient temperature.

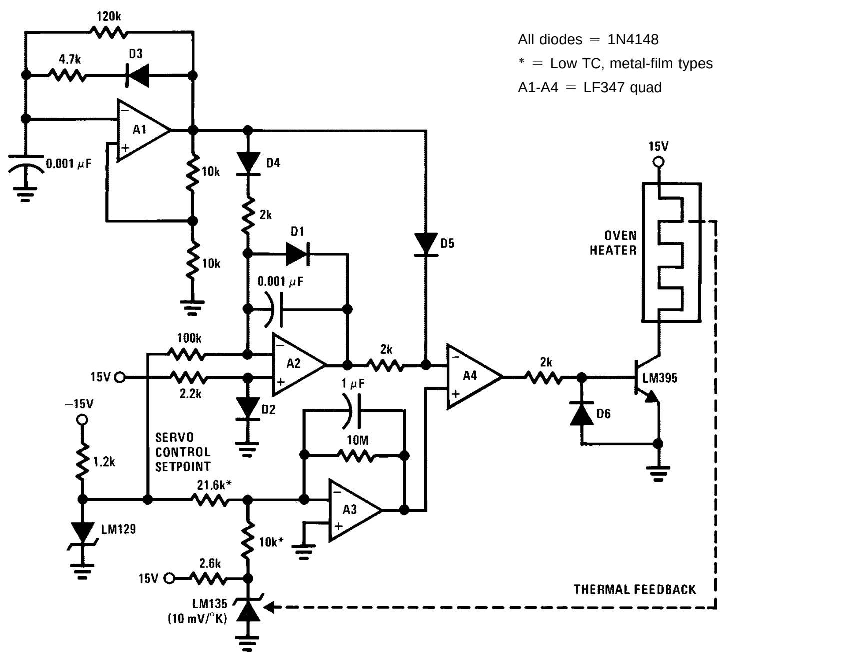

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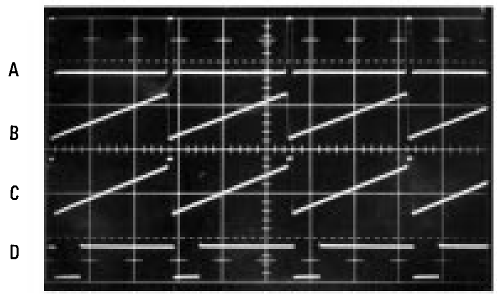
FIGURE 1. Connecting appropriate components to an LF347 quad FET op amp IC produces a high efficiency precision oven temperature controller. This design can hold a temperature within 0.05°C despite wide ambient temperature fluctuations.



TL/H/12587±2

Trace	Vertical	Horizontal
A	20V/Div	
B	10V/Div	50 µs/Div
C	10V/Div	
D	20V/Div	

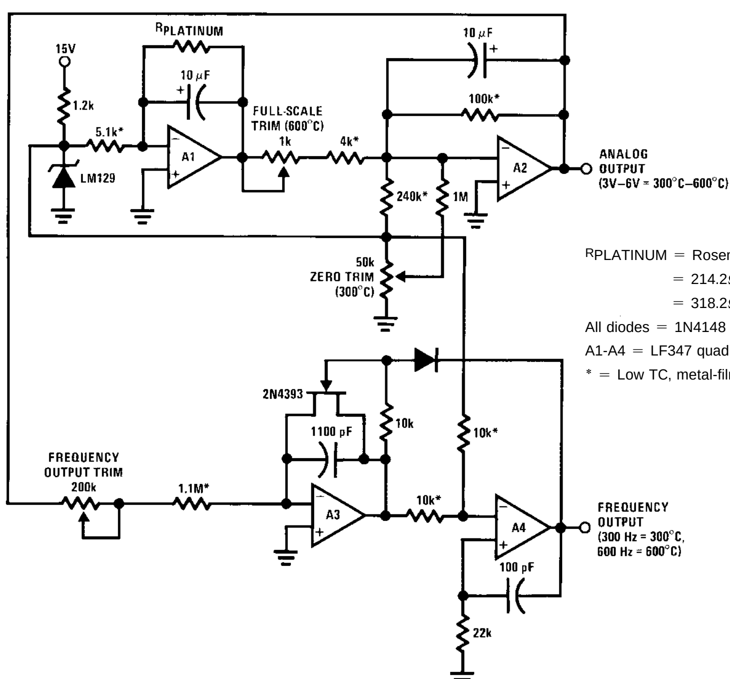
FIGURE 2. Oven-controller waveforms from *Figure 1's* circuit show A1's oscillator output (Trace A) and A2's integrator output (B) as the latter resets periodically to 0V. Trace C displays A4's ramp input, and (D) indicates the LM395's power input to the oven heater.

PLATINUM RTD HIGH TEMPERATURE THERMOMETER WITH ANALOG AND DIGITAL OUTPUTS

Another temperature related circuit appears in *Figure 3*. In this circuit an LF347 is used to signal condition a Platinum RTD and provide simultaneous analog and frequency outputs. These outputs are accurate to ±1°C over a range of 300°C–600°C (572°F–1112°F). Although the circuit maintains linearity over a much wider range the non-linear response of the RTD over wide range is the limitation to accurate, wide range operation (see graph, *Figure 4*).

A1 functions as a negative gain inverter to drive a constant current through the platinum sensor. The LM129 and the 5.1k resistor provide the current reference. Because A1 operates at negative gain the voltage across the sensor is extremely low and self-heating induced errors are eliminated. A1's output potential, which varies with the platinum sensor's temperature, is fed to A2. A2 provides scaled gain and offsetting so that its output will swing from 3.00V to 6.00V for a 300°C to 600°C temperature swing at the platinum sensor.

A3 and A4 form a voltage-to-frequency converter which generates a 300 Hz to 600 Hz output from A2's 3V to 6V analog output. A3 integrates in a negative-going direction at a slope which is linearly dependent upon A2's output voltage. A4 compares A3's negative ramp to the LM129's positive reference voltage by current summing in the 10 kΩ resistors. When the negative value of the ramp just exceeds the LM129 voltage A4's output goes positive, turning on the 2N4393 FET and resetting the A3 integrator. AC feedback at A4 causes it to "hang up" in the positive state long enough to completely discharge the integrator capacitor.



RPLATINUM = Rosemount 118 MG
= 214.2Ω at 300°C (572°F)
= 318.2Ω at 600°C (1112°F)
All diodes = 1N4148
A1-A4 = LF347 quad
* = Low TC, metal-film types

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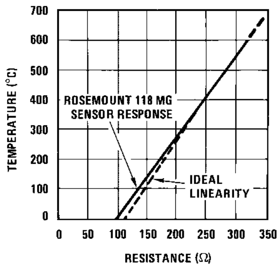
FIGURE 3. Generate simultaneous analog level and frequency outputs using one LF347 package by signal-conditioning a platinum RTD sensor. You can calibrate this high temperature (300°C to 600°C) measuring circuit to ±1°C by using three trimming pots.



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Temperature(°C)	Resistance(Ω)
600	318.2
500	284.7
400	249.8
300	219.2
200	177.3
100	139.2
0	100.0

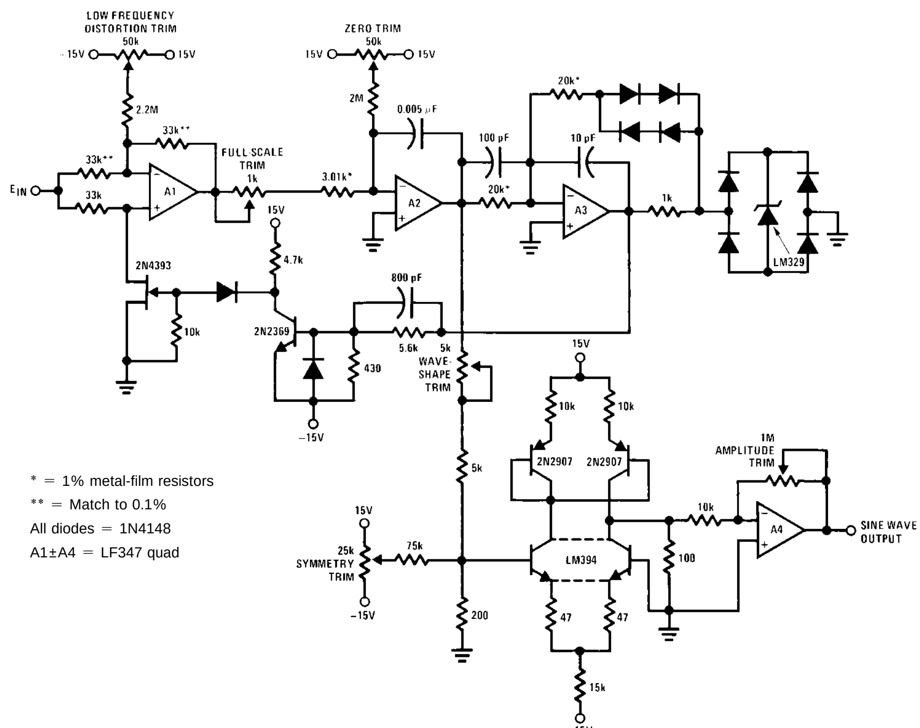
FIGURE 4. A platinum RTD sensor's resistance decreases linearly from 600°C to 300°C. Then, from 300°C to 0°C, the sensor's resistance deviates from a straight line slope and degrades the *Figure 3* circuit's accuracy beyond ±1°C.

To calibrate this circuit, substitute a high quality decade box (e.g., General Radio #1432-K) for the sensor. Alternately adjust the zero (300°C) and full-scale (600°C) potentiometers for the resistance values noted in *Figure 4* until A2's output is calibrated. Next, adjust the 200 kΩ frequency output trim so the frequency output corresponds to the analog value at A2's output.

VOLTAGE CONTROLLED SINE WAVE OSCILLATOR

Figure 5 diagrams a very high performance voltage controlled sine wave oscillator which uses a single LF347 package. For a 0V±10V input the circuit produces sine wave outputs of 1 Hz to 20 kHz with better than 0.2% linearity. In addition, distortion is about 0.4% and the sine wave output frequency and amplitude settle instantaneously to a step input change. The circuit's sine wave output is achieved by non-linearly shaping the triangle wave output of a voltage-to-frequency converter.

Assume the 2N4393 FET is on and A1's output has just gone low. With the FET on, A1's "+" input is grounded and A1 functions as a unity gain inverter. In this state its output will be equal to $-E_{IN}$ (Trace A, *Figure 6*). This negative voltage is applied to the A2 integrator which responds by ramping in a positive direction (Trade B, *Figure 6)*. This positive-going ramp is compared by A3 to the LM329 7V reference which is contained within its symmetrically bounded positive feedback loop. The paralleled diodes compensate the diodes in the bridge. When the positive-going ramp voltage just nulls out the −7V produced by the LM329, diode



* = 1% metal-film resistors
** = Match to 0.1%
All diodes = 1N4148
A1±A4 = LF347 quad

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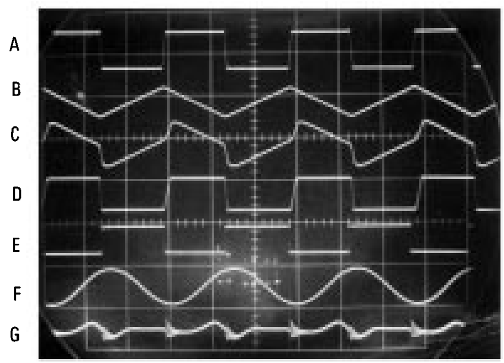
FIGURE 5. An LF347-based voltage-controlled sine wave oscillator combines high performance with versatility. For 0V to 10V inputs, this circuit generates 1 Hz to 20 kHz outputs with better than 0.2% linearity and only 0.4% distortion.

bound A3's output goes positive (Trace D, *Figure 6*). The 100 pF capacitor provides a frequency adaptive trim to A3's trip point, aiding V/F linearity at high frequencies by compensating A3's relatively slow response time when used as a comparator. The 10 pF capacitor provides AC positive feedback to A3's positive input (Trace C, *Figure 6*). The positive output of A3 is inverted by the 2N2369 transistor which also has the effect of further shortening A3's response time. It does this by using a heavy feed-forward capacitor in its base drive line. This allows the transistor to complete switching just barely after the A3 output has begun to move! (Trace E, *Figure 6*). The 2N2369's negative output turns off the 2N4393 FET. This lifts A1's ``+'' input from ground and causes A1 to become a unity gain follower. This forces A1's output to immediately slew to the value of E_{IN}. This causes the A2 integrator to reverse in direction, forming a triangle wave. When A2 ramps far enough negative A3 will again switch and the entire cycle will repeat. The triangle output at A2 is fed to the discrete transistors which form a sine shaper. This configuration uses the logarithmic relationship between collector current and V_{BE} in transistors to smooth the triangle wave. The last amplifier in the quad package provides gain and buffering and furnishes the sine wave output (Trace F, *Figure 6*).



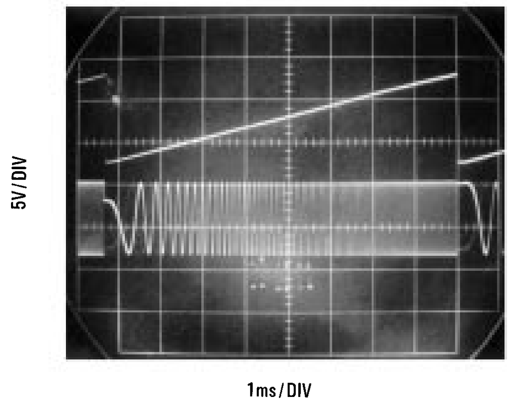
TL/H/12587±6

Trace	Vertical	Horizontal
A	20V/Div	
B	20V/Div	
C	10V/Div	
D	20V/Div	20 μs/Div
E	50V/Div	
F	2V/Div	
G	0.2VDiv	

FIGURE 6. Waveforms from the oscillator shown in *Figure 5* show that upon receiving A1's negative voltage (Trace A), A2 ramps in a positive direction (B). This ramp joins the AC feedback delivered to A3's positive input (C); Trace D depicts A3's positive-going output. This output in turn is inverted by the 2N2369 transistor (E), which turns off the 2N4393 and drives A1's positive input above ground. A2's triangle output also connects to four sine-shaper transistors and A4 and finally emerges as the circuit's sine wave output (F). A distortion analyzer's output (G) shows the circuit's minimum distortion products after trimming.

To calibrate the circuit apply 10V to the input and adjust the wave shape trim and symmetry trim for minimum distortion on a distortion analyzer. Next, adjust the input voltage for an output frequency of 10 Hz and trim the low frequency distortion potentiometer for minimum indication on the distortion analyzer. Finally, alternately adjust the zero and full-scale potentiometers so that inputs of 500 μV and 10V yield respective outputs of 1 Hz and 20 kHz. Distortion products are shown in Trace G, *Figure 6*.

This circuit provides an unusually clean and wide ranging response to rapidly changing inputs, something most sine wave oscillators cannot do. *Figure 7* shows the circuit's response to a 10V ramp applied to the input. The output is singularly clean, with no untoward dynamics, even during or following the high speed reset of the ramp.



TL/H/12587±7

FIGURE 7. Applying a 10V ramp input (top trace) to the *Figure 5* circuit's input produces an extremely clean output (bottom trace) with no glitches, ringing or overshoot, even during or after the ramp's high speed reset.

SINE WAVE VOLTAGE REFERENCE

Figure 8 depicts a simple and economical sine wave circuit which provides a fixed 1 kHz output with a precise 2.50 Vrms amplitude. The circuit may be used as inexpensive AC calibration source or anywhere an amplitude stabilized AC source is required. Q1 is set up in a phase shift oscillator configuration and oscillates at 1 kHz. The sine wave at Q1's collector is AC coupled to A1, which has a closed loop gain of about 5. A1's output, which is the circuit's output, is half-wave rectified by the diode and a DC potential appears across the 1 μF capacitor.

This positive voltage is compared by A2 to a voltage derived from the LM329 reference. The diode in the potentiometer wiper arm compensates the rectifying diode. The diode in A2's feedback loop prevents negative voltages from being applied to Q1 (and the feedback capacitor, an electrolytic) on start-up. A2 amplifies the difference of the reference and output signals at a gain of 10. The output of A2 is used to provide collector bias for Q1, completing an amplitude stabilizing feedback loop around the oscillator. The 2 μF electrolytic provides stable loop compensation. The 5 kΩ potentiometer is adjusted so that the circuit output is exactly 2.50V. This output will show less than 1 mV shift for $\pm$5V variation in either supply. Drift is typically 250 μV/°C and distortion is inside 1%.

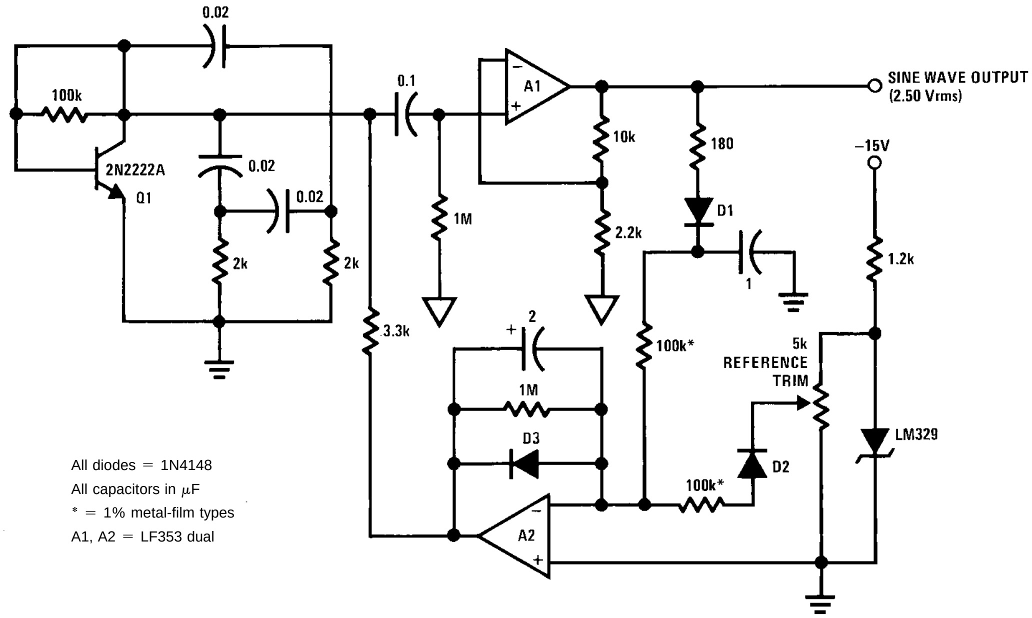


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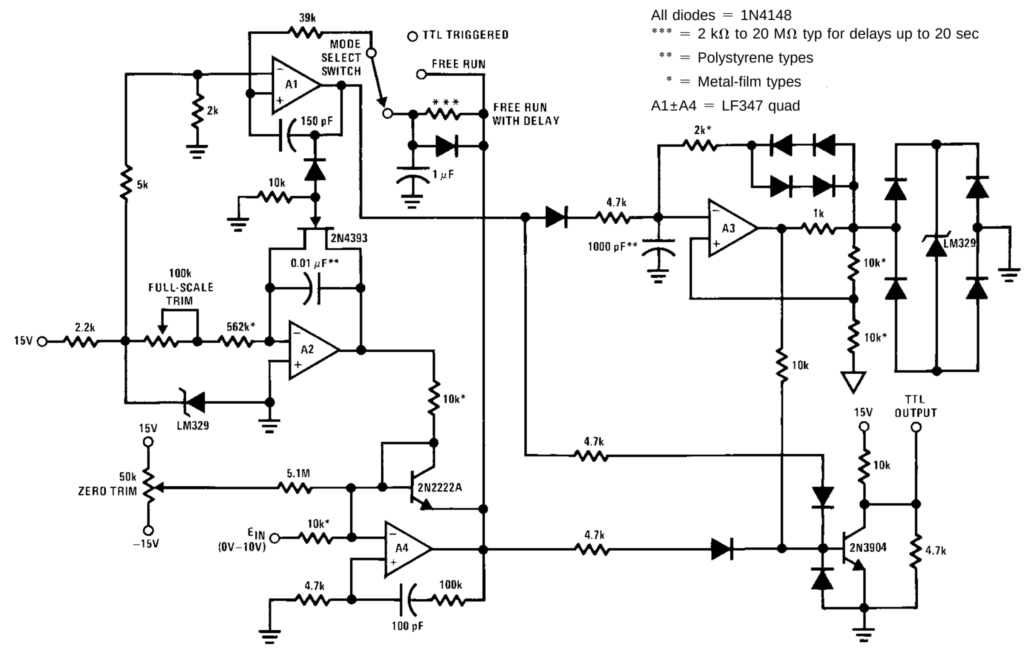
FIGURE 8. Reduce parts count and save money by basing this precision sine wave voltage reference on an LF353 dual FET op amp IC. This circuit generates a 1 kHz sine wave at 2.50 Vrms. The 2N2222A transistor functions as a phase-shift oscillator. The A1, A2 combination amplifies and amplitude stabilizes the circuit's sine wave output.

ANALOG-TO-DIGITAL CONVERTER

An extremely versatile integrating analog-to-digital converter appears in *Figure 9*. A single LF347 quad implements the A/D converter which can be either internally or externally triggered. As shown, the converter provides a 10-bit serial output word with a 10 ms full-scale conversion time.

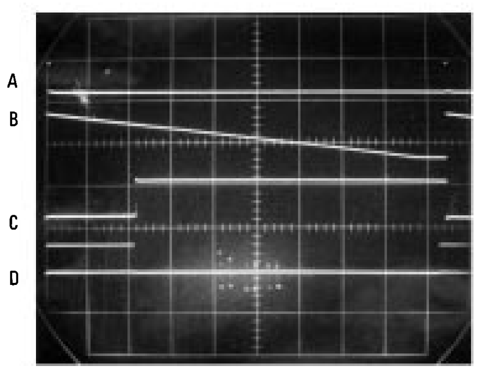
To understand this circuit assume the mode select switch is in the ``free run with delay'' position and the 2N4393 FET has just been turned off. The A2 integrator, biased from the LM129 reference, begins to ramp in a negative-going direction (Trace B, *Figure 10*). The 2N2222A transistor provides a −0.6V or a +7V feedback output bound for A4, keeping its output from saturating and aiding high speed response. AC positive feedback assures clean transitions. A3 is set up as a 100 kHz oscillator. The LM329 and the diodes provide a temperature compensated bipolar switching threshold reference for the oscillator. During the time A4 is low the pulses from A3's output are passed by the 2N3904 transistor. When A4 goes high the 2N3904 is biased on and no more pulses appear (Trace D, *Figure 10*). Since A2's output ramp is linear the length of time A4 spends low is directly proportional to the value of E_{IN}. The number of pulses at the 2N3904 output provides a digital indication of this information. A2's ramp continues to run after A4 goes high and the actual conversion ends. When the time constant associated with the ``free run with delay'' mode charges to 2V A1's output goes high (Trace A, *Figure 10*), turning on the 2N4393 FET, which resets the integrator. A1 stays high until the AC feedback provided by the 150 pF capacitor decays below 2V. At this point A1 goes low, A2 begins to ramp and a new conversion cycle starts. False data at the converter output is prevented during the time A1 is high by resistor diode gating at the 2N3904 base.

Normally, a ±1 count uncertainty at the output will be introduced because the 100 kHz clock runs asynchronously with the conversion cycle. This problem is eliminated by the diode and 4.7k resistor which run between A1's output and the A3 negative input. These components force the oscillator to synchronize to the conversion cycle at each falling edge of A1's output. The length of time between conversions in the ``free run with delay'' mode is adjustable by varying the RC combination associated with this switch position. The converter may be triggered externally by any source with a greater than 2V amplitude. In the ``free run'' mode the converter self triggers immediately after A4 goes high. Thus, the conversion time will vary with the input voltage.



TL/H/12587±9

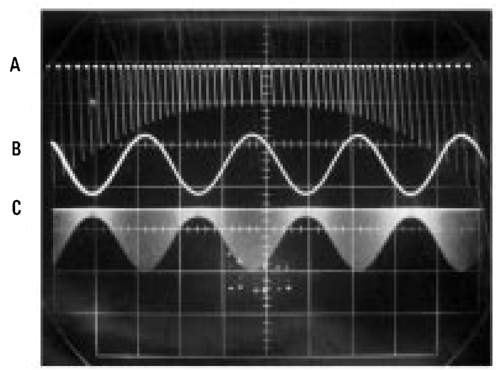
FIGURE 9. Three mode select switch positions offer a choice of internal or external trigger conditions for this integrating A/D converter. Over 15°C to 35°C, this trimmable converter provides a 10-bit serial output, converts in 10 ms and accepts 0V to 10V inputs.



TL/H/12587±10

Trace	Vertical	Horizontal
A	5V/Div	1 ms/Div
B	10V/Div	
C	10V/Div	
D	5V/Div	

FIGURE 10. Depicting the operation of *Figure 9's* A/D circuit in ``free run with delay'' mode, Trace A shows A1's output low. In this state, integrator A2 starts to ramp in a negative-going direction (Trace B). When A2's ramp potential barely exceeds the input voltage's negative value, A4's output goes high (C). This transition turns on the 2N3904 transistor, which shuts off the TTL output pulse train (D).



TL/H/12587±11

Trace	Vertical	Horizontal
A	1V/Div	2 ms/Div
B	5V/Div	20 ms/Div
C	5V/Div	20 ms/Div

FIGURE 11. Illustrating the A/D converter's operation in the ``free run'' mode, Trace B shows a positively biased sine wave input. Because reset and self trigger occur instantly after conversion. A2's output produces a ramp-constructed envelope of the input (Trace C). Trace A shows a time expanded form of the envelope waveform.

HIGH OUTPUT CURRENT AMPLIFIER

Figure 12 shows a scheme for obtaining high output current into a load by using all 4 amplifiers in an LF347 to supply output power. It operates on the principle that all the amplifiers have to supply the same current as A1, whether that current is plus, minus or zero. A single LF347 can be used to drive a 600Ω load to ±11V in this fashion. Two LF347 packages permit ±40 mA of output current. The series RC damper prevents oscillations. The circuit of *Figure 13* is similar but features a gain of 10 and output to a floating load. A1 amplifies the signal and A2 helps it drive the load. A3 operates as a unity gain inverter and A4 helps it to drive the load. This circuit will easily drive a 2000Ω floating load to ±20V.

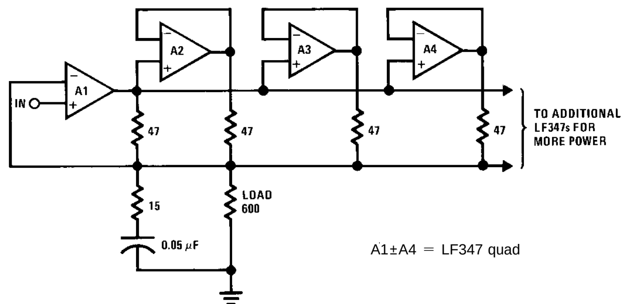


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FIGURE 12. Utilizing current-amplifying capabilities, one LF347 can drive a 600Ω load to ±11V. For additional power, two LF347's can supply an output current of ±40 mA.

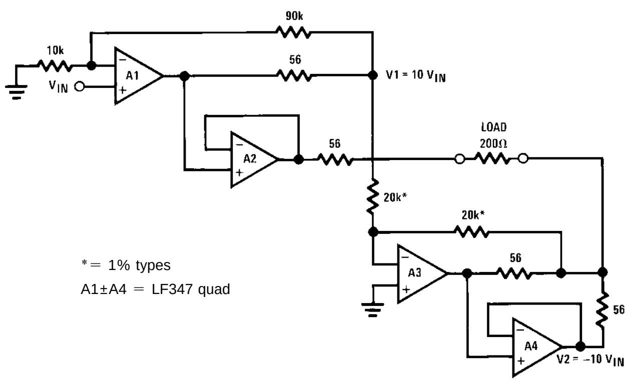

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FIGURE 13. Configured as a high output current amplifier with a gain of 10, this LF347 circuit can drive a 200Ω floating load to ±20V.

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