DATA SHEET

A high-speed converter for every application

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Philips
Semiconductors

PHILIPS

A HIGH-SPEED CONVERTER FOR EVERY APPLICATION

ADCs and front-ends

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	ENOB[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
6-bit								
TDA8705	2 × 6	40	±0.25	5.8 (10)	250	5 V; TTL	SO28	internal reference
TDA8705A	2 × 6	80	±0.25	5.8 (20)	250	5 V; TTL	SO28	internal reference
TDA8706	6	20	±0.5	5.7 (4.43)	300	5 V; TTL	DIP20, SO20	analog YUV, MUX
TDA8706A	6	40	±0.2	5.8 (4.43)	36	2.7 to 5.5 V; TTL	SSOP24	analog RGB, MUX; –40 to +85 °C
TDA8707	3 × 6	35	±0.35	5.3 (4.43)	335	5 V; TTL	QFP44	RGB inputs; –40 to +85 °C
8-bit								
TDA8703	8	40	±0.5	7.1 (4.43)	290	5 V; TTL	DIP24, SO24	see TDA8790 (new device)
TDA8708A	8	32	±0.5	6.7 (4.43)	365	5 V; TTL	DIP28, SO28	CVBS and Y inputs; AGC and clamp
TDA8709A	8	32	±0.5	6.7 (4.43)	380	5 V; TTL	DIP28, SO28	U, V, C, RGB inputs; gain control and clamp inputs
TDA8714	8	75	±0.2	7.7 (4.43) 7.2 (10)	340	5 V; TTL	SO24, SSOP24	40, 60 and 75 Msps versions
TDA8716	8	120	±0.25	7.5 (10)	780	–5.2 V; ECL	DIP24, SO32	–
TDA8718	8	600	±0.3	6.5 (100)	990	–5.2 V; ECL	PLCC28	–
TDA8752[2]	3 × 8	80	±0.5	7.0 (4.43)	1000	5 V; TTL	QFP100	100 MHz gain amp; PLL; clamp; I^2C-bus
TDA8753A	3 × 8	20	±0.5	7.2 (4.43)	500	5 V; TTL	SDIP42	clamp; YUV: 4 : 1 : 1
TDA8755	3 × 8	20	±0.3	7.1 (4.43)	550	5 V; TTL	SO32	clamp; YUV: 4 : 1 : 1
TDA8758	2 × 8	32	±0.4	7.1 (4.43)	530	5 V; TTL	LQFP48	Y/C interface
TDA8785	8 (+8-bit DAC)	30	±0.4	7.0 (4.43)	600	5 V; TTL	QFP44	100 MHz gain amp; fast offset amp.

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	ENOB[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
TDA8790	8	40	±0.25	7.3 (4.43)	30	2.7 to 5.5 V; CMOS	SSOP20	4 mW standby
TDA8792	8	25	±0.3	7.3 (4.43) 7.0 (10)	53	3.3 V; TTL	SSOP24	30 MHz input bandwidth
TDF8704	8	50	±0.2	7.4 (4.43)	380	5 V; TTL	SO24	–40 to +85 °C; for automotive
9-bit								
TDA8761A	9	40	±0.3	8.2 (10)	185	5 V/3 V; TTL	SSOP28	256 QAM
10-bit								
TDA8760	10	40	±0.6	8.2 (10)	850	5 V; TTL	PLCC44	220 MHz input at –3 dB
TDA8762A	10	80	±0.3	9.3 (4.43)	380	5 V; TTL	SSOP28	60 and 80 Msps versions
TDA8763	10	50	±0.5	9.2 (4.43)	240	5 V/3 V; TTL	SSOP28	internal ref.; 30, 40 and 50 Msps versions
TDA8763A	10	50	±0.5	9.2 (4.43)	195	5 V/3 V; TTL	SSOP28	30, 40 and 50 Msps versions
TDA8766	10	20	±0.25	9.3 (10)	53	2.7 to 5.25 V; CMOS	LQFP32	5 × 5 × 1.4 mm package
TDA8779[2]	2 × 10 (+2 × 10 DAC)	20	±0.5	9.2 (5.0)	520	5 V/3 V; TTL	QFP44	quadrature transceiver for telecom
TDA8786	10 (+CDS + AGC); note 3	18	±0.5	9.0 (4.43)	400	5 V/3 V; TTL	LQFP48	control DAC with 3-wire interface
12-bit								
TDA8767	12	30	±0.75	–	335	5 V/3 V; TTL	QFP44	differential or single input

Notes

1. Effective Number Of Bits (ENOB) measured at maximum speed; value in brackets is the input rate in MHz.
2. In development; production 1Q 97.
3. Correlated Double Sampling (CDS).

DACs

TYPE NUMBER	RESOLUTION (BITS)	CONVERSION RATE MAX. (Msps)	DNL RAMP INPUT AT MAX. SPEED (LSB)	SFDR[1]	DISSIPATION (mW)	SUPPLY VOLTAGE AND I/O	PACKAGE	FEATURES/ REMARKS
8-bit								
TDA8702	8	30	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–
TDA8712	8	50	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–
TDF8712	8	50	±0.5	–52 (4.43)	250	5 V; TTL	DIP16, SO16L	–40 to +85 °C
TDA8771	3 × 8	35	±0.5	–50 (4.43)	200	5 V; TTL	QFP44	3 V output; 1 kΩ load
TDA8772/A	3 × 8	85	±0.5	–50 (4.43)	405	5 V; TTL	QFP44	1 V output; 75 Ω load
10-bit								
TDA8775	3 × 10	50	±0.5	–55 (4.43)	395	5 V; TTL	LQFP48	0.7 V output; 37.5 Ω or 150 Ω load
TDA8776	10	500	±0.2	–68 (10)	925	–5.2 V; ECL	PLCC28	internal reference; 50 Ω output load
TDA8776A	10	1000	±0.2	–60 (50)	925	–5.2 V; ECL	PLCC28	internal reference; 50 Ω output load

Notes

1. SFDR measured at maximum speed; value in brackets is output rate in MHz.