PULNiX **TECHNICAL NOTE**

NO. TH-1062 DATE 8-16-90

EXTERNAL SYNC INPUT IMPEDANCE EFFECT

Recently we observed an external sync problem related to the input impedance of PULNiX cameras. The problem was that some cameras would not sync to a vision system's horizontal sync and the resulting picture on the display was dozens of horizontal bars (Figure 1).

This is a typical characteristic of video when the horizontal frequency is higher than the monitor's capture range. The problem turned out to be a subtle variation in the pulse edge which would not show up during routine factory testing.

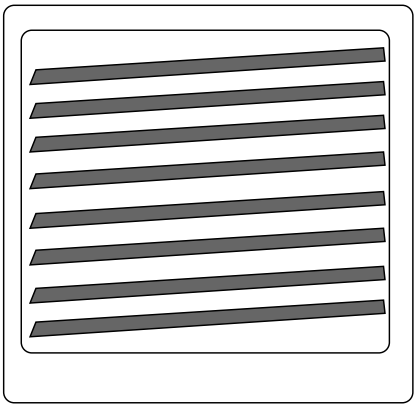


Fig.1

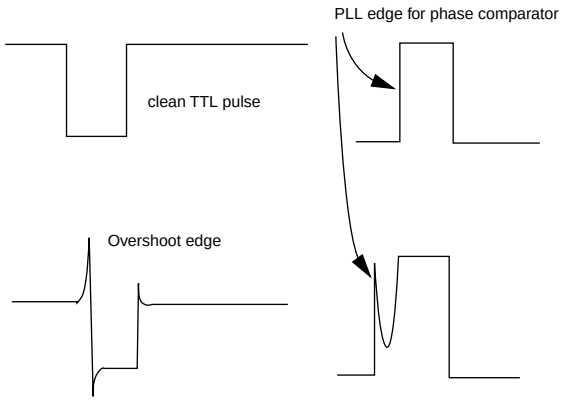


Fig.2

The initial investigation was done with a TM-765. The PLL (Phase Lock Loop) input inside the camera was not receiving a clean pulse due to the over shoot of the input external sync (Figure 2).

1. Input impedance

PULNiX cameras are designed with the external sync impedance to accept direct TTL pulses from TTL ICs.The typical impedance is 4.7KΩ. Some other manufacturers' cameras use 75Ω and require an external sync driver in the vision system.

2. Clean pulse, overshoot or ringing

The transistor driver occasionally outputs horizontal pulses with overshoot or ringing edges. Since the PLL needs a clean edge to lock the frequency, these peaked pulses confuse the phase locking.

3. Solution

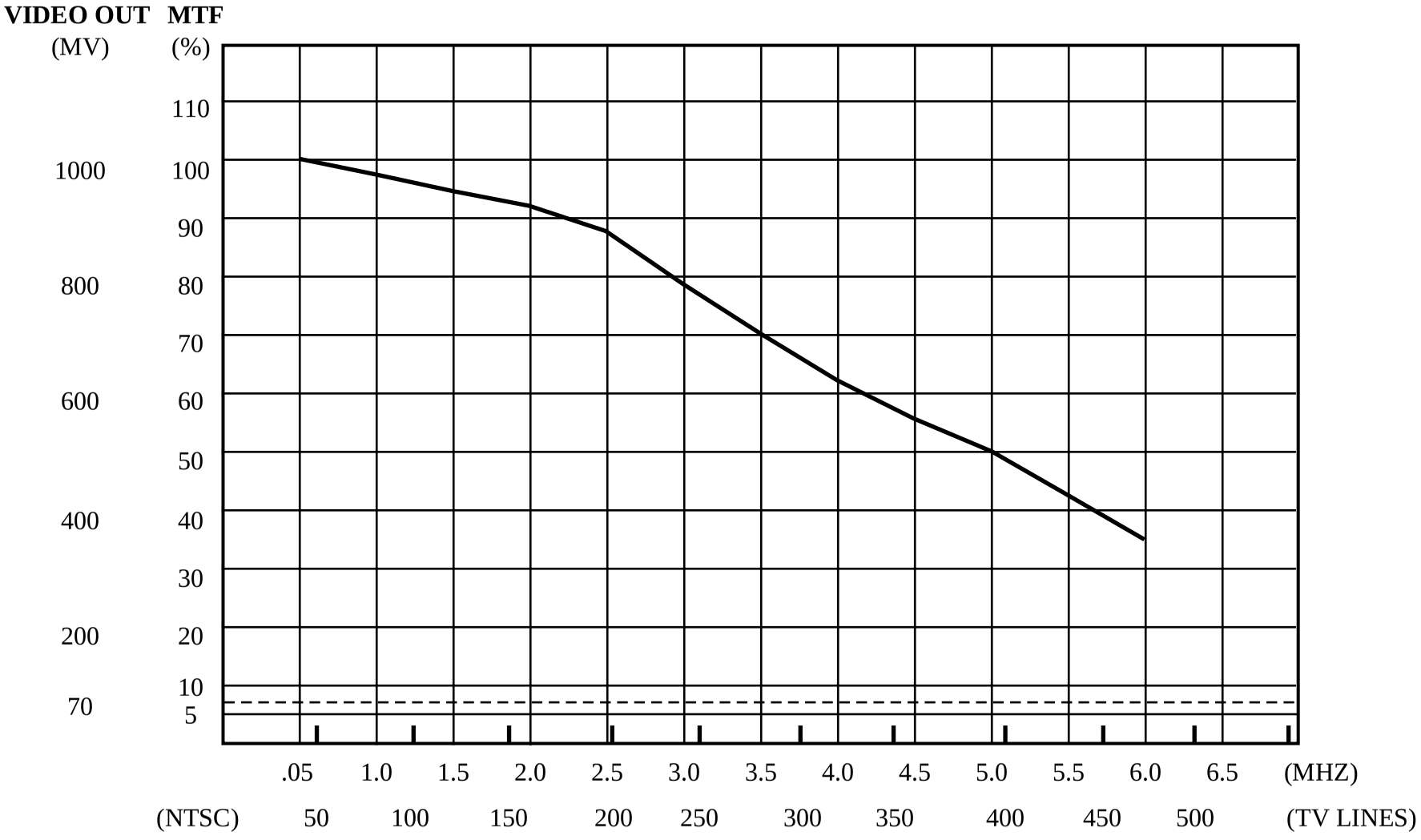
By reducing input impedance at the camera input, such pulses can be suppressed and potential noises can be eliminated from running cables.

4. Option T (SONY compatible pinout option)

Since the majority of SONY CCD cameras come with 75Ω termination, PULNiX will change the impedance spec to 75Ω instead of 4.7KΩ. Please consult PULNiX for further information in order to optimize impedance matching.

MTF AND RESOLUTION CHART

TM-7EX



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