design ideas

Edited by Bill Travis and Anne Watson Swager

Delay line aids in one-shot simulations

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Many designers use small pulse generators to delay signals, open timing windows, drive sample/hold circuits, and other functions. Though the hardware implementation of these generators does not pose any problems, the lack of dedicated circuitry sometimes puzzles the Spice simulation of the system. A common approach to this problem is to implement a time constant involving a resistor, a capacitor, and a comparator. Unfortunately, each time you need a time constant, you must recalculate the resistor value, the capacitor value, or both. Despite the fact that inline equations can do this job for you, delay lines can often offer a smarter solution. **Figure 1** shows the implementation of a small pulse generator. The operating principle of the circuit lies in applying two "1" levels to the AND-gate input before the delay line switches high. **Figure 2** shows the signals associated with the circuit in **Figure 1**. **Listing 1** shows netlists for Intusoft's IsSpice4 and Cadence's PSpice.

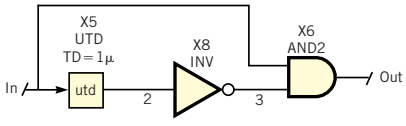

Figure 1 A one-shot multivibrator (shown with Spice nomenclature) makes a simple short-pulse generator.

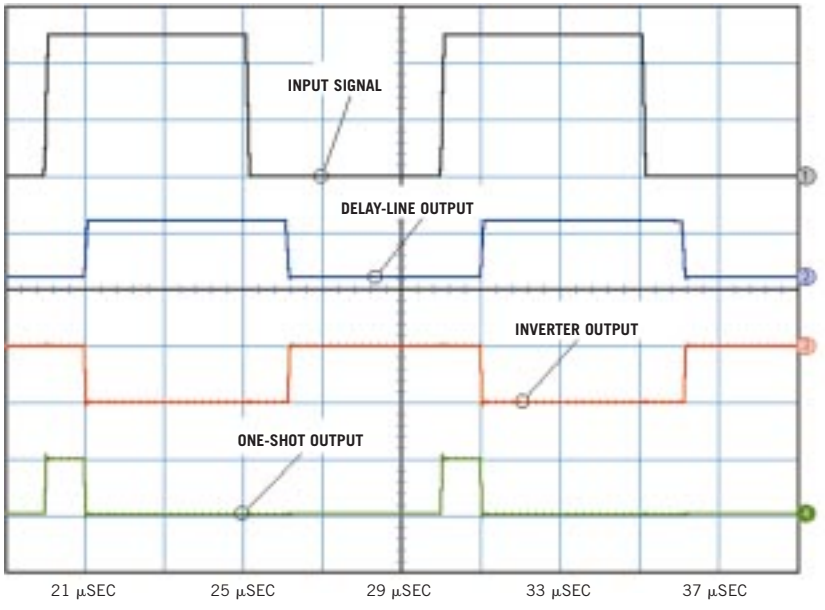

Figure 2 This plot shows timing details for Figure 1's Spice model.

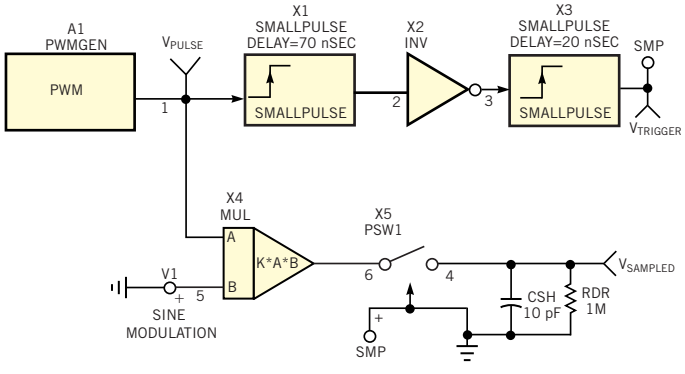

Figure 3 This PWM application is a sample/hold circuit in Spice-simulation nomenclature.

Figure 3 shows a typical application circuit for the one-shot multivibrators. You can use IsSpice4 or PSpice to simulate this sample/hold circuit. **Figure 4** shows the waveforms associated with the circuit in **Figure 3**. A PWM signal (top waveform) generates a kind of arbitrary staircase signal. The multiplier, X4, sinusoidally modulates the PWM signal. The circuit cascades two small pulse generators (SMALLPULSE). One creates a delay signal to sample at a given time (X1, 70 nsec); the other calibrates the width (X3, 20 nsec) of the sampling signal (second waveform). The third waveform in **Figure 4** shows the sinusoidally modulated signal; the fourth waveform is the sampled signal. You can download the IsSpice4 and PSpice listings for three one-shot types from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2680.

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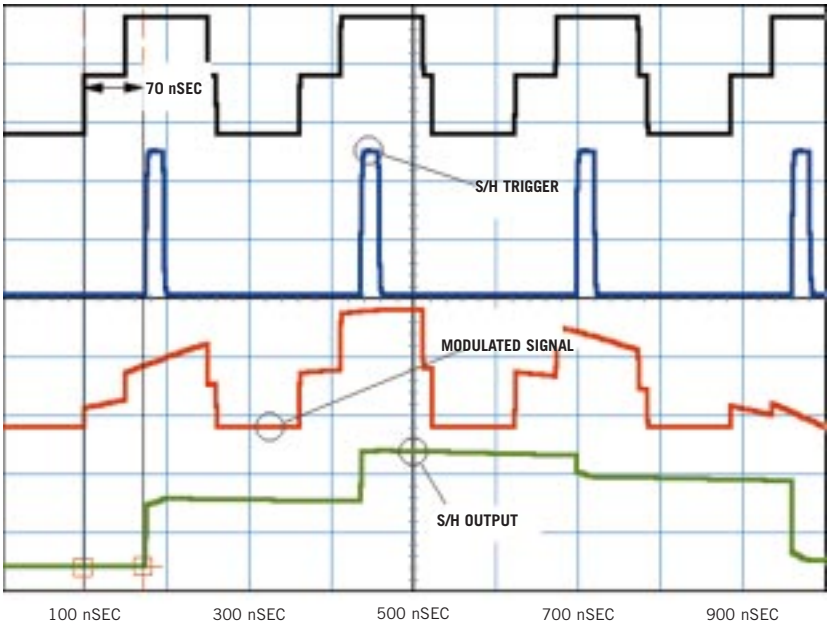


Figure 4 These timing signals illustrate the operation of Figure 3's circuit.

LISTING 1—NETLIST FOR MONOSTABLE SHORT-PULSE GENERATOR

IsSpice4

```
.SUBCKT SMALLPULSE In Out {DELAY=3u}
X5 In 2 UTD PARAMS: TD=DELAY
X6 In 3 Out AND2
X8 2 3 INV
.ENDS
*INCLUDE MNFLOPS.LIB
*******
****** MODELS ****
.SUBCKT UTD 1 2 {TD=???}
*
RIN 1 0 1E15
E1 3 0 1 0 1
T1 3 0 2 0 Z0=1 TD={TD}
R1 2 0 1
.ENDS
*******
.SUBCKT INV 1 2
B1 4 0 V= V(1)>800M ? 0 : 5V
RD 4 2 100
CD 2 0 10P
.ENDS INV
*******
.SUBCKT AND2 1 2 3
B1 4 0 V= (V(1)>800M) & (V(2)>800M) ? 5V : 100m
RD 4 3 100
CD 3 0 10P
.ENDS AND2
*******
```

PSpice

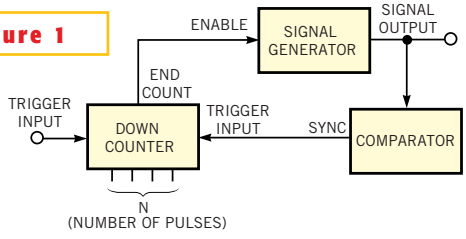
```
SUBCKT SMALLPULSE In Out PARAMS: DELAY=3u
X5 In 2 DL PARAMS: TD={DELAY}
X6 In 3 Out AND2
X8 2 3 INV
.ENDS
*******
****** MODELS ****
.SUBCKT DL 1 2 PARAMS: TD=500n
*
RIN 1 0 1E15
E1 3 0 1 0 1
1 3 0 2 0 Z0=1 TD={TD}
R1 2 0 1
ENDS DL
*******
**** 1 INPUT INVERTER ****
.SUBCKT INV 1 2
EB1 4 0 VALUE = { IF ( V(1)>800M, 0, 5V ) }
RD 4 2 100
CD 2 0 10P
.ENDS INV
*******
**** 2 INPUT AND CIRCUIT ****
.SUBCKT AND2 1 2 3
EB1 4 0 VALUE = { IF ( (V(1)>800M) & (V(2)>800M), 5V, 0 ) }
RD 4 3 100
CD 3 0 10P
ENDS AND2
*******
```

Sine-wave generator outputs precise periods

JM Terrade, Clermont-Ferrand, France

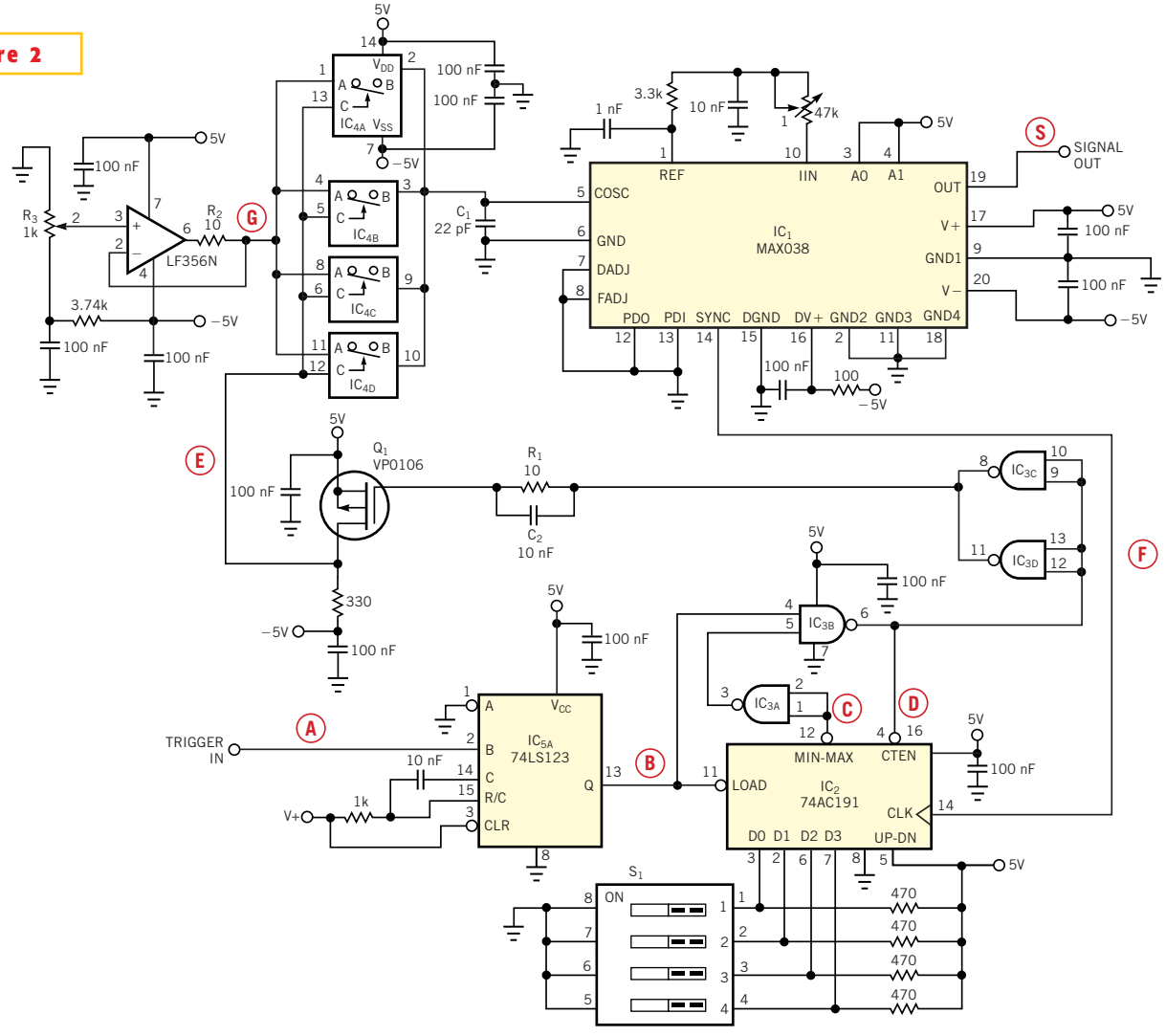
RECTANGULAR PULSE generators, even at high frequencies, are easy to design. However, the design becomes more difficult if you need a signal that contains a precise number of periods with a sinusoidal shape. Although it is easy to produce a good sine wave, the difficulty is producing a signal with a precise number of periods. The signal has to start and stop exactly at 0V. The scheme in **Figure 1** can produce one to 15 periods of a 20-MHz sinu-

Figure 1



A signal generator, down counter, and comparator can produce an output signal that contains a precise number of sine-wave periods.

Figure 2



IC_1 contains the generator and comparator. The sync signal at point F drives the counter, IC_2. The setting of S_1 determines the end of count and thus the number of periods, N, at the output.

soidal wave. The scheme has two main characteristics: The positive edge of a 5V signal triggers the input, and the output is one to 15 periods of a 20-MHz signal, adjustable to within ±10%.

Initially, the trigger input is inactive, the generator is disabled, and the counter is loaded with the number N. When the trigger input becomes active, the counter waits, and the end-count output enables the generator. A sine wave appears at the output. At the end of each period of the sine wave, the comparator produces a sync signal that drives the counter's clock input. When N periods of the output wave have occurred, the end-count signal disables the generator.

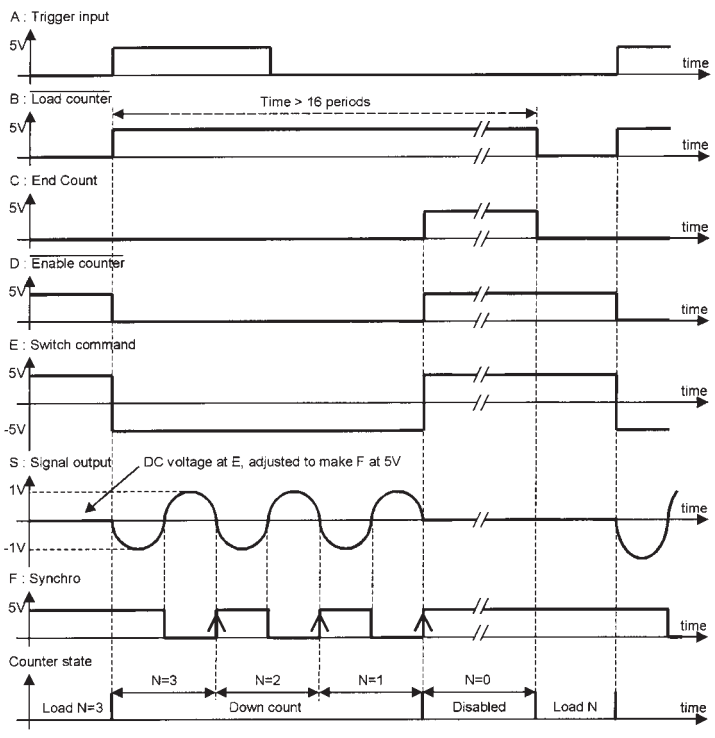
In the actual circuit, a MAX038, IC_1, is the generator (**Figure 2**). This IC contains the sine-wave generator and the comparator. The sync signal is available at Pin 14. The counter has to be fast enough to stop the generator before the next output period starts. The 74AC191, IC_2, is a 4-bit up/down counter with preset inputs. NAND gates IC_{3A} and IC_{3B} disable the counter after the end-count goes active. A one-shot circuit, IC_{5A}, ensures that the input trigger pulse is long enough to allow 15 pulses. A MOS switch, IC_4, short-circuits the oscillator capacitor, C_1, to stop IC_1's generator. If the circuit simply grounds C_1 to stop the generator, the output voltage is not zero. To obtain a zero output voltage, the circuit connects input Pin 5 of IC_1 to a negative 0.5V-dc voltage generator comprising an LF356N and associated components.

Because the signal at Pin 5 of IC_1 goes positive and negative, IC_4's switch requires a ±5V supply. The level for the command signal also has to swing positive and negative. MOS transistor Q_1 provides the level-shifting from 0 to 5V logic levels to ±5V, or 4016, logic levels. NAND gates IC_{3C} and IC_{3D} allow a fast drive for Q_1.

The circuit's operation consists of three timing periods: load N with trigger input inactive, down-count with trigger input high, and disabled (**Figure 3**). When the trigger input is inactive, one-shot IC_{5A} is inactive. The level at Point B in the circuit is low, and counter IC_2 is continuously loading the number N that you program using S_1. The level at D is high, and the counter can't run. The voltage at C is low. The circuit connects NAND gates IC_{3C} and IC_{3D} in parallel to provide more current to drive Q_1 faster during switching. C_2 is also necessary to drive Q_1 faster. These NAND gates invert the level at D, and Q_1 is on, driven with 0V through R_1. Thus, a 5V level is present at E, and the IC_4 switches are on. Potentiometer R_3 controls the voltage at G; the LF356N acts as a voltage follower. The 10Ω resistor, R_2, prevents oscillations during switching. C_1 and the MAX038 input represent the charge impedance. The four switches of IC_4 connect in parallel to present a lower resistance of 200Ω/4, or approximately 50Ω, of total resistance. The switches apply the voltage at G to Pin 5 of IC_1, which stops the internal oscillator. The levels at the signal output and at the sync output, F, depend on the voltage at Pin 5. The voltage at F needs to be 5V, and the voltage at Signal Out needs to be as close to 0V as possible. You need to carefully adjust R_3 to match these conditions. The output voltage is just over 0V when G is close to −0.5V.

When the trigger input goes high, one-shot IC_{5A} starts running. The voltage at B also goes high for 10 µsec. This delay must be longer than 16 periods of the output signal. The voltage at D now goes low and enables the counter. As before, IC_{3C} and IC_{3D} invert the level at D, and the 5V drive turns off Q_1. A −5V level is present at E, and IC_4 switches are off. The internal oscillator of IC_1 is now running, and a signal is present at the output, S. Each time the output signal is positive, the sync output at F is also positive. At the

Figure 3



A timing diagram that corresponds to three periods shows the precise sine-wave output at S.

TABLE 1—WAVEFORM-SHAPE SETTINGS

A_0	A_1	Waveform
X	1	Sine
0	0	Square
1	0	Triangle

end of each period, a positive-going edge appears at F. Each positive edge at F makes counter IC_2 count down by one.

When the circuit has produced N periods at S, the voltage at C goes high, which indicates end of count. The voltage at D goes high and disables the counter. IC_{3C} and IC_{3D} invert the voltage at D, and the resulting 0V drive turns on Q_1. A 5V level is present at E, and IC_4 switches are on. The internal oscillator of IC_1 stops, and the output signal at F returns to zero. Before returning to the original state, the signal at B should return to zero, which happens after the end of the delay that one-shot IC_{5A} produces.

All is now ready for another train of pulses. Using S_1, you can program the circuit for one to 15 pulses. The circuit can produce other signal shapes, depending on how you connect A_0 and A_1 of IC_1 (**Table 1**). You can also replace S_1 with a µC to produce any pattern of pulses.

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High-voltage current-feedback amplifier is speedy

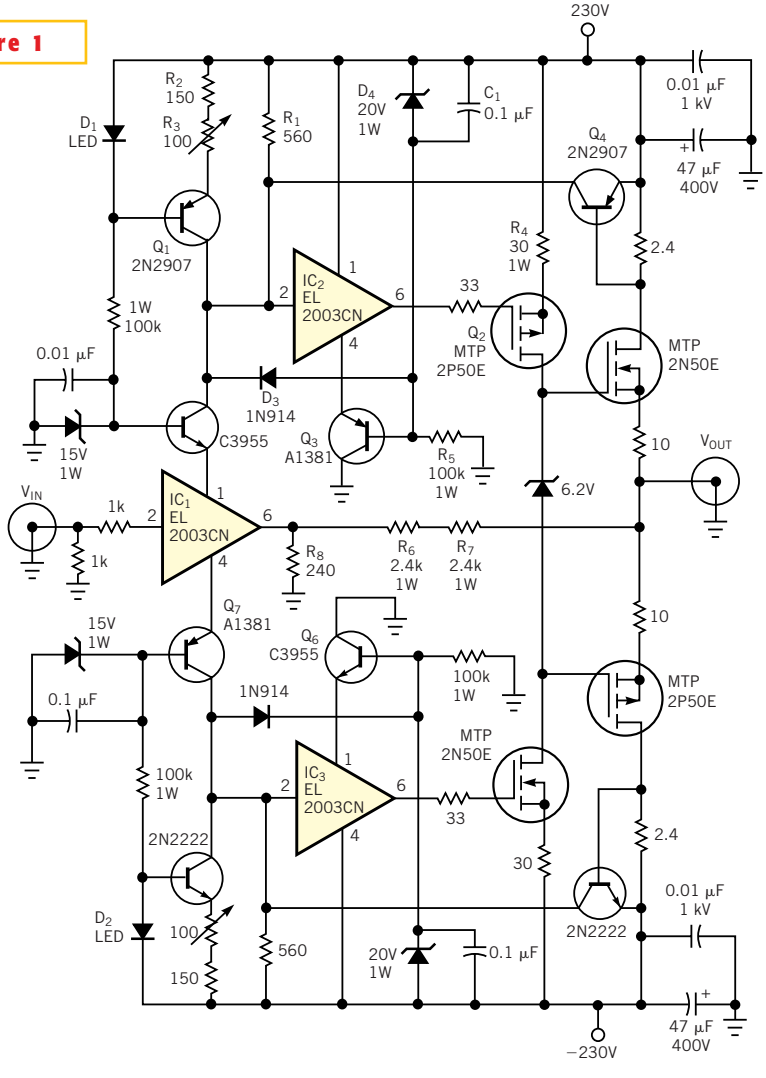
Joseph Ting, Institute of Atomic and Molecular Sciences of the Academia Sinica, Taipei, Taiwan

THE CIRCUIT IN FIGURE 1 powers a microparticle and nanoparticle ion trap through a 1-to-5-turns-ratio, high-voltage transformer. It also works successfully as a driver for a piezo-tube scanner and in a near-field scanning optical microscope. The circuit is robust and works with supplies ranging from ±50 to ±230V. The measured parameters at ±230V supply voltage are gain of 26-dB from dc to −3-dB point at 7 MHz; output swing of ±200V, rise and fall times of 70 nsec for an output step of 350V, slew rate of 4100V/µsec, and supply current of 56 mA.

The red LEDs, D_1 and D_2, in **Figure 1** provide a 1.8V drop; the LEDs are more rugged than precision IC voltage references. The current supply for IC_1 comes from R_1 and the source comprising D_1, R_2, R_3, and Q_1. R_3's trimmed value is such that Q_2's quiescent current is approximately 15 mA. You can determine this current by measuring the voltage drop across R_4. The same adjustment also controls the output-voltage offset. IC_2 is a unity-gain, high-current driver for Q_2. D_3 prevents IC_2's input from going more negative than its negative supply. Q_3, D_4, C_1, and R_5 provide the negative bias for IC_2. Q_4 is an output-current limiting switch. Q_4 starts to turn on at I_{OUT}=290 mA. You can replace the bipolar transistors C3955 (npn, Q_2 and Q_6) and A138 (pnp, Q_3 and Q_7) by equivalents as long as they have the following minimum specs: V_{CEO}≥250V; I_C≥100 mA, and f_T≥100 MHz.

You should mount all the power tran-

Figure 1



This high-voltage, current-feedback amplifier slews at 4100V/µsec.

sistors in individual finned heat sinks with an overhead 3-in. fan for cooling. The pc-board layout is not critical and needs no ground plane. However, you must use single-point grounding to minimize ringing. For the component values shown, the circuit is very stable and needs no compensation capacitors. **Figure 2** shows a large-signal response for a ±9V, 1-MHz square-wave input. This circuit has a fixed gain of 20. For higher gains, you can increase the values of R_6 and R_7. For lower values, it is better to insert an attenuator at the input, because smaller values of R_6 and R_7 may result in excessive dissipation. Do not change the value of R_8, because it is optimized for speed. Be cautious when measuring and using this circuit, because it harbors lethal voltages. The National Science Council of Taiwan sponsored this project.

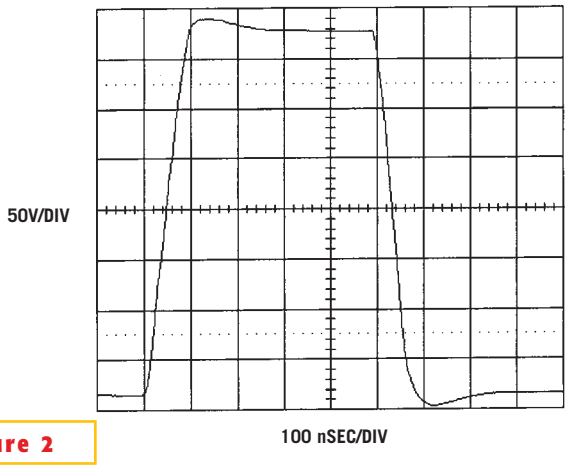


Figure 2

The circuit has a clean square-wave response with minimal overshoot and no ringing.

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AC-power monitor uses remote sensing

Sanjay R Chendvankar, Tata Institute of Fundamental Research, Colaba, Mumbai, India

The detection circuit in the Design Idea "Circuit monitors ac-power loss" (*EDN*, Nov 24, 1999, pg 172) requires a physical connection with the mains to sense the power loss. The circuit in **Figure 1** senses the power loss through the radiated power-line signal. The battery-operated circuit has a quiescent-current drain of approximately 2 µA. The antenna, which is either a telescopic antenna or simply an approximately 2-ft-long wire, intercepts the radiated power-line signal. The CMOS inverters, IC_{1A} and IC_{1B}, amplify this weak signal and convert it into a digital signal. D_1 and C_1 generate a steady dc voltage at the input of IC_{1C}. D_1 prevents discharge of C_1 through the output of IC_{1B} when the square wave at this output periodically goes to a low level. Inverters IC_{1D}, IC_{1E}, and IC_{1F} connected in parallel enhance the current-sink capacity for sinking the piezo-buzzer current. When the ac mains is present, the output of IC_{1C} is low; hence, the levels of IC_{1D}, IC_{1E}, and IC_{1F} are high, and the buzzer is off. When the ac power fails, the output of IC_{1B} goes low; C_1 discharges through R_1; and IC_{1D}, IC_{1E}, and IC_{1F} go low. This level activates the piezo-buzzer and warns of ac-line failure. Switching off the battery power deactivates the buzzer. You can turn S_1 on after ac power resumes.

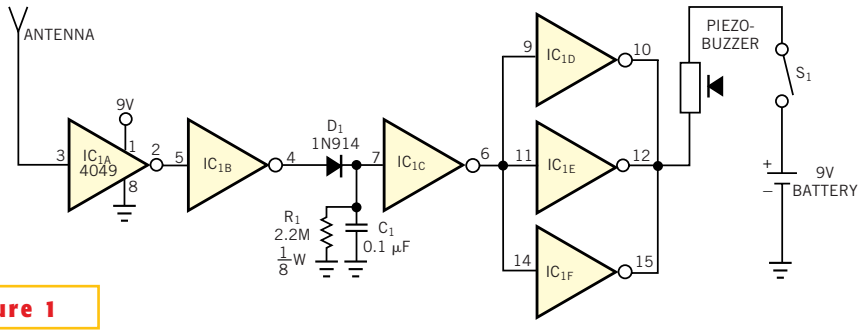

Figure 1

A low level at the outputs of IC_{1D}, IC_{1E}, and IC_{1F} activates the piezo-buzzer and warns of ac-line failure.

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