

# design ideas

Edited by Bill Travis and Anne Watson Swager

## FPGA implements X.50 Division 3 recommendation

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**T**HE SCHEME IN **Figure 1a** uses five delay cells and an XOR gate to configure the data stream for the X.50 Division 3 recommendation of ITU-T. The X.50 recommendation defines the fundamental parameters of a multiplexing scheme for interworking data networks using different envelope structures. Division 3 applies to the interworking between two networks, both of which use the 8-bit envelope structure. X.50 rec-

**TABLE 1—GENERATING THE 0110 PATTERN**

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Value	A	1	1	0	1	0	0	1	0	0	0	0	1	0	1	0	1	1	1	0

ommends a pattern of 19+1 bits, which the following primitive polynomial generates:  $1+x^2+x^5$ . With this polynomial and the initial conditions, **Table 1** generates the pattern 01110. The polynomial does not directly generate the first value, A, in the table because this value depends on the rest of the system. The scheme in **Figure 1a** is typical of a scramble, and is one part of a transmitter/receiver system for data communications. You can implement **Figure 1a** in a 30,000-gate FPGA.

It is important to set the delay cells to the correct initial value. For this design to achieve the correct data stream, the initial data should be 0010110. The use of a 7-bit word for the initial data enables you to change the design to X.50 Divi-

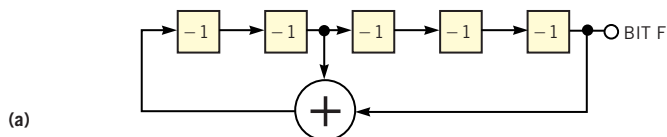
sion 2 by changing only the initial word and the position of the XOR gate. The process for achieving the polynomial is as follows:

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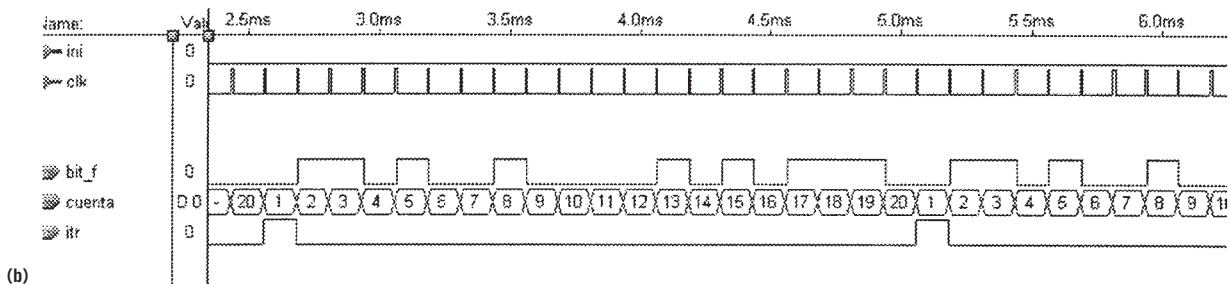
gen_scr:process(clk, count,scr, aux, ini)
begin
  if (ini or aux)='1' then
    scr_new <= "0010110";
  elsif clk'event and clk = '0' then
    for i in 1 to 6 loop
      scr_new(i-1) <= scr(i);
    end loop;
    scr_new(4) <= scr(0) xor scr(3);
  end if;
end process;
  
```

The clk signal is not exactly a true clock signal. This design uses a 244-nsec-wide

FPGA implements X.50 Division 3 recommendation.....	199
Concurrent processing produces fast priority selector .....	200
Proportional thermoregulator synchronizes to line .....	202
Spread-spectrum method identifies audio path .....	204
5-to-1.8V converter works without magnetics .....	206
Band-reject filter includes compensation .....	208
Low-cost active load draws constant battery power .....	210



**Figure 1**



Five delay cells and an XOR gate (a) configure the data stream (b).

clock pulse and a 125- $\mu$ sec period. Rising edges generate the interval number, and falling edges generate the data out. Because 244 nsec is much less than 125  $\mu$ sec, data out is present in all intervals.

You can download the source file from EDN's Web site, [www.ednmag.com](http://www.ednmag.com). Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2509. The

timing diagram in **Figure 1b** shows the resultant data. (DI #2509)

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# Concurrent processing produces fast priority selector

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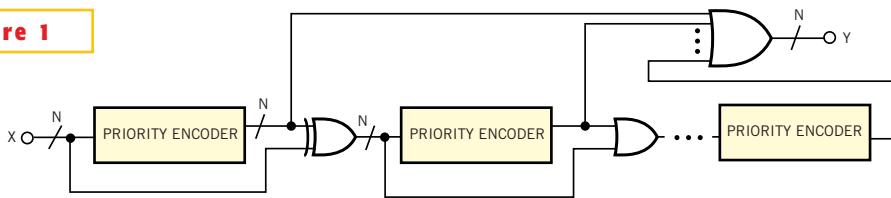
**P**Riority-encoding circuits are common in high-speed digital applications, such as interrupt controllers and task schedulers, for selecting the highest priority set bit of all set bits in a given binary vector. Typically, the bit index corresponds to its priority level. A project required that several logic-function blocks, as opposed to one, would be enabled concurrently at any given time. Accordingly, the design goal was to identify the M highest priority admissible logic blocks. A conventional 1-bit priority selector receives as its input an arbitrary binary vector and outputs a vector of the same size, where the location of the set bit corresponds to the position of the highest priority set bit in the input vector. Such a selector may be described by the following Boolean expressions:

$$Y_i = \left\{ \begin{array}{l} X_1 \\ \left( \sum_{j=1}^{i-1} \overline{X_j} \right) \cdot X_i \end{array} \right\} \cdot X_i = \left\{ \begin{array}{l} \overline{X_1} \\ \left( \sum_{j=1}^{i-1} X_j \right) \cdot X_i \end{array} \right\} \cdot X_i \quad \left. \begin{array}{l} i = 1 \\ i > 1. \end{array} \right\}$$

**Figure 1** depicts a straightforward realization of an N-bit priority selector by means of cascading 1-bit priority selectors. Despite its simplicity, the design introduces extensive delay, which grows linearly with M.

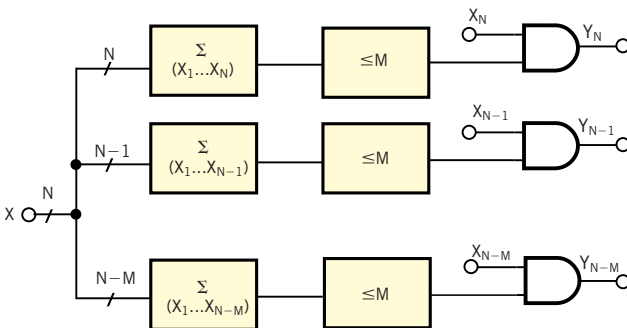
An alternative implementation (**Figure 2**) is based on processing elements of the input vector concurrently as opposed to sequentially. The architecture com-

**Figure 1**



**A straightforward realization of an N-bit priority selector involves cascading a series of 1-bit priority selectors.**

**Figure 2**



**An alternative priority selector processes elements of the input vector concurrently.**

prises a bit-count function, which counts the number of set bits in its input vector, and a comparator. Parallel bit counts are deployed to concurrently determine the number of set bits in subsets of the input vector. A logical 1 at the comparator's output indicates that the bit count is smaller than or equal to M. The result is a binary mark signifying the range of bits in the input vector, which contains the M highest priority set bits. Note that, if N is the input vector length, then only N-M

paths are necessary because the first M bits of the input vector contain by definition at most M set bits. You obtain the final output as a product of the input bits and the corresponding mask bits. The complexity of the bit-count function is  $O(\log N)$ ; hence, the proposed scheme offers a high-speed invariant to M. (DI #2515)

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# Proportional thermoregulator synchronizes to line

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**T**HE CIRCUIT IN **Figure 1** is a proportional thermoregulator in which the switching of the triac occurs when the mains voltage crosses the zero level. As a result, the circuit generates no RFI. The circuit can easily achieve linear regulation and perfect isolation between the control and power sections.

Whenever the mains voltage crosses zero, a 1-msec positive pulse appears at the collector of  $Q_1$ . From the resultant series of pulses, dual binary counter  $IC_1$ , DAC  $IC_2$ , and  $R_4$  generate a sawtooth voltage with a 150-mV amplitude and a 2.56-sec period. Through  $R_4$ , the circuit subtracts this voltage from the constant setpoint voltage,  $V_S$ , that  $R_1$ ,  $R_2$ ,  $R_3$ , and follower  $IC_{3A}$  create. Simultaneously, sensing transistor  $Q_2$  cooperates with  $IC_{3C}$  and associated resistors to create a

voltage proportional to the object's current temperature with a sensitivity of 25 mV/°C.

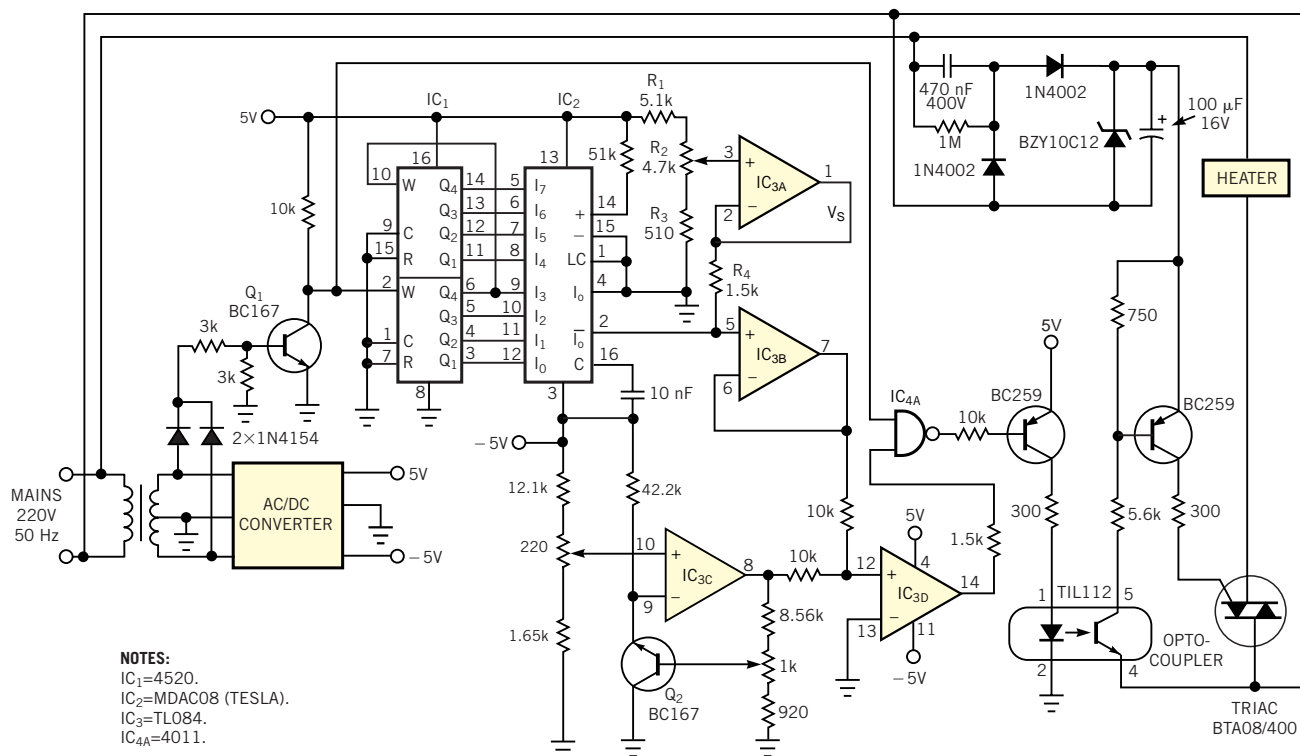
If the difference between the desired and the real temperature of the object exceeds 6°C when the regulator is turned on for the first time, the output of the comparator  $IC_{3D}$  is continuously positive. The 4011 gate,  $IC_{4A}$ , passes all the triggering pulses from  $Q_1$  through the TIL112 optocoupler to the triac's control electrode, and the heater delivers it full power. When the difference in temperatures becomes less than 6°C, the circuit starts working proportionally. In this condition,  $IC_{4A}$  passes only part of the triggering pulses generated within one period of the sawtooth voltage to the triac. The higher the object's temperature, the less time that the gate and the lower the av-

erage power delivered by the heater. When the real temperature reaches the setpoint temperature, the circuit always keeps the gate closed, and the heater is constantly off.

Thus, during the final stage of regulation, the temperature rises smoothly toward the desired value and is free from the overshoots and oscillations around the setpoint that on/off regulators exhibit. The resolution in the region of proportional regulation is as low as 0.4% of the nominal heater power. If necessary, you can change the width of this zone by simply changing  $R_4$ . (DI #2510)

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**Figure 1**



Depending on the object's temperature, which  $Q_2$  senses,  $IC_{4A}$  passes all, part, or none of the triggering pulses to the triac that controls the heater.

# Spread-spectrum method identifies audio path

Bob Dougherty, Nielsen Media Research

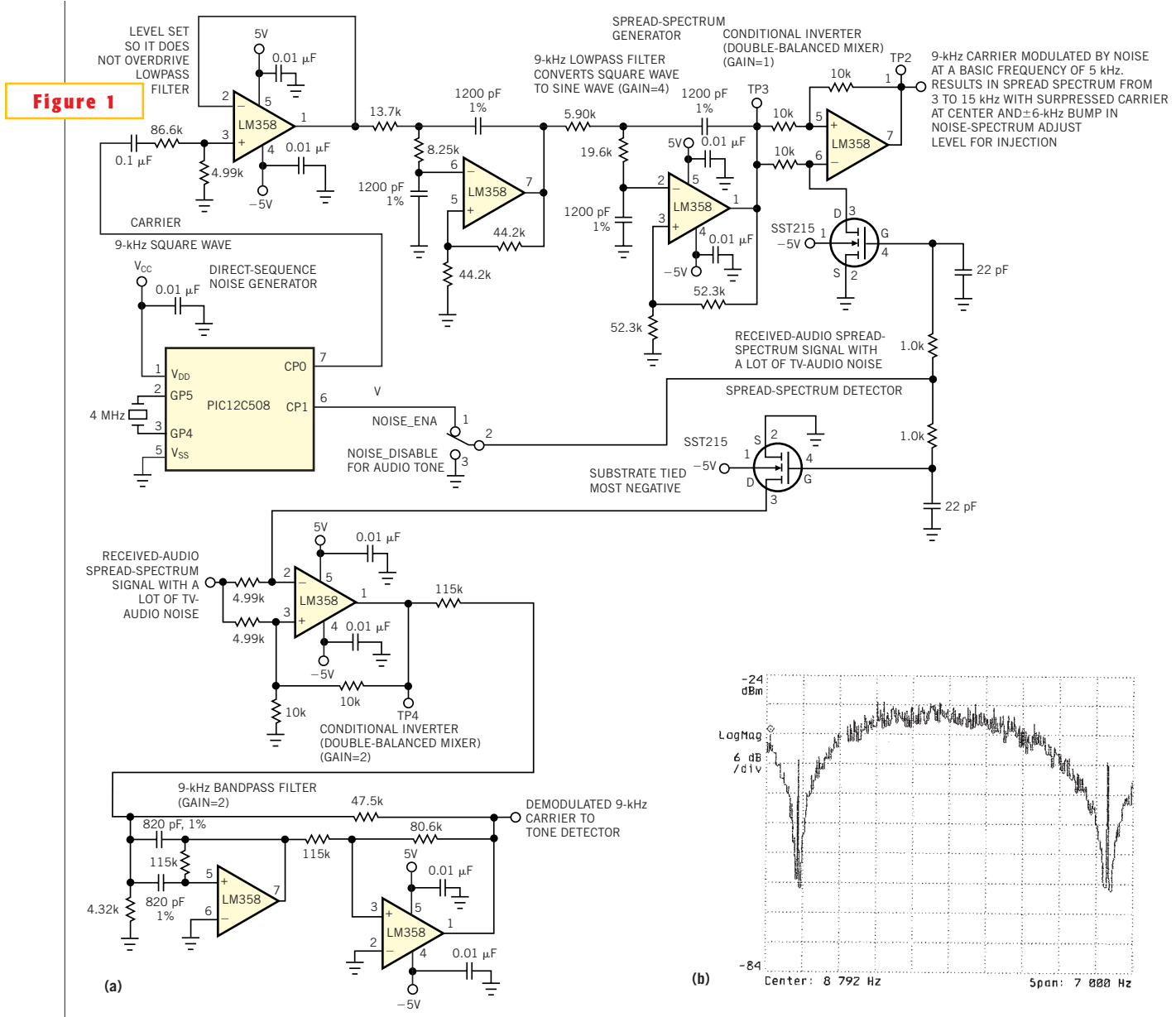
**A**N UNUSUAL METHOD of audio spread spectrum can identify the audio path that's currently in use through a consumer-electronic device. The design in **Figure 1a** uses an injected audio spread-spectrum tag signal because a listener does not notice the low-level noise in the audio bandpass, whereas the listener would hear a steady-tone tag signal. The design injects the tag into the vari-

ous inputs of the possible paths and detects the tag at the output, or speaker.

A direct-sequence noise generator running at 6 kHz furnishes the local oscillator, and a 9-kHz square-wave, low-pass filter that is filtered for its fundamental furnishes the sine-wave carrier. The circuit derives both of these signals from an 18-kHz clock. A PIC12C508A, running at 4 MHz, generates the local os-

illator and the carrier. You can download the firmware from *EDN's* Web site, [www.ednmag.com](http://www.ednmag.com). Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2513.

The local oscillator appears as  $\sin x/x$  noise in the frequency domain, which the circuit then mixes with a clean, 9-kHz audio sine wave in a double-balanced mix-



An audio-path identifier (a) injects an audio spread-spectrum tag signal (b).

er (DBM). Transformer and diode DBMs are unsuitable for the audio range. This circuit's DBM is simply an analog conditional complementor, and the local oscillator flips the output. The output of the DBM is a suppressed-carrier, double-sideband amplitude-modulated audio signal. The circuit bandpass-filters this output to 3 to 15 kHz to bandlimit the audio spread-spectrum signal (**Figure 1b**). Most of the audio "talk power" is lower than 3 kHz. The circuit then sets the level and buffers the output, which is the inject-tag signal. Note that, if the local-oscillator input to the DBMs is held either high or low, the DBMs become

simple amplifiers and the tag signal is simply a 9-kHz tone.

Detection of a direct-sequence spread spectrum requires knowing that the signal, which sounds like noise, is present and that a synchronized-sequence local oscillator that's identical to the modulator side is present and requires a synchronized-sequence local oscillator that's identical to the modulator to demodulate the signal. In this case, the modulator and demodulator are in the same box, so the circuit knows when the signal is being generated, and it uses the same direct-sequence noise generator for both the injector and the detector. Thus, you elimi-

nate the two biggest problems with spread spectrum.

The detector uses the same type of local oscillator and DBM, an analog conditional complementor, as does the injector. The detector then narrowly bandpass-filters the demodulated signal at the frequency of the modulated tag signal, or 9 kHz. This scheme separates the tag signal from the much louder audio. The audio has sporadic components in this narrow bandpass, so averaging is necessary to verify that the tag signal is present. (DI #2513)

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## 5-to-1.8V converter works without magnetics

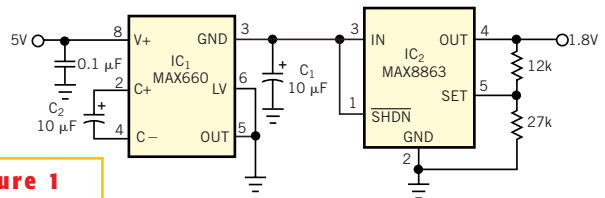
Dan Christman, Maxim Integrated Products, Sunnyvale, CA

**T**O DERIVE 1.8V FROM 5V, you might think of using a switch-mode regulator. Switchers are highly efficient but also complicated and expensive. Linear regulators, too, are out of the question unless your design can tolerate 40% efficiencies. The circuit in **Figure 1**, on the other hand, is more than 70% efficient (**Figure 2a**), sources as much as 100 mA, costs less than a switch-mode regulator, and requires less space.

IC<sub>1</sub> is a CMOS charge-pump voltage converter that the circuit configures as a voltage inverter. With its output grounded and 5V at its V+ pin, IC<sub>1</sub> generates

V+ / 2, or approximately 2.5V at Pin 3. This nominal 2.5V output, which sags as the device sources current, drives linear-regulator IC<sub>2</sub>, which regulates the 2.5V input to 1.8V. IC<sub>2</sub> is can source 100 mA

before its sagging input voltage falls below the dropout level (**Figure 2b**). Using larger values for C<sub>1</sub> and C<sub>2</sub> enables IC<sub>1</sub> to maintain its output voltage with heavier



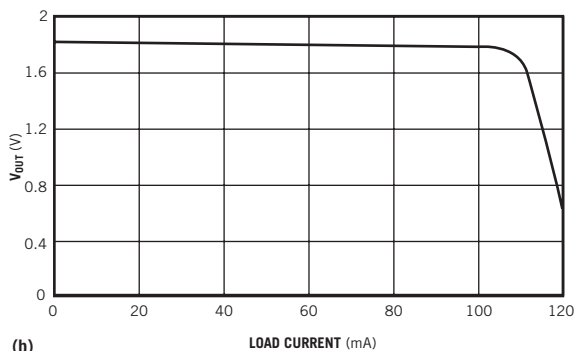
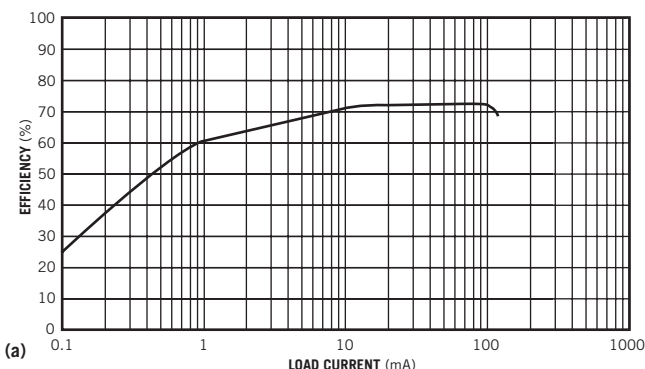
**Figure 1**

A 5-to-1.8V converter uses a charge-pump IC to lower the input voltage and then uses a linear regulator to achieve the desired output level.

load currents. (DI #2511)

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**Figure 2**



The circuit provides maximum efficiency for load currents of 10 to 100 mA (a) and maintains its output level for load currents as high as 100 mA (b).

# Band-reject filter includes compensation

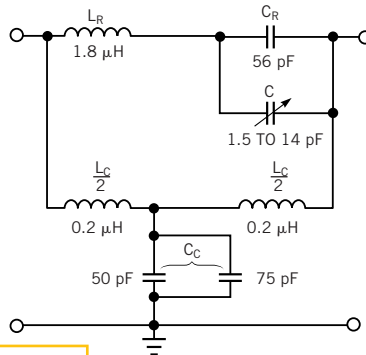
Richard M Kurzrok, RMK Consultants, Queens Village, NY

**S**OME BAND-REJECT LC filters employ a reactance to decouple individual resonators. One such filter uses relatively small shunt inductors to decouple series resonators, known as a top-L coupling. This type of coupling readily achieves narrow filter bandwidths while degrading amplitude response symmetry about the frequency of peak rejection.

Filter peak rejection occurs at a transmission pole that the shunt resonance of the coupling inductor and the effective capacitance (below resonance) of the series resonator create. A transmission zero occurs on the filter's high-frequency skirt due to series resonance. **Table 1** shows the amplitude response data of an uncompensated single-resonator band-reject filter with a center, or peak-rejection, frequency, of 14 MHz, a nominal 3-dB bandwidth of 1 MHz, and a 50Ω source/load impedance. The data in the **table** reveals appreciable asymmetry.

You can add compensation to the band-reject filter by connecting a grounded shunt capacitor to the midpoint of the coupling inductance, which this circuit realizes using two toroidal inductors in series (**Figure 1**). The measured 3-dB bandwidth of 0.9 MHz demonstrates good symmetry about the 14-MHz center frequency. Peak rejection of 21.4 dB corresponds to effective resonator unloaded Q of approximately 180. **Table 2** shows the measured amplitude response for the compensated one-pole band-reject filter.

The compensating capacitor and the bisected coupling inductor form a tee section. This section is a three-pole low-pass filter with 0.01-dB of passband ripple and a 3-dB cutoff frequency of 47 MHz, which provides supplementary lowpass selectivity superimposed upon the basic band-reject behavior. For multisection band-reject filters using artificial quarter-wave connecting lines, additional lowpass selectivity is available (**Reference 1**). Also note that the compensated top-L coupled band-reject filter is the LC counterpart of microwave



**Figure 1**

**A compensated one-pole band-reject filter connects a grounded shunt capacitor to the midpoint of the coupling inductance.**

band-reject filters. (**Reference 2**).

You can avoid the need for compensation by tapping down on shunt resonators connected in series. This technique is useful for band-reject filters that use low-frequency pot-core inductors with many turns. The technique is unattractive for band-reject filters at higher frequencies

**TABLE 1—UNCOMPENSATED AMPLITUDE RESPONSE**

Frequency (MHz)	Insertion loss (dB)
11	0.6
11.5	0.7
12	0.9
12.5	1.2
12.8	1.6
13.1	2.2
13.4	4.0
13.7	6.3
14	21.8 (peak)
14.3	4.4
14.6	1.2
14.9	0.4
15.2	0.2
15.5	0.1
15.8	0.1
16.5	0.2
17	0.2
17.5	0.3
18	0.4
19	0.5
20	0.6
25	1.0

using toroidal inductors with few turns. The compensated LC band-reject filter (**Figure 1**) is practical and provides substantial partial correction of filter-response-shape symmetry and can provide additional lowpass filtering. (DI #2514)

## REFERENCES

1. Kurzrok, R, M, "Band reject filter provides supplementary low pass filtering", *RF Design*, October 1999, pg 54, plus errata, November 1999 , pg 16.
2. Kurzrok, R, M "Trimming improves response of waveguide band-reject filter", *Electronic Design*, Nov 8, 1967, pg 116.

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**TABLE 2—COMPENSATED AMPLITUDE RESPONSE**

Frequency (MHz)	Insertion loss (dB)
11	0.15
11.5	0.2
12	0.2
12.5	0.4
12.8	0.6
13.1	0.9
13.4	1.9
13.56	3.0
13.7	3.9
14	21.4 (peak)
14.3	5.6
14.46	3.0
14.6	2.1
14.9	1.1
15.2	0.75
15.5	0.5
15.8	0.3
16.5	0.2
17	0.2
18	0.15
19	0.15
20	0.1
25	0.25
30	0.55
35	1.3
40	3.1
45	5
50	7.2
60	14.2



# Low-cost active load draws constant battery power

Doug Farrar, Los Altos, CA

**U**NLIKE NICKEL-METAL-HYDRIDE and lithium-ion rechargeable batteries, the discharge voltage of alkaline batteries is not constant and tends to vary from 1.5 to 0.8V per cell. Alkaline-battery manufacturers specify the discharge life of their batteries under constant *power* loads. Because of the varying discharge voltage, you can't simply connect a load resistor to the cells to verify or measure power profiles without incurring a lot of error in your measurements. The circuit in **Figure 1** draws a constant power from the battery pack. Thus, as the battery voltage decreases, the load current increases. A single potentiometer allows a user to set the desired wattage draw. The

circuit is simple and inexpensive to build. The heart of the load is an analog multiplier/divider circuit based on a cheap transistor array, IC<sub>1</sub>. The five transistors have closely matching V<sub>BE</sub>'s, which is crucial to the accuracy of the circuit. The circuit does not use the one transistor, Q<sub>1E</sub>, whose emitter ties to the chip's substrate. The circuit applies the battery voltage between V<sub>1</sub> and circuit ground. Op amp IC<sub>2A</sub> forces current I<sub>1</sub> to flow through R<sub>1</sub>; thus, I<sub>1</sub> = V<sub>BATTERY</sub>/R<sub>1</sub>. Likewise, current I<sub>2</sub> flows through R<sub>2</sub> and is equal to V<sub>2</sub>/R<sub>2</sub>. The setting of potentiometer R<sub>SET</sub> determines I<sub>2</sub>, Q<sub>1A</sub> and Q<sub>1B</sub>, which the circuit wires as diodes, are within the feedback paths of the op amps, so their currents

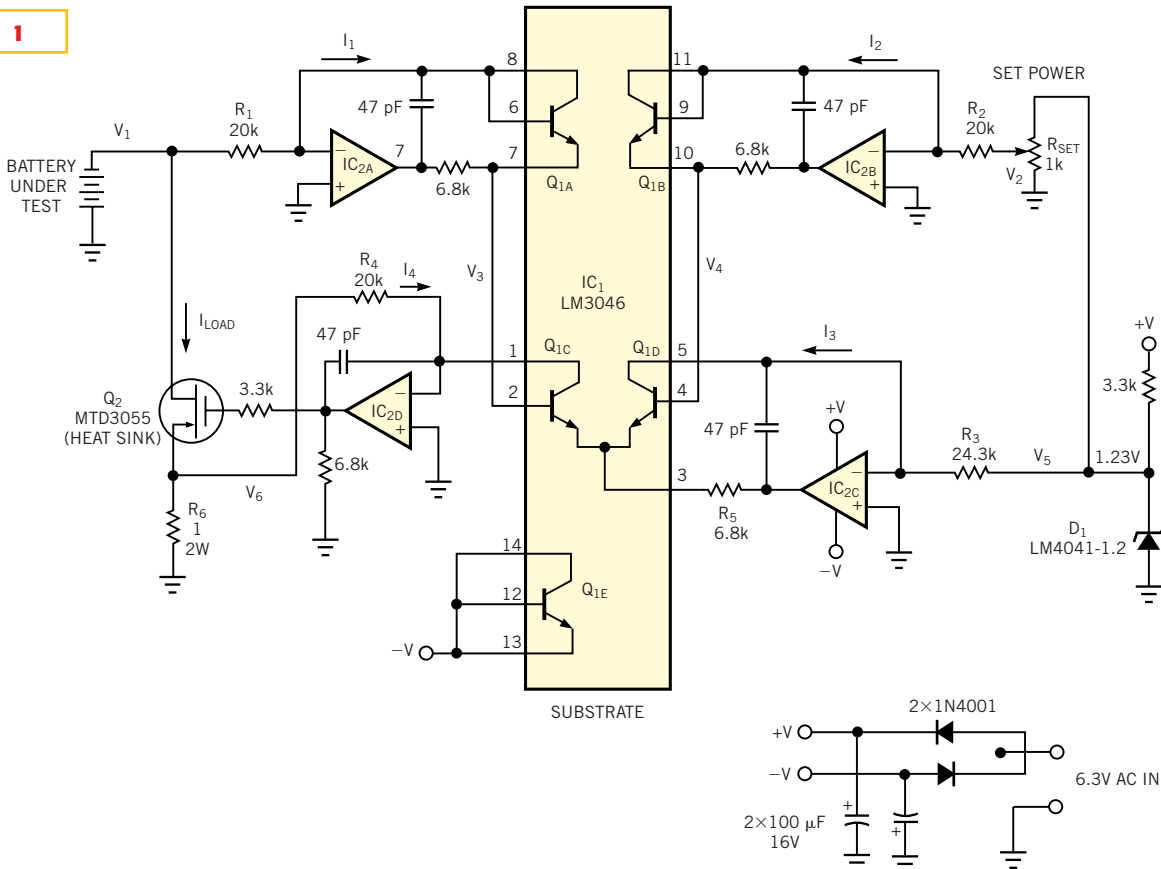
equal I<sub>1</sub> and I<sub>2</sub>, respectively. Because of the logarithmic nature of V<sub>BE</sub>'s, the voltage difference between the two diodes is as follows:

$$V_{Q1A} - V_{Q1B} = 0.026 \times \ln\left(\frac{I_2}{I_1}\right) = V_4 - V_3.$$

The circuit applies this voltage differential to the bases of Q<sub>1C</sub> and Q<sub>1D</sub>. Because all four transistors closely match one another, the ratio of currents I<sub>3</sub>/I<sub>4</sub> equal the ratio I<sub>2</sub>/I<sub>1</sub>, or

$$0.026 \times \ln\left(\frac{I_2}{I_1}\right) = 0.026 \times \ln\left(\frac{I_3}{I_4}\right).$$

**Figure 1**



**This active-load draws constant power; load current is inversely proportional to the applied voltage.**

$I_3$ , like  $I_1$  and  $I_2$ , is set by an op-amp feedback network:  $I_3 = V_3/R_3$ . Because  $I_3$  must flow through  $Q_{1D}$ ,  $IC_{2C}$  will supply enough current to the differential pair  $Q_{1C}/Q_{1D}$  to force  $I_4 = V_6/R_5$ .  $IC_{2D}$  will then force its output voltage, which drives current sink  $Q_2$ , such that  $V_6$  equals  $I_4 \times R_4$ . All you need to do now if finish the math:

$$\frac{I_2}{I_1} = \frac{V_1}{R_1} \div \frac{V_2}{R_2} = \frac{I_3}{I_4} = \frac{V_3}{R_3} \div \frac{V_6}{R_4}$$

or

$$V_6 = (V_3 \times V_2) \div V_1 \times \frac{R_1}{R_2} \times \frac{R_4}{R_3}$$

Note that the circuit forces  $V_6$  across the current-setting resistor,  $R_6$ , so that the current forced through transistor  $Q_2$  is  $I_{LOAD} = V_6/R_6$ . Thus,

$$I_{LOAD} = (V_3 \times V_2) \div V_1 \times \left( \frac{R_1}{R_2} \right) \times \left( \frac{R_4}{R_3} \right) \div R_6$$

The load current is inversely proportional to the applied battery voltage, which is precisely what you want.  $V_2$  and  $V_3$  are scaling voltages, allowing you to trim the current source value. In this case, the reference diode,  $D_1$ , sets  $V_3$  at 1.225V, and a potentiometer sets  $V_2$ . The resistor ratios in **Figure 1** allow DMM measurements of  $V_2$  to correspond to a power-dissipation level of  $1W = 1W$  from a four-cell battery pack. You should try to keep  $I_1$  through  $I_4$  at 10 to 500  $\mu A$  for best linearity. Using an op amp with a lower input offset voltage also helps improve accuracy.

$R_1$  draws a small amount of power from the battery as well, adding to the preceding equation. However, this error term is small, and you can ignore it. The current-source bias voltage, namely the load current times the sum of  $R_6$  and  $Q_2$ 's on-resistance, or  $R_{FET}$ , limits the minimum battery voltage. Doing the math, you'll find that  $V_{IN(MIN)} = \sqrt{V_2 \times (R_6 + R_{FET})}$ , where  $V_2$  is the desired power draw.

A small power supply that outputs approximately 6.3V ac powers the circuit. Two 1N4001 diodes half-wave-rectify the positive and negative voltages, and two 100- $\mu F$  capacitors provide filtering. The extremely light load of the circuit means that postfilter regulation is unnecessary. If portability is necessary, you could power the circuit from a pair of series-wired 9V batteries. You can also use asymmetrical power supplies, but you need a positive voltage of around 8V to allow  $Q_2$  to turn fully on. If you substitute a different op amp, make sure that it can withstand the power-supply voltages.  $Q_2$  dissipates most of the power, so it needs an attached heat sink. (DI #2512)

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