

# design ideas

Edited by Bill Travis and Anne Watson Swager

## Cheap pushbutton replaces rotary switch

Abel Raynus, Armatron International Inc, Melrose, MA

**T**HE PROBLEM OF SETTING any one of four modes of a  $\mu$ C-operated process has a straightforward solution: Have the  $\mu$ C check the states of some 4 bits of a  $\mu$ C register or an input port and then execute one of the four predetermined subroutines according to the result. The next question is how the operator sets these 4 bits or, specifically, selects a desirable mode of operation.

One approach is to use a rotary switch (Figure 1a). This circuit does the job but is rather expensive for consumer applications. You can also reject DIP switches because even a qualified person can choose a wrong setting when using this solution. Slide switches are another possibility, but those in the catalogs have no more than three positions (SP3T), and this application requires four.

Figure 1b shows a simple and cost-effective solution that uses one pushbutton switch and four LEDs for mode indication. (You can download the corresponding  $\mu$ C program from EDN's Web site, [www.ednmag.com](http://www.ednmag.com).

Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2605.)

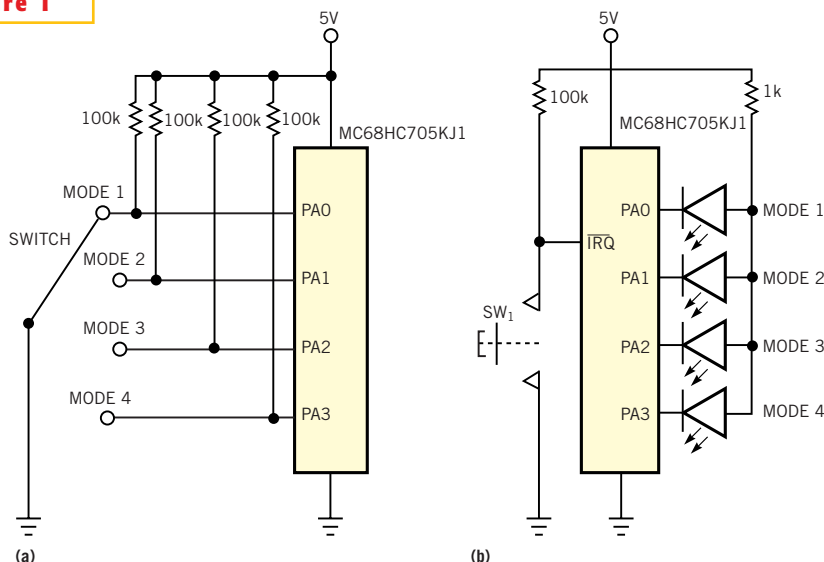
The four  $\mu$ C bits PA0 through PA3 serve as a mode register and simultaneously as a mode indicator via the LEDs. After the  $\mu$ C resets, the initialization routine puts a low level on PA0, which sets MODE 1 and lights the corresponding LED. All other LEDs remain off, and all the rest of the bits of Port A stay unchanged. For the intended project application, it is more convenient to organize the mode-switching process as an external interrupt and let the main program perform its other functions. When an operator pushes the normally open switch, SW<sub>1</sub>, the resulting negative edge at the IRQ pin of the  $\mu$ C causes an external in-

terrupt. The interrupt-service routine shifts the low level to the next output pin consecutively from PA0 to PA3. When the routine reaches PA3, it goes back to PA0, and so on. The service routine has no effect on bits PA4 through PA7, and they remain unchanged. The debouncing delay is 54 msec.

The circuit in Figure 1 uses an inexpensive  $\mu$ C, but the program contains the standard instruction set and therefore is applicable to any  $\mu$ C.

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Figure 1



As an alternative to a rotary switch (a), you can use a pushbutton switch (b) to cycle through four modes of a  $\mu$ C-controlled process. Four LEDs indicate the selected mode.

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# FPGA makes simple FIFO

Luis Miguel Brugolaras, SIRE, Madrid, Spain

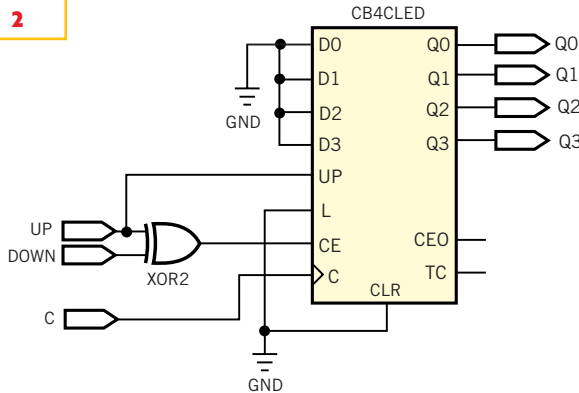
**T**HE CIRCUIT IN **Figure 1** is an FPGA-based, synchronous FIFO that uses the same clock for read and write operations. The circuit can generate FIFO-occupancy flags with a minimum of logic. The boxed area in **Figure 1** shows a more conventional occupancy meter. The circuit is implemented in a demultiplexer that writes data in the FIFO when the data arrives and reads data according to FIFO occupancy. The circuit uses a Xilinx Spartan (XC4000 equivalent) FPGA.

The method uses three main blocks: a 16-bit deep but can be as great as 16 bits deep using the RAM16X1D macro. Read and write counters can take the form of any cyclic counter, a conventional binary

counter, a Gray-code counter, or a linear-feedback shift register. FIFOs commonly use Gray-code counters. These counters have the property that only one bit changes from state to state. Thus, they have the advantage of not providing intermediate false states when the counter advances. For example, a binary counter moving from 0111 to 1000 changes all its bits but with different delays and thus can fool asynchronous comparison logic. Linear-feedback shift registers have the advantage of requiring modest

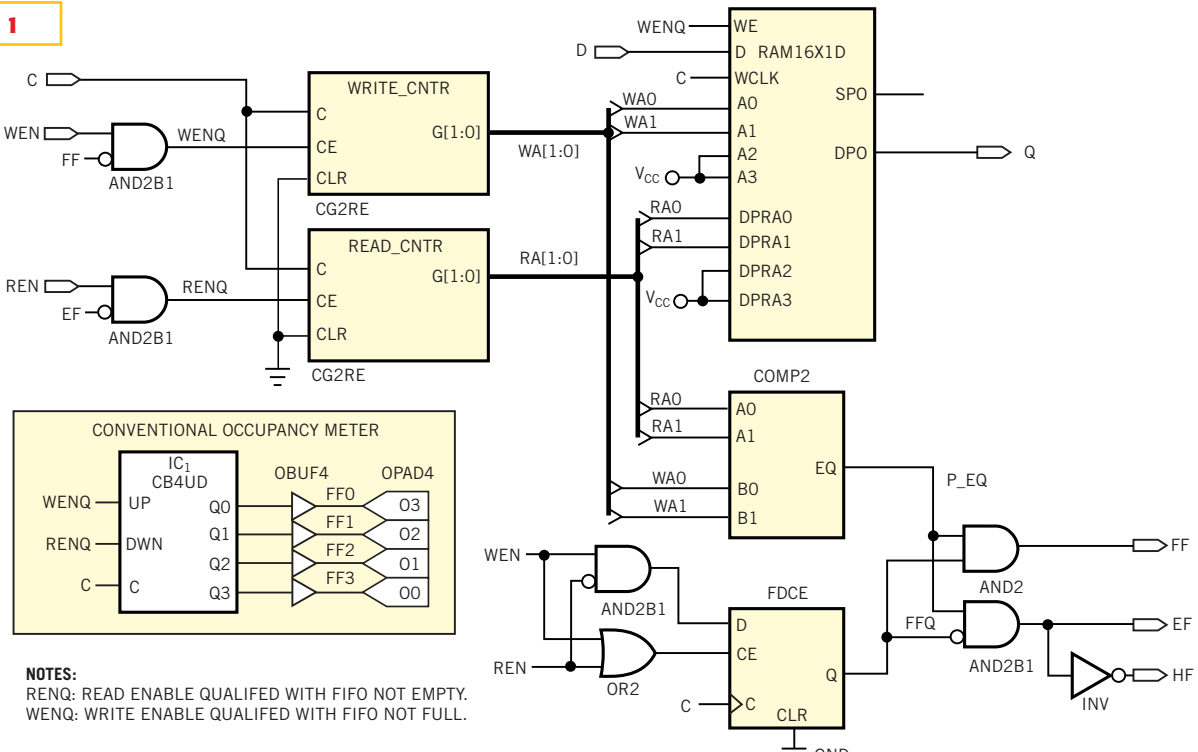
logic resources and can work at high clock rates. They pose one small inconvenience, however: For an n-stage shift register, only  $2^n - 1$  states exist.

**Figure 2**



**The CB4CLED increments upon assertion of UP and CE and decrements upon assertion of CE and deassertion of UP.**

**Figure 1**



**NOTES:**  
 RENQ: READ ENABLE QUALIFIED WITH FIFO NOT EMPTY.  
 WENQ: WRITE ENABLE QUALIFIED WITH FIFO NOT FULL.

**This simple scheme makes it easy to determine FIFO occupancy.**

You can read FIFO occupancy in an orthodox way, by using an up/down counter controlled by read- and write-enabled clocks (**Figure 2**). This method makes the counter advance up when the FIFO is written to but not read, advance down when the FIFO is read but not written to, and remain unchanged otherwise. Such an arrangement leads to full knowledge of FIFO occupancy, a valuable asset during debugging. For example, you can use a DAC to convert the occupancy data and monitor it with an oscil-

loscope. In this application (**Figure 1**), it was necessary to keep logic to a minimum. We simply needed to know whether the FIFO was full (to avoid loss of data in a write attempt), or empty; hence, the application needed just Full and Empty flags. The addresses of the read and write pointers are equal only when the FIFO is either full or empty. These states are distinguishable because, before the FIFO became full, a write operation occurred after no previous read operation. A flip-flop qualifies this status

by latching data only when a read or write attempt occurs. The flip-flop latches a high level when a write operation (but not a read operation) occurs, indicating an attempt to increment the FIFO's occupancy.

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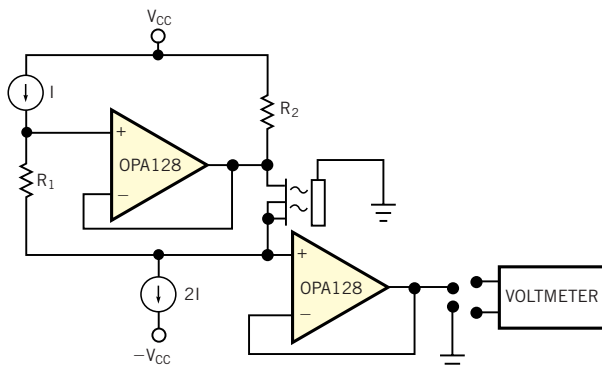
## Circuit provides constant current for ISFETs/MEMFETs

*S Casans, D Ramirez, and AE Navarro, University of Valencia, Burjassot, Spain*

ISFETs AND MEMFETs (ion-sensitive and membrane FETs) are solid-state chemical sensors that provide an electrical signal associated with the change of a chemical concentration in a solution. These types of sensors need a stable operating point. A common operating point is a drain-source current of 100  $\mu\text{A}$  and a drain-source voltage of 500 mV. Under these conditions, the sensed chemical information is contained in the gate-source voltage. **Figure 1** shows a constant-current driver for ISFETs/MEMFETs. The current source,  $I$ , produces a voltage drop in resistor  $R_1$ ; the voltage follower reflects this voltage to the drain-source terminals of the chemical sensor. In this example,  $V_{DS}$  is equal to  $IR$ . The entire current,  $I$ , traverses resistor  $R_1$ , because the op amp is an electrometer type with femtoamp-range input-bias current. The sensor's drain-source current is the difference between the constant currents,  $2I$  and  $I$ —in this case,  $I$ . A REF200 provides the constant currents in the circuit in **Figure 1**. The REF200 has two internal 100- $\mu\text{A}$  current sources and a current mirror.

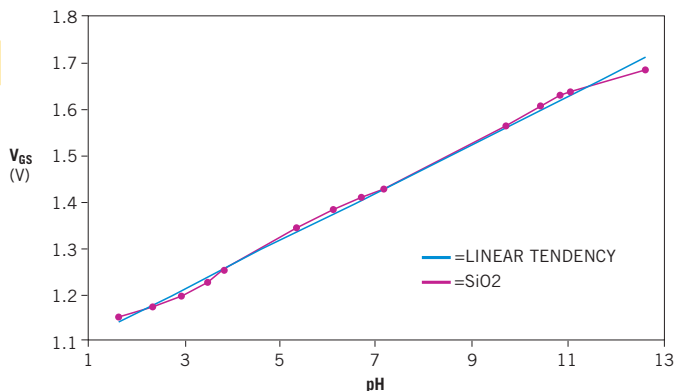
One of the 100- $\mu\text{A}$  current sources provides  $I$  in **Figure 1**. The lower  $2I$  current source uses the REF200's second

**Figure 1**



**A constant-current driver provides the basis for a chemical-concentration test system.**

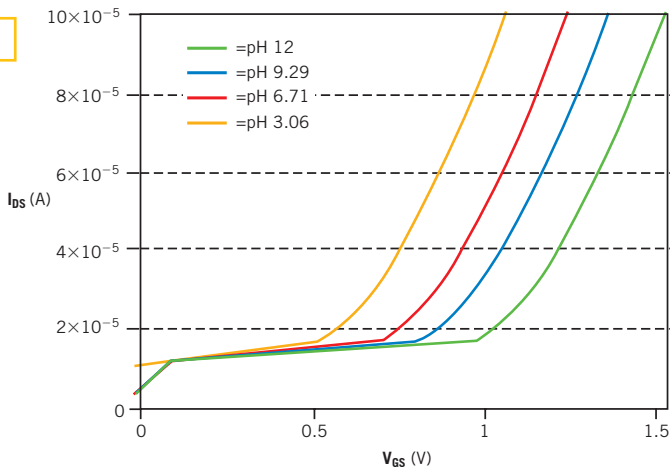
**Figure 2**



**The gate-source voltage shows good correlation with the concentration of [H<sup>+</sup>] ions.**

100- $\mu$ A current source and the internal current mirror. The second voltage follower measures the gate-source voltage of the sensor—hence, the chemical concentration of interest. **Figure 2** shows experimental results. You can see that the setup provides a linear relationship between gate-source voltage and the concentration of  $[H^+]$  ions. The experiment used  $SiO_2$ - and  $Si_3N_4$ -based IS-FET sensors. **Figure 3** shows the variation of the threshold voltage as a function of pH.

**Figure 3**



The gate-source voltage of an ISFET shifts with the degree of acidity.

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## USB link neatly measures temperature

Mary Burke, Analog Devices, Limerick, Ireland

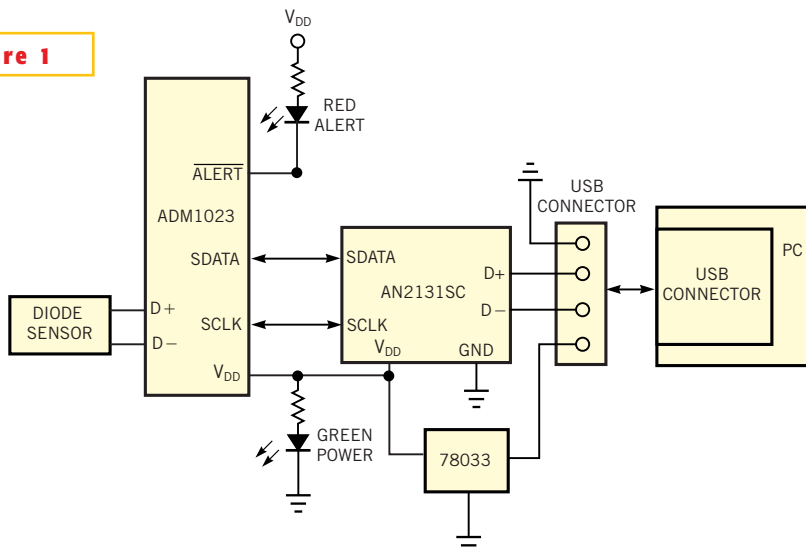
**FIGURE 1** SHOWS A convenient and neat way to measure temperature using the USB of a PC. An ADM-1023 IC senses the temperature, and an Anchor Chips EZ-USB AN2131SC  $\mu$ C provides control. The ADM1023 is a low-cost device with an accuracy of  $1^\circ C$  and a resolution of  $0.125^\circ C$ . The IC is a two-channel device that can measure its own local temperature and the temperature of a remote location. You obtain remote-temperature sensing by connecting a remote thermal diode between the D+ and D- pins of the  $\mu$ C. You can locate this remote diode (for example, a diode-connected 2N3906) in a hot spot that can be as far as 100 ft from the ADM1023. However, for distances greater than 12 in., you should use twisted-pair cable. For distances greater than 12 ft, you should use shielded twisted-pair cable, such as microphone cable.

The EZ-USB  $\mu$ C includes an integrated I<sup>2</sup>C controller. This feature is useful in that the  $\mu$ C communicates via I<sup>2</sup>C, thereby simplifying both the circuit and the  $\mu$ C's firmware. The  $\mu$ C takes care of the

lower level PC signals. The firmware needs only to place the data destined for the I<sup>2</sup>C data register and to tell the  $\mu$ C to send it. A second advantage of this  $\mu$ C is the availability of on-chip RAM. You can

write Windows drivers such that the firmware automatically downloads to the RAM when you plug in the board. The  $\mu$ C then simulates a disconnect and re-connects the board as a new device. This

**Figure 1**



Use the USB port on your PC to make quick and easy temperature measurements.

feature of the  $\mu\text{C}$  is called reenumeration. The circuit in **Figure 2** works as follows: The SDA and SCLK pins of the ADM1023 connect to the corresponding pins of the  $\mu\text{C}$ . You need a 2.2-k $\Omega$  pullup resistor on both lines, because these pins have open-drain outputs. Also connected to these lines is a 24LC00, a 16-byte EEPROM. This ROM stores the board's device descriptors (the vendor and product IDs). Windows uses this information to identify which device driver to use.

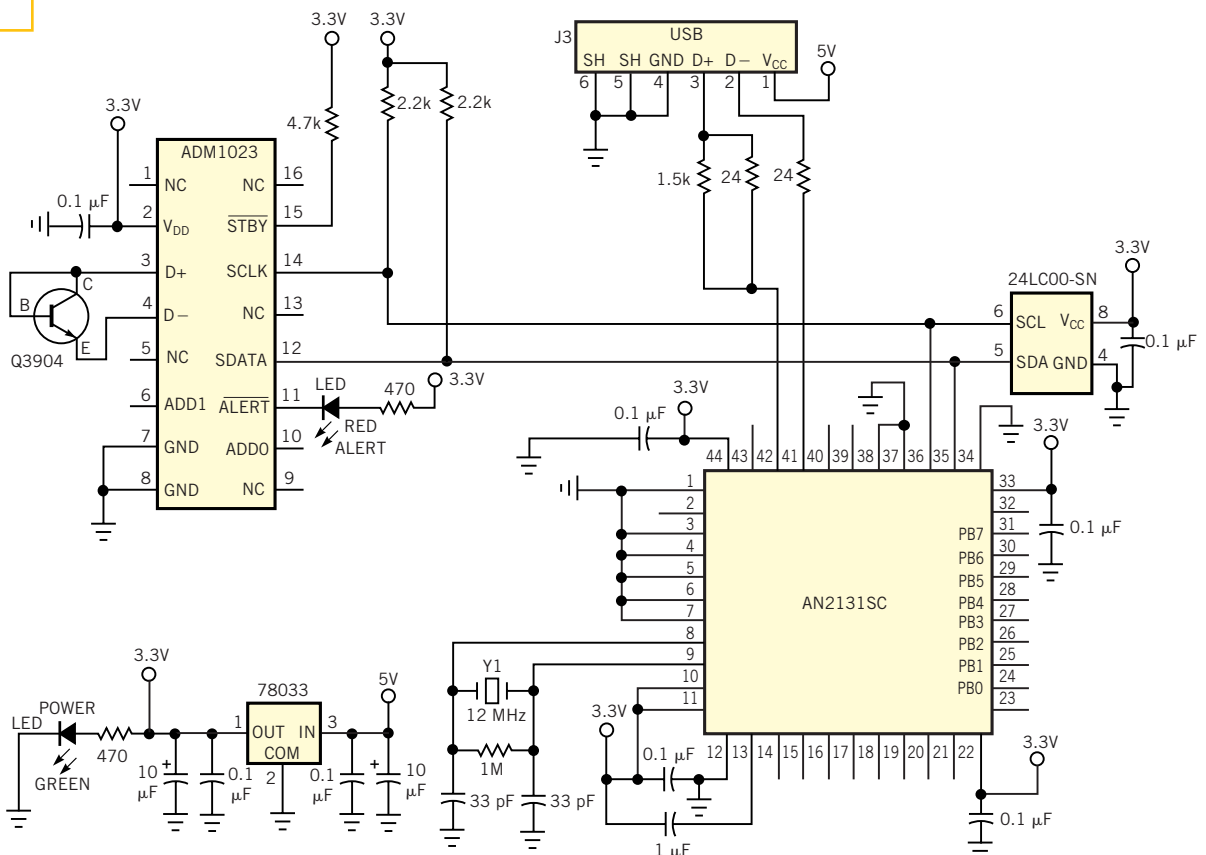
The remote thermal diode (or diode-connected transistor) connects between the D+ and D- lines of the ADM1023. The ADM1023 can also signal an Alert. You can program the IC with high and low temperature limits for both the local and the remote channels. If any of the

measured values of temperature are beyond the temperature limits, then the ADM1023 signals an Alert. The ALERT is active-low; an LED tied to the pin lights whenever an Alert signal arises. The USB port supplies power to the circuit. The port can supply as much as 500 mA at 5V. Because both chips in **Figure 2** operate at 3.3V, the circuit uses a 78033 regulator to generate the required 3.3V. The USB Master, which in this case is the application running on the PC, maintains control of the circuit. The master initiates all USB communications. The temperature-measurement circuit is the slave. It responds only when the master requests it to do so. When the master requests data (via the PC application), the request travels down the USB cable to the  $\mu\text{C}$ . This

request consists of the device address of the ADM1023 and the address of the register that stores the data. It also tells the  $\mu\text{C}$  whether a read or a write is required. The  $\mu\text{C}$  then uses this information to interrogate the ADM1023 over the I<sup>2</sup>C interface. You can download the software used in this project from EDN's Web site. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2596.

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**Figure 2**



This temperature-measurement system requires minimal components.

# Single-sideband demodulator covers the HF band

Israel Schleicher, Bakersfield, CA

**T**HE CIRCUIT IN **Figure 1** complements a previous Design Idea (“SSB modulator covers HF band,” *EDN*, Sept 30, 1999, pg 122). The modulator employs a phasing network to split a low-frequency audio signal into in-phase and quadrature (orthogonal) components. This circuit delivers a phase error of only 0.15° and has a low sensitivity to component tolerances, which are advantages over other phasing circuits (**Reference 1**). By reversing the direction of the network, that is, feeding the output with two orthogonal signals and tapping the input, the network functions as a detector. Feeding the two signals one way may produce a signal at the input, but if you interchange the two signals, no signal will go through.

Because the network in the modulator circuit has two floating differential outputs, the demodulator network requires two floating sources. The simplest way to accomplish this requirement is by using transformers.  $T_1$  and  $T_2$  are 600Ω 1-to-1 telephone-coupling transformers with a center-tapped bifilar primary. It is important to minimize the capacitance between the primary and the secondary windings.

$Q_1$  to  $Q_4$  and  $Q_5$  to  $Q_8$  function as balanced mixers. They provide a high dynamic range for the circuit, which is part of a direct-conversion receiver.  $IC_1$  provides two, quadrature LO signals, and this IC requires a drive of four times the carrier frequency.  $IC_2$  allows for upper or lower sideband selection. The prototype

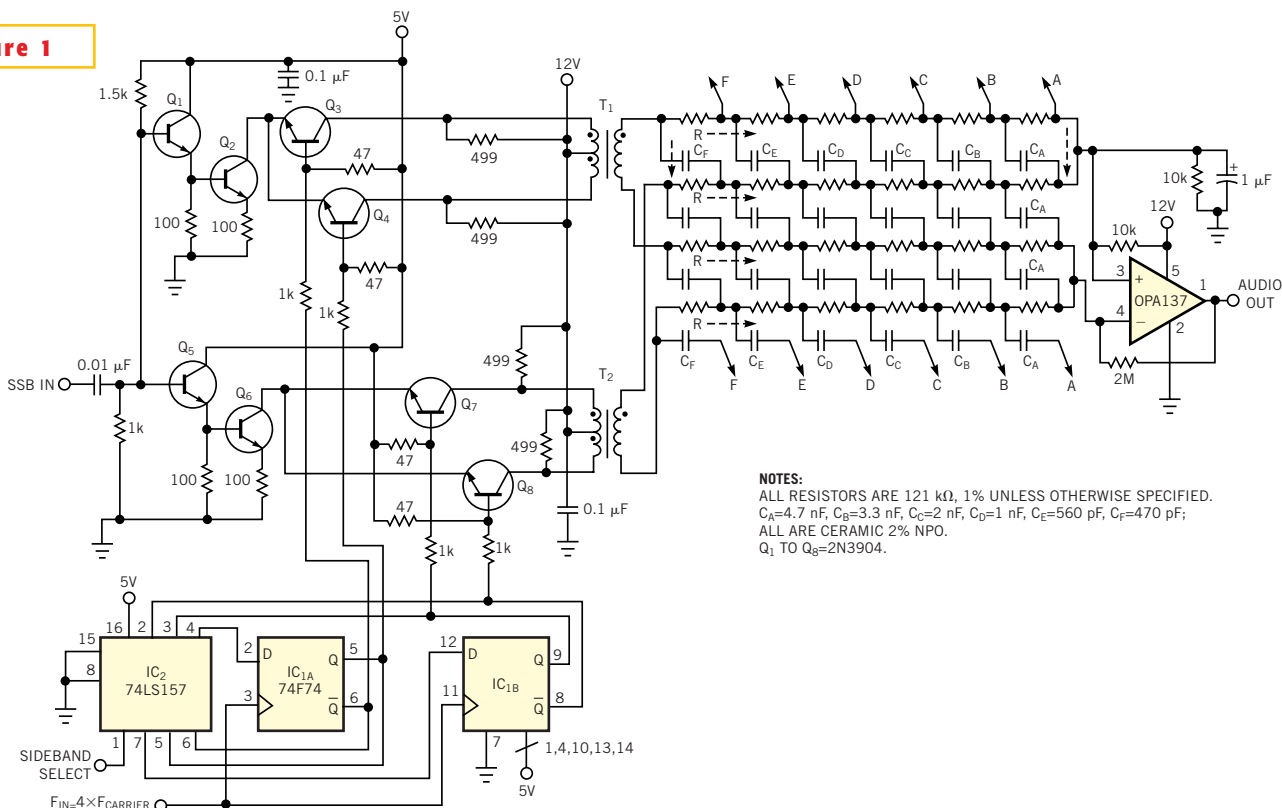
circuit measures 37 dB of unwanted sideband rejection for a 1-kHz modulated carrier and 32-dB rejection for a 3-kHz modulation. A sharp 3-kHz lowpass filter must follow the circuit.

## REFERENCE

1. Zavrell, Robert, J, “New low-power single sideband circuit,” Philips Semiconductor, AN1981.

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**Figure 1**



**NOTES:**  
 ALL RESISTORS ARE 121 kΩ, 1% UNLESS OTHERWISE SPECIFIED.  
 $C_A=4.7$  nF,  $C_B=3.3$  nF,  $C_C=2$  nF,  $C_D=1$  nF,  $C_E=560$  pF,  $C_F=470$  pF;  
 ALL ARE CERAMIC 2% NPO.  
 $Q_1$  TO  $Q_8=2N3904$ .

A single-sideband demodulator uses two transformers as floating sources.

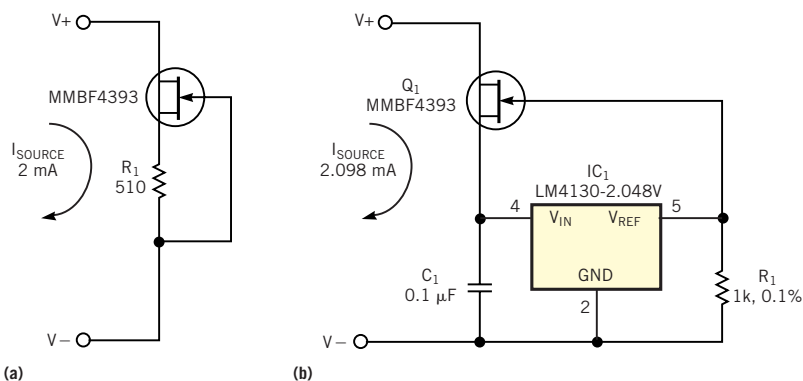
# Voltage reference improves JFET

Clayton Grantham, National Semiconductor, Tucson, AZ

**T**HE COMMON JFET current-source in **Figure 1a** has average output impedance and depends heavily on the JFET's  $V_p$  and  $I_{DSS}$  variations. These manufacturing variations limit the initial accuracy of the current setpoint that the circuit can obtain with a fixed  $R_1$ . Most users of JFET current-sources sample  $V_p$  and  $I_{DSS}$  for each lot of JFETs and then select  $R_1$  by first solving the quadratic equation  $I_D = I_{DSS}(1 - V_{GS}/V_p)^2$  for  $V_{GS}$  and then solving the current-setpoint equation  $I_{SOURCE} = V_{GS}/R_1$ . After completing these lot-specific calculations, the accuracy error for  $I_{SOURCE}$  can be less than  $\pm 15\%$ . In addition to initial accuracy error at ambient, the  $V_{GS}$  overtemperature performance limits the current temperature drift to  $0.3\%/^{\circ}\text{C}$ . The temperature dependence of  $V_{GS}$  is a function of both the mobility variation of  $I_{DSS}$  with  $I_{DSS}$  negative-temperature coefficient and the built-in potential of  $V_p$ 's positive coefficient.  $V_{GS}$  has one  $I_D$  operating point at which it has a zero temperature coefficient, but this one current setpoint is probably not the one that you wanted. With resistors commonly available at 0.1%, 25 ppm/ $^{\circ}\text{C}$  grade,  $R_1$  will be a small contributor to any errors in the current setpoint. Compliance voltage across the current source is  $V_{GS}$  to  $BV_{DSS}$ . The output impedance,  $R_O$ , for this current source is approximately  $1\text{ M}\Omega$ . You can improve  $R_O$  to approximately  $10\text{ M}\Omega$  by adding another JFET in a cascode configuration.

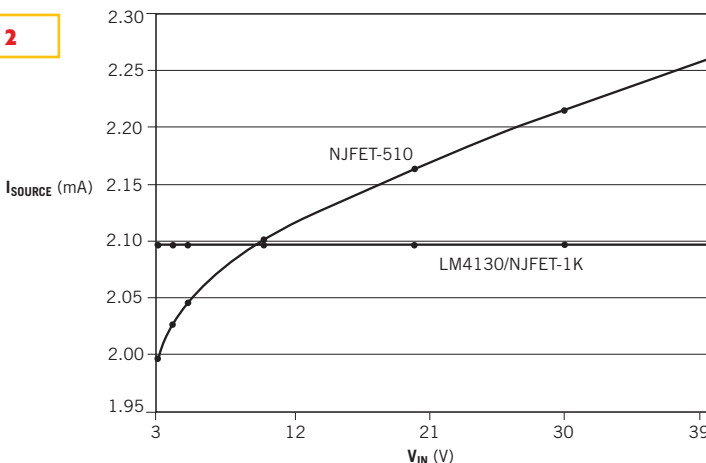
In contrast, the composite circuit in **Figure 1b** adds an IC voltage reference to the JFET that improves the output impedance.  $I_{SOURCE}$  is set by  $IC_1$ 's output voltage divided by  $R_1$  plus the small ground-current ( $50\text{ }\mu\text{A}$ ) of  $IC_1$ . The good supply rejection of the LM4130 nulls any  $V_{GS}$  variation of the JFET. The current path is from  $V+$  through the n-channel JFET (drain to source) into  $IC_1$ 's supply input and then out  $V_{REF}$  and through  $R_1$  to  $V-$ . The gate current of  $Q_1$  is in the pi-

**Figure 1**



The common JFET transistor current source (a) has an average output impedance. A composite voltage reference and JFET circuit (b) features higher output impedance, high accuracy, and low temperature drift.

**Figure 2**



The composite configuration improves the variation of  $I_{SOURCE}$  with a change in  $V_{IN}$ .

coamp range. The JFET's  $V_{GS}$ , approximately 1.2V, keeps  $IC_1$  biased well above its dropout level.

**Figure 2** shows  $I_{SOURCE}$  versus  $V_{IN}$  of both the JFET and the composite current sources. The slope of these two operating plots represents the inverse of output resistance. The JFET-only curve has an output resistance of approximately  $0.2\text{ M}\Omega$ . The composite circuit curve has an output resistance of greater than  $200\text{ M}\Omega$  as compared with the JFET-only output resistance of  $0.2\text{ M}\Omega$ .

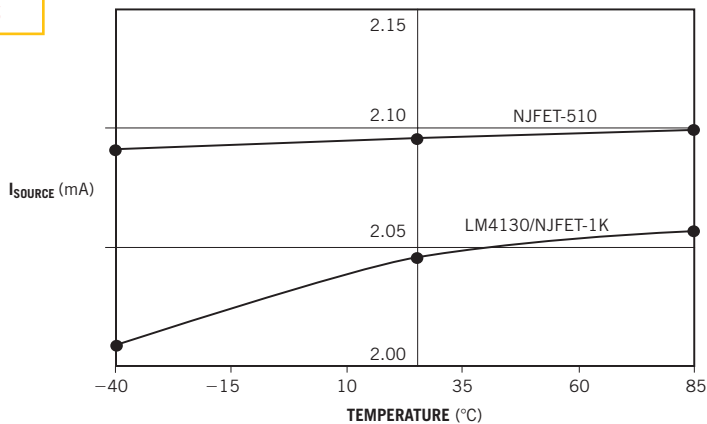
To a slighter degree than output impedance, the circuit in **Figure 1b** also improves the initial accuracy of  $I_{SOURCE}$ . The

high accuracy achievable with  $IC_1$  and  $R_1$  controls the setpoint. Both these components are available in at least 0.1% grades. However,  $IC_1$ 's ground current of  $50 \mu A$  introduces an offset to  $I_{SOURCE}$ , which you must include in the calculation.  $IC_1$ 's ground-current variation of  $\pm 7 \mu A$  is the practical limit of  $I_{SOURCE}$ 's accuracy. **Table 1** summarizes the impact on the practical accuracy that you would attain for a range of  $I_{SOURCE}$  values.

**Figure 3** compares the overtemperature performance. Again,  $IC_1$ 's ground-current variation dominates for  $I_{SOURCE}$  set below  $200 \mu A$ .  $IC_1$ 's variation of ground-current overtemperature is  $\pm 5 \mu A$ .

The compliance voltage across the composite is  $V_{GS} + 2.1V$  to  $BV_{DSS} + 5.5V$ , or approximately 3.5 to 36V. Regarding overvoltage stress, when  $V_{IN}$  goes above  $BV_{DSS} + 5.5V$ , the composite circuit's set-

**Figure 3**



The composite configuration also offers a slight improvement in the variation of  $I_{SOURCE}$  with a change in temperature.

point permanently goes into the microamp range due to the CMOS struc-

tures within the LM4130 that the overvoltage destroys. The JFET-only configuration may shift the setpoint by 20% but otherwise will be more forgiving of an overvoltage stress. You can further enhance the composite configuration by cascoding the JFET, which boosts the output resistance to approximately  $1 G\Omega$  and extends the  $V_{IN}$  range to more than 70V.

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**TABLE 1—IMPACT ON ACCURACY FOR  $I_{SOURCE}$**

$I_{SOURCE}$ (mA)	$R_2$ ( $\Omega$ )	Accuracy-error range (%)	Temperature-coefficient range (ppm/°C)
4.066	510	$\pm 0.4$	$\pm 75$
2.098	1k	$\pm 0.6$	$\pm 95$
1.074	2k	$\pm 1.0$	$\pm 135$
0.255	10k	$\pm 3.0$	$\pm 380$
0.126	27k	$\pm 6.0$	$\pm 980$

Note:  
 $R_2 = 0.1\%$ , 25 ppm/°C.

## Wideband filter uses image parameters

Richard M Kurzrok, RMK Consultants, Queens Village, NY

**Y**OU CAN DESIGN various lowpass and highpass filters using image parameters (references 1 and 2). By cascading a highpass and a lowpass filter using image-parameter designs, you can also realize a low-cost wideband filter (Figure 1). A different approach uses a composite design with terminating m-derived half-sections and two interior constant-k full sections. This approach

results in viable performance with the use of relatively few components. For this approach, however,  $m = 0.5$ , which is not the preferred value for classic-filter designs.

In Figure 1's filter, the upper and lower cutoff frequencies of this overall bandpass filter can be independent design parameters. For this filter, the nominal highpass cutoff frequency is 3.3 MHz, and the lowpass cutoff frequency is 10

MHz. Impedance levels are  $50\Omega$ . A male-to-male BNC adapter connects the two separate filter units. At higher frequencies, total integration of the two filters in a single enclosure would be desirable. Use of surface-mount components might also be appropriate.

**Table 1** shows the measured amplitude responses of the highpass and lowpass sections. **Table 2** summarizes the overall



bandpass filter's amplitude response. You can see that the highpass and low-pass cutoff frequencies are sufficiently removed from each other to realize a fairly wide passband of low insertion loss. If the cutoff frequencies of the highpass and lowpass filters are too close to each other, you can reduce interactions between the two filters by using a fixed-pass attenuator to connect the two filters.

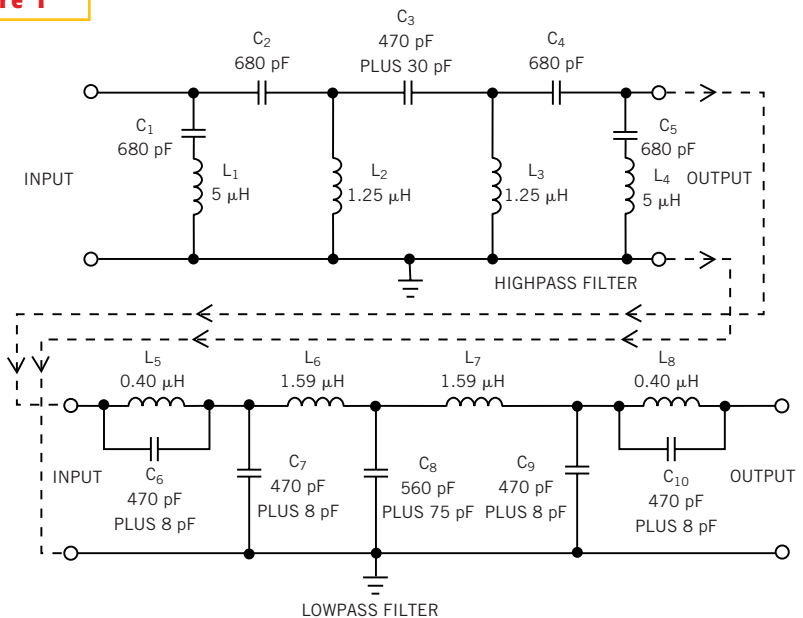
The design computations are simple, harking back to the days of slide-rule designs. You can gauge the theoretical performance of composite lowpass filters using modern computer-aided analysis (Reference 3).

REFERENCES

1. Kurzrok, Richard M, "Low cost low-pass filter design using image parameters", *Applied Microwave & Wireless*, pg 72, February 1999, plus correction pg 12, May 1999.
2. Kurzrok, Richard M, "Filter design uses image parameters", *EDN*, May 25, 2000, pg 111, May 25, 2000.
3. Kurzrok, Richard M, "Update the design of image-parameter filters", *Microwaves & RF*, pg 119, May 2000.

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Figure 1



NOTES:

- C<sub>1</sub>, C<sub>2</sub>, C<sub>4</sub>, C<sub>5</sub>=POLYPROPYLENE.
- C<sub>3</sub>: 470 pF=POLYPROPYLENE, AND 30 pF=CM-15 DIPPED MICA.
- L<sub>1</sub>, L<sub>4</sub>=MICRO METALS T37-2 32T-#26.
- L<sub>2</sub>, L<sub>3</sub>=MICRO METALS T37-2 14T-#26.
- C<sub>6</sub>, C<sub>7</sub>, C<sub>9</sub>, C<sub>10</sub>: 470 pF=POLYPROPYLENE, AND 8 pF=CERAMIC.
- C<sub>8</sub>: 470 pF=POLYPROPYLENE, AND 75 pF=CM-15 DIPPED MICA.
- L<sub>5</sub>, L<sub>8</sub>=MICRO METALS T25-6 10T-#30.
- L<sub>6</sub>, L<sub>7</sub>=MICRO METALS T25-6 23T-#30.
- ADAPTER=BNC M-M (U6-491A/U, COMMERCIAL).
- I/O CONNECTORS=BNC FEMALE.
- ENCLOSURE=ALUMINUM BOX (HAMMOND 1590A/BND CU-123).
- PC BOARD=VECTOR BOARD 169P44C1, CUT BY HAND.
- STANDOFFS=MALE, FEMALE (AMATOM 9794-SS-0440).

A low-cost wideband filter results from cascading a highpass and a lowpass filter using image-parameter designs.

TABLE 1—PARTS LIST FOR WIDEBAND FILTER

Frequency (MHz)	Highpass insertion loss (dB)	Lowpass insertion loss (dB)
2.9	23.8	Less than 0.1
3.3	9	Less than 0.1
3.4	2.5	—
3.5	1.15	—
4	0.65	0.1
5	0.3	0.1
7	0.15	0.2
9	0.1	0.55
9.5	—	1
10	—	5
11	—	23.5
12	0.1	—

TABLE 2—AMPLITUDE RESPONSE

Frequency (MHz)	Insertion loss (dB)
2.9	24.4
3.3	7.9
3.4	2.7
3.5	1.2
4	0.8
4.5	0.6
5	0.4
7	0.3
8	0.5
9	0.8
9.5	1.1
10	4.8
12	Greater than 28