

16-Bit PWM Optoisolated DAC Is PC-Controlled

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CIRCLE 520

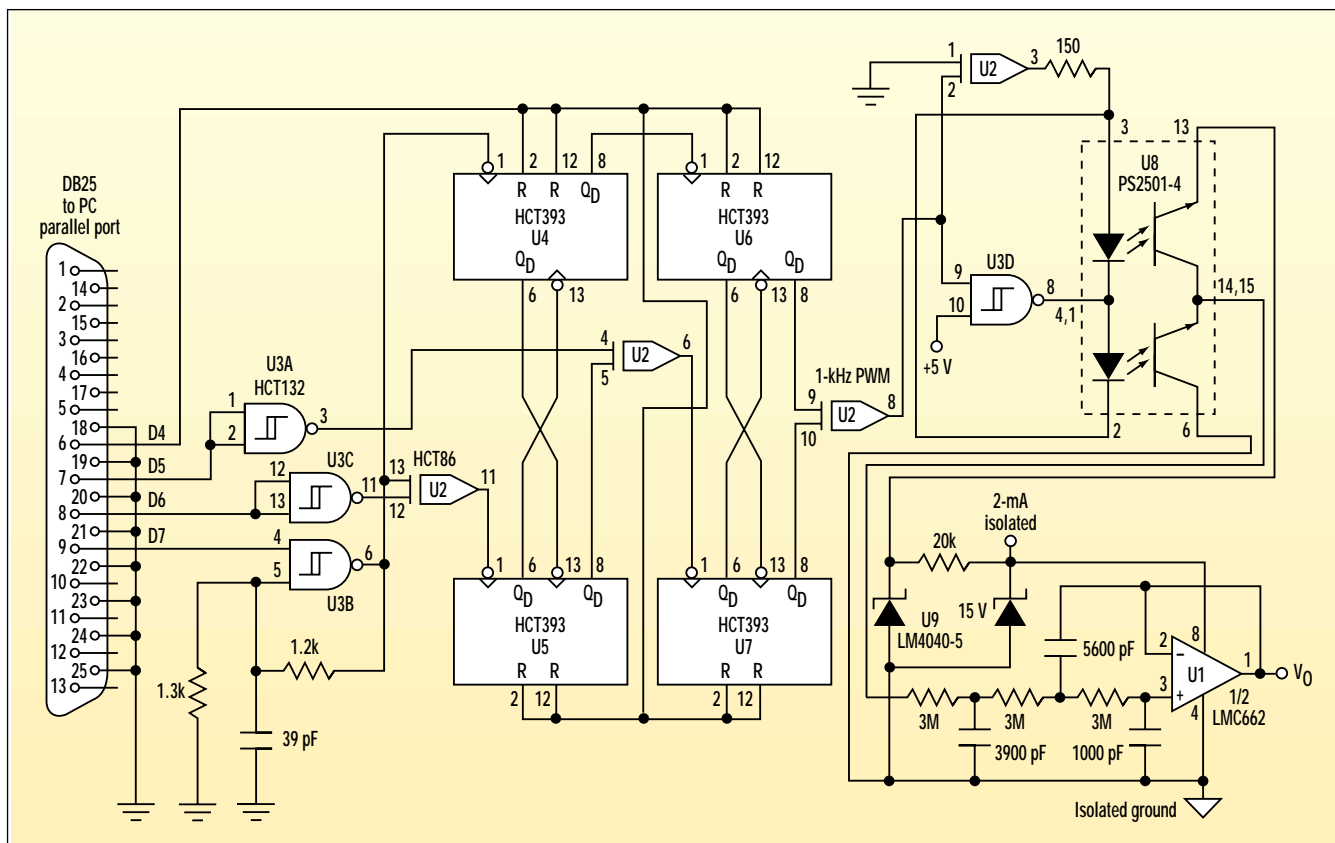
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There was a time when an “honest” (e.g., DNL < 1/2 LSB) 16-bit digital-to-analog converter (DAC) was an expensive, premium component. Nowadays they’re almost jellybeans—almost. Some applications, however, can still benefit from multichip 16-bit DAC solutions. The circuit presented here (see the figure) was designed to serve one of these applications. It features a virtually perfect DNL, which is an inherent characteristic of PWM conversion. It also includes an optoisolated output and an interface to the ubiquitous PC’s parallel (printer) port.

A general description of DAC circuit operation is as follows: control of the 16-bit PWM conversion waveform comes from the relative phase of the 500-Hz square-wave outputs of two 16-bit ripple-carry counters (comprising U4, 5, 6, and 7) free-running from a common 30-MHz RC clock (U3B). The phase is determined by the initial values loaded into the counters before the clock is enabled and the states of PC port bits D5 and D6. Depending on this phase, the duty cycle of the output of exclusive-OR U2C can be varied linearly from 0% to 100% in increments

of 0.0015% ($1/2^{16}$). The PWM waveform is then split into two complementary drive signals and applied to the anti-parallel LEDs and inverted (i.e., $V_{CE} < 0$) phototransistors of optoisolator U8.

The operation of the U8 phototransistors in inverted mode reduces their on-state saturation voltage to the sub-mV range. Thus, the dc component of the isolated square wave is accurately (to 13-bit precision) equal to the product of the PWM duty cycle and the U9 voltage reference. The dc component is extracted by the three-pole, 14-Hz, uni-



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ty-gain, low-pass filter (U1). The sub-pA bias current of U1 limits the error term arising from the net 9-M Ω filter resistance to negligible levels. Also, the good CMR of U1 preserves better than 14-bit integral nonlinearity (INL). While the output ripple of the filter is at the sub-16-bit level, its 16-bit settling time is approximately 0.1 s.

A closer look at the circuit reveals such details as the criss-crossed connection of ripple counters U4-U7. The purpose of this curious topology is to equalize the carry propagation delays of the four 'HCT393s. Together these delays, of the order of 20 ns/bit, represent more than 10 DAC LSB-bits. If left uncompensated, the manufacturing tolerances in the counter chips could

result in an unacceptable (up to several LSB-bits) zero-offset in the PWM waveform. Adding the cross-connects allows each '393 to contribute equally to both counters. It distributes the propagation delay of the four chips equally over the two 16-bit counting chains, thus cancelling this error source.

Downloading a DAC setting from the PC to the PWM DAC involves a three-step process. First, the D7 bit is cleared to disable the clock. D4 is set to clear all the counter bits. Then, D4 is cleared and D5 and D6 are toggled the requisite number of times to enter the desired output value into the MSB byte (D5) and LSB byte (D6) of the conversion value. The somewhat large number (up to 256) of interface operations

required to enter the conversion value using this “unary” serial means is outweighed by the simplification it affords in the conversion logic. The ability to use non-presettable counter chips was quite convenient. The actual time required for download of a new conversion is, in any case, much faster than the settling time of the U1 filter.

Following the download of the conversion value, bit D7 is set to enable the clock. Then, the continuous generation of the PWM waveform commences. An example of suitable code for keyboard input and downloading of DAC settings is presented in the MSBasic listing. This code listing is located at www.PlanetEE.com (click on the Ideas for Design icon). 