Circuit Measures Small Currents Referenced To High-Voltage Rails

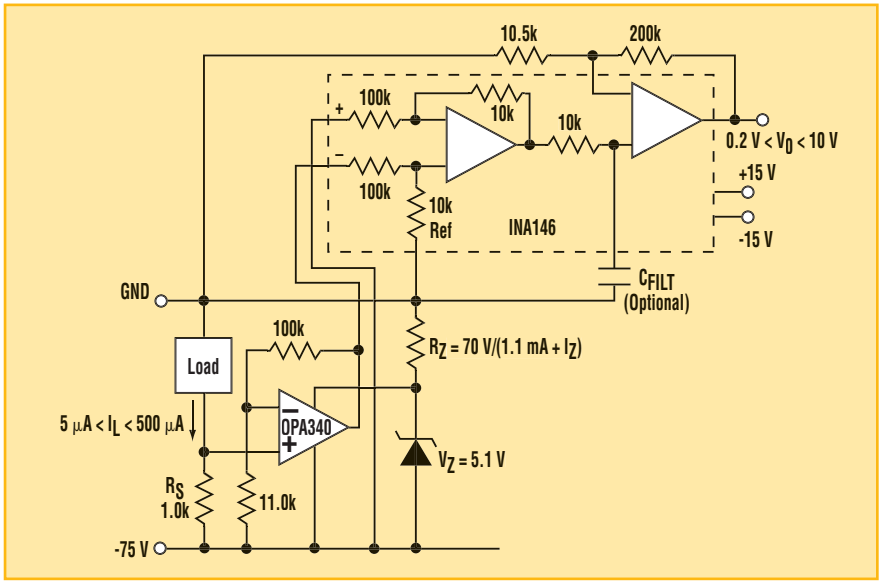
William P. Klein, PE
Texas Instruments, 6370 South Tucson Blvd., Tucson, AZ 86706; e-mail: klein_bill@ti.com

CIRCLE 520

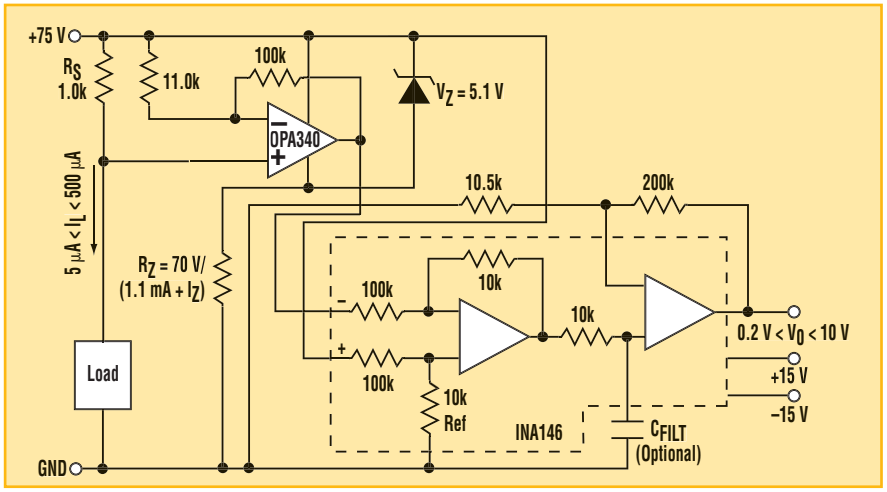
Designs that need to measure small signals riding on high-voltage power rails suggest the use of isolation devices. However, a high-common-mode-voltage instrumentation amplifier used with a rail-to-rail input and output amplifier can recover the signal cleanly and at a much lower cost.

Consider the system where a 5- to 500-µA current is flowing in a circuit at −75 V. A 1-kΩ sense resistor will not disturb the circuit in this instance and will provide a 5- to 500-mV signal. Direct application of the sense voltage to a difference amplifier is not advised because the magnitude of the sense resistor will unbalance the input of the difference amplifier. This will compromise the common-mode rejection of the difference amplifier. A solution is shown in Figure 1.

The voltage developed across the 1-kΩ sense resistor, R_S, is applied to the noninverting input of the OPA340. With a gain of 10, the output of the OPA340 swings from 50 mV to 5 V above the −75-V rail.



1. The sense voltage should be buffered using a CMOS op amp before sending the signal to the difference amplifier.



2. A similar circuit configuration will detect small currents referenced to a large positive voltage rail.

A simple zener-regulated 5.1-V supply is used to power the OPA340. This minimal regulator is adequate because the load current variation from minimum to maximum is 5 µA. This design is based on a load of 1.1 mA for the op amp and 5 mA for the zener diode. The value of R_Z is then set at (75 V − 5 V)/(6.1 mA) or 11.5 kΩ. Since the current through the zener is relatively constant, the change in supply for the op amp will be insignificant.

The INA146 is furnished with ±15-V supplies about ground. The input stage of the INA146 has a gain of 0.1 V/V. This gain ratio, accomplished with 100-kΩ input resistors, allows common-mode voltages of ±100 V. A gain of 20 V/V is set with the 200-kΩ and 10.5-kΩ second-stage gain resistors. The output signal will now swing between 0.2 V and 10 V.

Note that while the output signal is only positive, a negative supply is required for the INA146. This supply is necessary to allow the large negative

common-mode voltage.

Variations in the –75-V rail will cause the output of the OPA340 to change but will be rejected from the INA146 output by its common-mode rejection of 80 dB. This translates to 100 µV of output change per volt of change in the –75-V rail.

For the situation where the signal is sensed from a high positive supply, a similar circuit as shown in Figure 2 can be used.

Serial-Port-Powered ADC Streams Data To PC

Dale Litwhiler

Lockheed Martin Commercial Space Systems, e-mail: dale.h.litwhiler@lmco.com

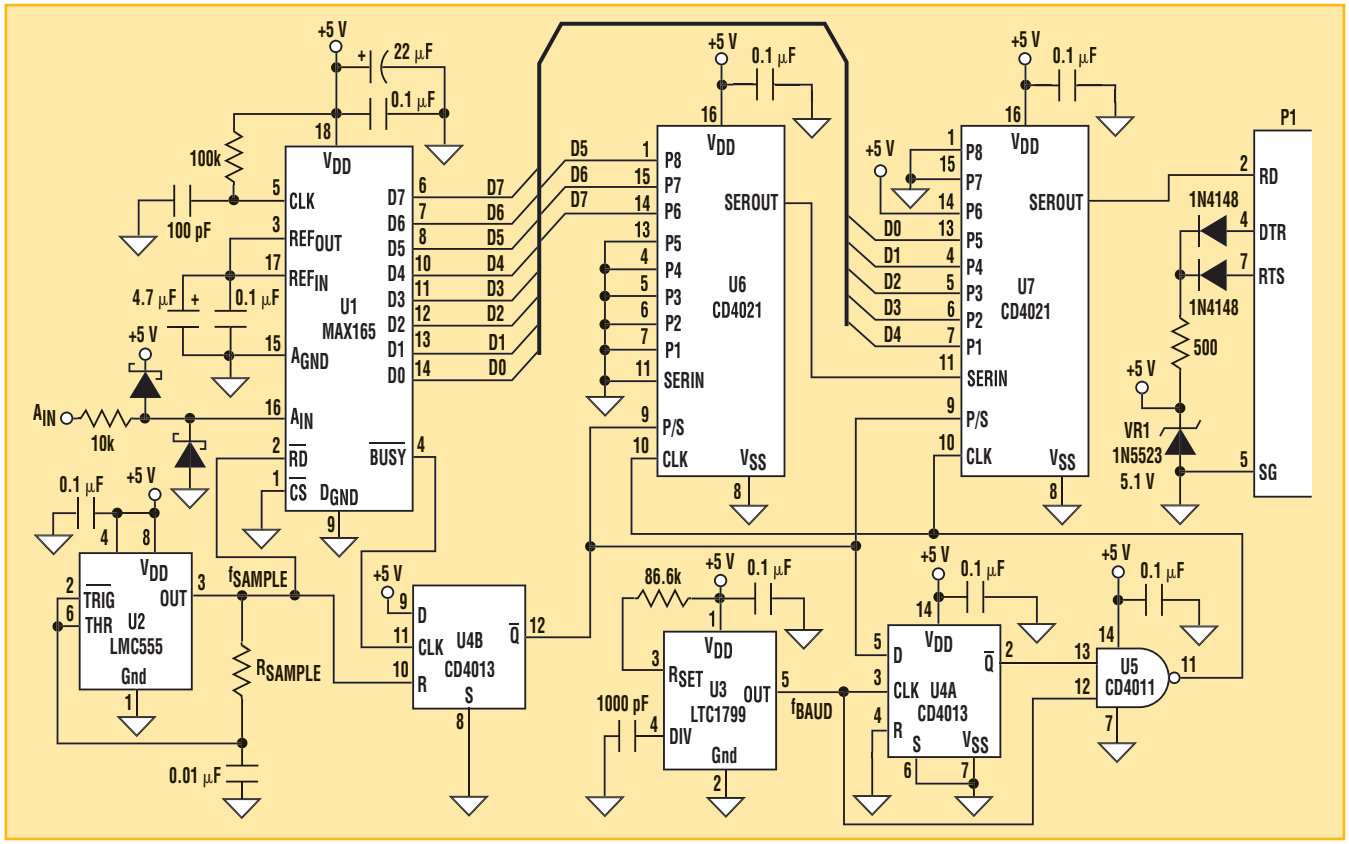
The circuit shown in Figure 1 provides a simple, low-power means of digitizing analog signals and sending the data directly to a PC's serial port where it can easily be read, analyzed, and stored. The low power requirements of this circuit allow it to be powered directly from the control signal outputs of the serial port. Thus, no external power supply is required.

When power is applied, the circuit continually samples the analog input at the frequency set by the sample clock. It transmits the data serially to the PC at the baud rate set by the baud-rate clock. Sampling frequencies up to 4 kHz can be achieved by the circuit as shown. These sampling rates make this circuit suitable for chart-recorder-type applications.

The circuit is comprised of an 8-bit parallel analog-to-digital converter (ADC) with an internal sample-and-hold and voltage reference (U1), a sample-frequency oscillator (U2), a baud-rate oscillator (U3), gating circuitry (U4 and U5), parallel-in/serial-out shift registers (U6 and U7), and power-conditioning circuitry (VR1 and nearby components).

The ADC's parallel outputs are connected to the shift registers such that they can be shifted out in order from LSB to MSB following the hard-wired high start bit at U7 pin 14. The stop bit and all trailing bits are hard-wired low (U6 pins 13, 4, 5, 6, 7, and 11, respectively) to complete the formatted serial byte with 8 data bits, no parity, and one stop bit. The serial output from this circuit at U7 pin 3 is a 0- to 5-V signal, which is adequate to be recognized as having pseudo-RS-232 logic levels by most PCs. The ASCII value of the eight data bits is inverted due to the RS-232 convention of a logic zero being a high-level voltage. This inversion can easily be corrected in the software used to read the data from the serial port.

U1 is the MAX165 CMOS-microprocessor-compatible, 5-µs, 8-bit, parallel-output ADC. The analog input voltage range is 0.0 to +2.46 V. U1 is



The low power requirements of this data-acquisition circuit allow it to be powered directly from a PC's serial port.

configured to use its internal conversion oscillator with the 100-kΩ resistor and the 100-pF capacitor connected to pin 5. With this setup, the typical conversion time is 5 µs. An A/D conversion begins on the falling edge of the sample clock, which is connected to the $\overline{RD}$ input of U1. The $\overline{BUSY}$ signal of U1 is low during the conversion and transitions high to indicate that the conversion is complete. Data from the most recent conversion is available at the parallel outputs within 80 ns after $\overline{BUSY}$ transitions high.

The rising edge of $\overline{BUSY}$ clocks the D flip-flop, U4B, to produce a falling edge on the Q output that latches the parallel data into the shift registers. The delay through U4B allows the ADC's parallel outputs to set up prior to being latched into the shift registers. Then, U4B is reset by the high level of the sample clock. The baud-rate oscillator output is gated by U4B's $\overline{Q}$ signal, and data begins shifting out of the registers on the falling edge following the first rising edge of the baud clock after a conversion is complete. This gating is required to ensure that no partial baud-rate clock periods appear at the beginning of the data stream.

The circuit as shown runs at a baud rate of 115.2 kbits/s, which is set by the 86.6-kΩ resistor between U3-1 and U3-3. The accuracy and stability of U3 is such that no trimming is necessary to obtain adequate baud-rate timing. The sampling frequency is less critical and is therefore set by a CMOS 555 timer to minimize power consumption.

The circuit was tested with sampling rates from 100 Hz to 4 kHz. The total 5-V supply current for this circuit was measured at about 4 mA, which is easily provided by the DTR and RTS modem-control signal outputs of the PC's port. The supply voltage for all of the ICs is regulated by the 5.1-V Zener diode, VR1.

On the PC end, many software implementations are possible. Home-grown C code or applications such as LabView can easily be used to perform the following steps to set up and receive data: (1) Set up the desired serial port (such as COM1) for the circuit's baud rate (115.2 kbits/s for the circuit shown), eight data bits, no parity, and one stop bit. (2) Set the DTR and RTS modem-control outputs high to apply power to the circuit. (3) Begin reading received data from the serial port buffer. The ASCII value of each character read from the buffer must be subtracted from 255 to account for the data bit inversion discussed earlier. The software can then become as elaborate as the application requires. This can range from simple data logging to a full-blown virtual oscilloscope with triggering, display, histogram analysis, etc.

The serial port buffer can be read at a convenient, noncritical timing interval set by the software. This interval can be up to several seconds, depending on the size of the receive buffer and the sampling frequency of the circuit. Regardless of the interval chosen, the appended data points will maintain the point-to-point time spacing set by the sampling clock of the circuit.

This circuit can be used to monitor low-frequency transducers such as seismic or pressure sensors. Additional analog signal-conditioning circuits (gain, scaling and filter networks) can be added to this circuit without the need for an external power supply. A plethora of micropower, single-supply voltage operational amplifiers are commercially available to perform such functions.

Inductance-Substitution Circuit Uses Variable Coils

Dana Romero

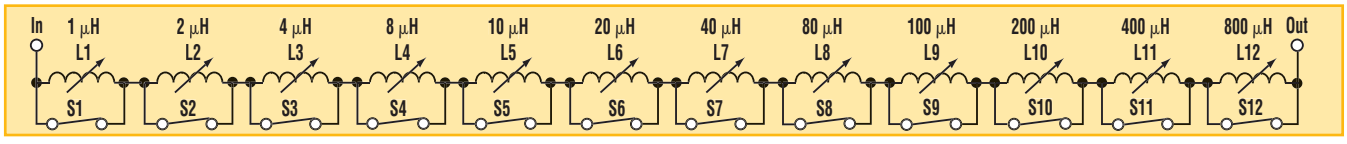
Phonex Broadband Corp., 6952 S. High Tech Drive, Midvale, UT 84047; e-mail: dromero@phonex.com

CIRCLE 522

When prototyping RF circuits, computer simulation or design programs can potentially yield the wrong component values. These errors are caused by the omission of capacitances or inductances originating from the board layout or other considerations. This can be quite problematic when it comes to surface-mount or through-hole components where, after a few changes, the pc-board pads can be lifted or ruined.

One alternative is the use of old-fashioned component substitution, where different components are quickly switched in or out to achieve a range of values. The process is greatly simplified if individual values are grouped into a convenient sequence. Since BCD code is most easily added mentally, I chose the following sequence: 1, 2, 4, 8, 10, 20, 40, 80, 100, 200, 400, 800 *(see the figure)*. Unfortunately, standard capacitors and inductors aren't available in these values. For an inductance-substitution circuit, the easy solution is to use adjustable coils. Even though 1, 10, and 100 µH are standard inductor values, variable coils have the added advantage of allowing the user to set these and all of the other inductances to within 1% of the desired values. To achieve a value of 2.00 µH, adjust a 2.2-µH coil downward; for a value of 4.00 µH, adjust a 3.9-µH coil upward; and for a value of 8.00 µH, adjust an 8.2-µH coil downward. The same adjustment process is repeated for the other two decades.

In this circuit, each coil is shorted out of the sequence through default by its corresponding switch. To add the coil's value to the total substitution inductance, just open the switch. This scheme yields a range of values from 1 to 1665 µH (1.665 mH) in 1-µH steps.



Using variable inductors to create a binary set of component values makes the operation of this inductance-substitution box more intuitive.