High-Q Bandpass Filter Is Well Suited To Current-Mode Signal Processing

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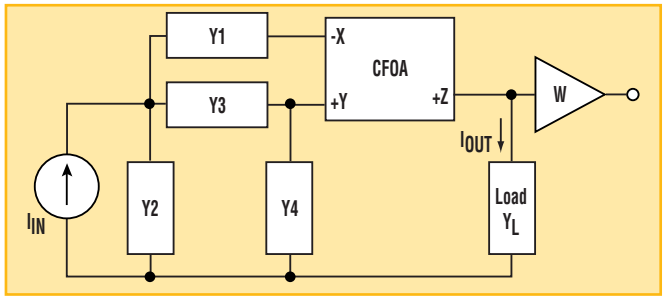
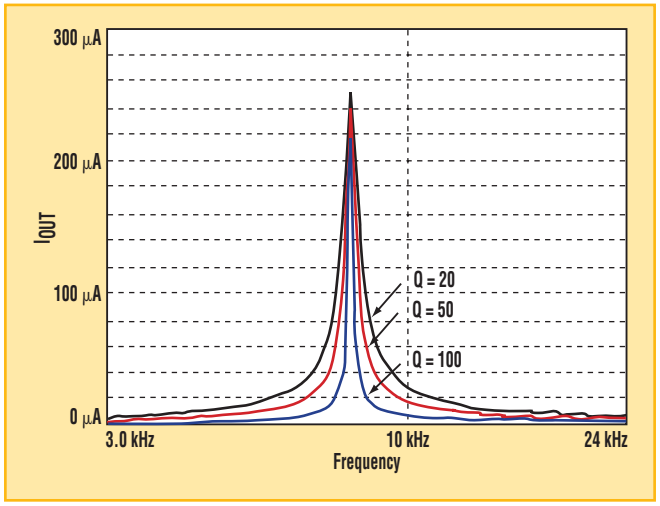


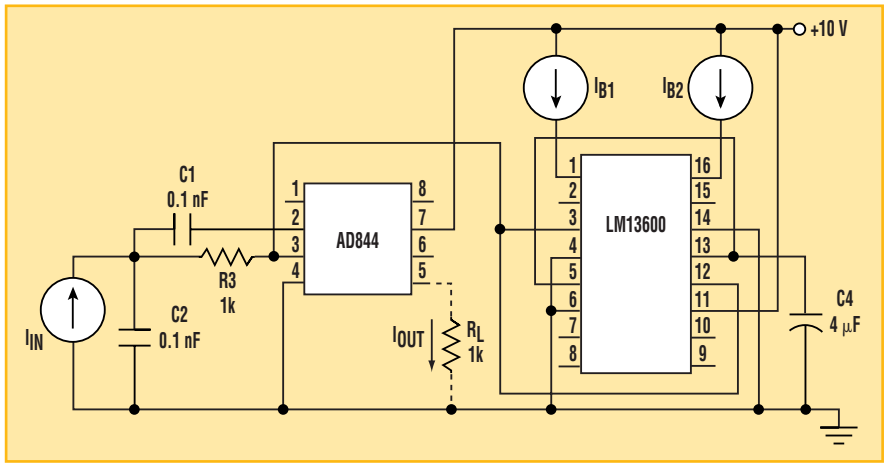
1. This current-mode second-order bandpass filter can easily provide quality factors as high as 100 without needing precision components.



3. The experimental results for three values of Q are shown. As G3 is varied, no shift in the natural frequency is observed.

Analog signal processing has conventionally been viewed as a voltage-dominated form of design. But voltage-mode processing can restrict the system's dynamic range. There is also a limitation on the input range of signals for linear operation. An approach to overcoming these problems is the use of voltage-to-current signal transformation. Recent advances in this context have opened a new dimension of analog design referred to as current-mode signal processing (CMP).

A novel current-mode second-order bandpass filter (BPF) is presented that can easily provide quality factors as high as 100 while still using nominal component values. Such high-Q filters are particularly important in applications like communication receivers and graphic equalizer displays. The circuit shown in Figure 1 provides a current-mode bi-quad output (for $Y_1 = sC_1$, $Y_2 = sC_2$, $Y_3 = G_3$, $Y_4 = 1/sL$). Terminal W is the voltage-buffered output. If needed, the circuit can be programmed as a high-pass or low-pass filter as well *(see the table)*.



2. A monolithic current-feedback op amp (AD844) and a dual-OTA implementation of a synthetic inductor (LM13600) fully implement the bandpass filter.

Analog Devices' AD844, a monolithic current-feedback op amp, forms the heart of the circuit *(Fig. 2)*. A dual-OTA implementation of a synthetic inductor, the LM13600 from National Semiconductor, is used for Y_4. This provides the additional advantage of current-tunable filter characteristics. The current-mode transfer function of the BPF is modeled as:

$$\frac{I_O}{I_{IN}} = \left[\frac{s\left(\frac{C_1}{C_2}\right)\times G_3 \times L}{s_2 + s\left(\frac{C_1 + C_2}{C_2 \times G_3 \times L}\right) + \frac{1}{C_2 \times L}}\right]$$

where $L = C_4/g_M^2$ and $G_3 = 1/R_3$ with $I_{B1} = I_{B2}$.

Upon analysis,

$$Q = \frac{G_3(C_2 \times C_4)^{\frac{1}{2}}}{g_M(C_1 + C_2)}$$

$$\omega_0^{\,2} = \frac{g_M^{\,2}}{(C_2 \times C_4)}$$

where g_M is the OTA's transconductance, which is the function of the biasing current. For the bias configuration shown:

$g_M = I_B/2V_T$

FILTER SUMMARY

Component	LPF	HPF	BPF
Y_1	G_1	sC_1	sC_1
Y_2	sC_2	G_2	sC_2
Y_3	sC_3	G_3	G_3
Y_4	G_4	sC_4	1/sL

where I_B = biasing current.

From these expressions, we can observe that independent control of Q is possible by varying only R_3. Varying R3 from 1 to 5 kΩ results in values of Q that range from 20 to 100, respectively.

Over this range of Q values, the other circuit parameters, with ω_o = 50 krad/sec (i.e., f_C is approximately 7.96 kHz) and with a simulated value of L = 4 H are:

$C_1 = C_2 = 0.1$ nF
$g_M = 1$ mΩ^{-1} (at $I_B \sim 50$ μA)
$C_4 = 4$ μF

The experimental results for three values of Q are shown in Figure 3. Note that in all the cases as G_3 is varied no shift in the natural frequency is observed, confirming the independent Q-factor control.

Interface 20-Bit Sigma-Delta ADCs Through A PC's Parallel Port

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CIRCLE 521

In most sigma-delta analog-to-digital converter (ADC) applications, the serial data transfer occurs through a serial port. A microcontroller configures the serial port as required—setting the baud rate and stop/start bits, initializing the serial port, and so on.

In this simple, inexpensive design, the ADC, an AD7703, connects to the PC via its parallel port *(Fig. 1)*. The controlling software is written in the graphic language LabVIEW version 6.0, which collects the ADC's serial data through one of the bits in the LPT1 Status port (0x379)—i.e., through pin 15 (LPT port ERROR input) of the DB-25 connector. Software can be written in any higher language like Turbo "C," C++, VB, VC, etc. The AD7703 is connected in the synchronous external-clock (SEC) mode to permit the direct interfacing of the synchronous serial data transfer to the host PC.

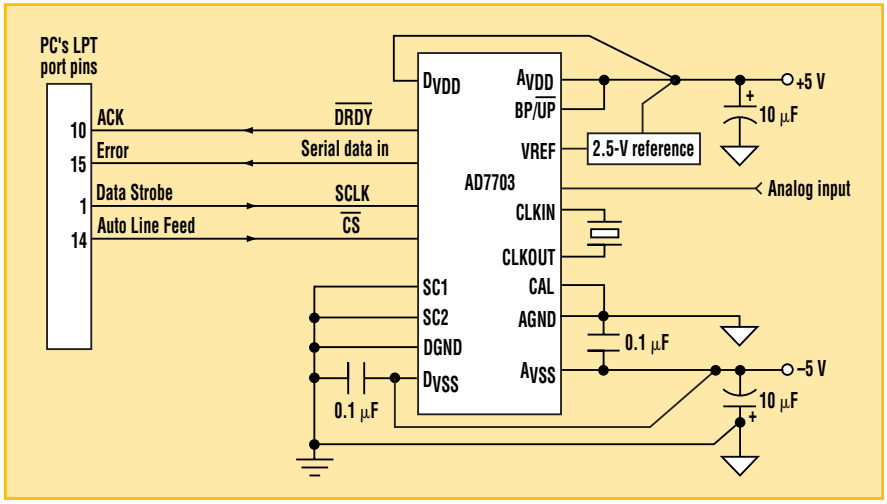
Once the ADC completes the conversion, its Data Ready ($\overline{DRDY}$) pin goes from high to low. The DRDY output of the ADC is connected to the PC's LPT1 port, pin 10 (Acknowledge input). The controlling software senses the DRDY and sets the ADC's chip select, $\overline{CS}$, through pin 1 (DATA Strobe output) to low and receives the most significant bit (MSB) from the ADC. After receiving the MSB, it generates a Serial Clock output (SCLK) through pin 14 (Auto Line Feed output) to acquire the remaining 19 bits from the ADC.

Once all 20 bits are received, the $\overline{CS}$ is set to high, enabling the ADC to set the new data in its three-state output buffer. This sequence will continue, and the acquired data will be displayed in both the digital and analog panel meters on the LabVIEW front panel *(Fig. 2)*.

As the serial 20-bit data is acquired through pin 15, the controlling software shifts most of the bits left as per the bit position. Some of the bits are shifted right, setting other unwanted bits to zero. Finally, a logic OR function of the 20-byte word produces the 20-bit pattern of the acquired signal.

For example, the MSB 20th bit will appear as the first bit for transfer. This bit must be set as the 20th position of the word. Therefore, the data received through the fourth (D3) bit has to be shifted 16 positions left to form it as a 20th bit.

Similarly, the next MSB received through this D3 bit is shifted 15 positions left to assign it as a 19th bit, and so on. In this sequence of data fashioning, once the fourth bit of the 20-bit pattern (LSB 4) has appeared, it doesn't need any shifting because it's an actual



1. A 20-bit sigma-delta ADC, such as the AD7703, can have its serial data output sent to a PC's parallel port. There, pin 15 accepts the serial data.

D3 bit. Likewise, for the third bit (D2), shifting is required to the right by one position, and the D1 and D0 bits require right shifting by two and three positions, respectively.

This way of shifting and finally doing a logical OR produces the exact 20-bit data pattern from the serial data received through one pin of the parallel port. The LabVIEW Virtual Instrument program provides a time delay of 125 µs between SCLK and the serial data read (i.e., inport function). This sets the data transfer rate to 4 kHz, the maximum suggested by the manufacturer. This time delay will let the read cycle read exactly at the midpoint of the data bit to avoid an improper data read.

Designers can use this simple and low-cost approach with any sigma-delta ADC. But ADCs that include a start bit and a stop bit in each byte will require a slight program modification.

2. The LabVIEW program produces this "virtual" front panel. Note that both analog and digital meter displays are featured.

Read Temperature With One Digital Output And One Digital Input

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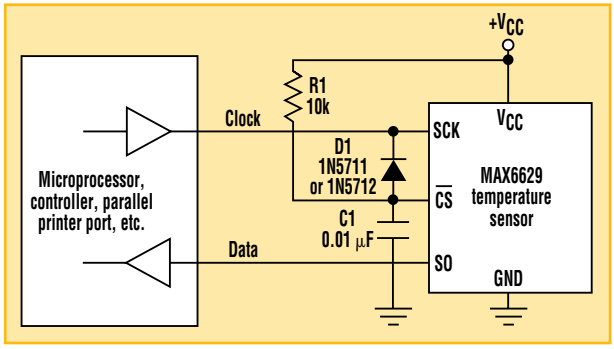
CIRCLE 522

Before the MAX6629/30/31/32 series of temperature sensors were available, all digital-output temperature sensors were I²C (alternatively called SMBus) sensors that had to be written to for addressing, before they were read. Prior SPI sensors also required writing. Because the MAX66xx series sensors are read-only, data can be obtained by simply clocking them. But there's one tiny complication—they use a chip-select line.

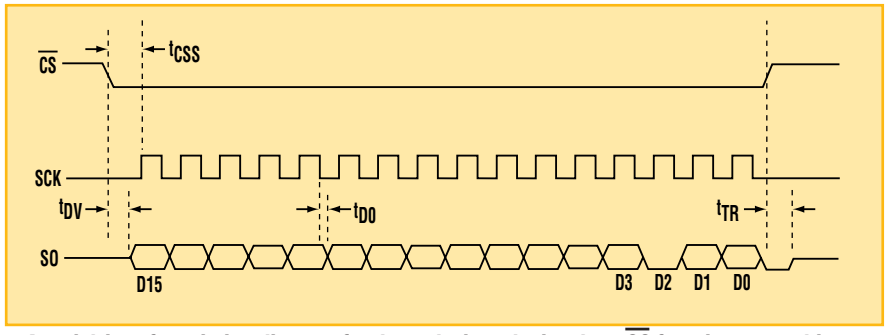
You can get around the need for an additional logic line to drive the chip-select line with the circuit shown in Figure 1. Only one digital output and one digital input are necessary to communicate with a MAX66xx device by simply clocking it to retrieve the digital data.



1. This circuit eliminates the need for an additional logic line to drive the $\overline{CS}$ pin of the MAX6629/30/31/32 series digital-output temperature sensors. Temperature data is obtained by simply clocking it out of the device.

Normally, serial-interface temperature sensors require three interface lines: $\overline{CS}$, SO, and SCK, the functions of which are depicted in the timing diagram in Figure 2. If only two lines are available, Clock and Data, this circuit makes it possible to communicate with the device without a separate $\overline{CS}$ line. This method requires that the "rest" or quiescent state of the clock be high, modifying the above timing diagram accordingly.

The circuit operates by generating a $\overline{CS}$ signal from the clock. When the clock initially goes low, it pulls down the $\overline{CS}$ line via Schottky diode D1. Set the time constant of R1 and C1 so that the $\overline{CS}$ line rises to no higher than $0.3 \times V_{CC}$ between clock pulses. The resultant slow rise of $\overline{CS}$ must be greater than $0.7 \times V_{CC}$ for at least 0.5 s between reads to let the devices perform temperature-to-digital conversions.



2. A serial-interface timing diagram for these devices depicts how $\overline{CS}$ functions as a chip-select line. $\overline{CS}$ essentially enables the interface by going low. $\overline{CS}$ also suspends temperature-to-digital conversions until it returns to a high level greater than $0.7 \times V_{CC}$, after which you must wait at least 0.5 s before reading again to complete a new conversion.

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