ESD: where it comes from and how to protect against it

There's no doubt about it: Overvoltage causes severe damage. Learn how to protect devices and discover test methods for determining the robustness of ICs when subjected to ESD.

By Michael Krickl, Maxim GmbH, Planegg, Germany

Minimum levels of distortion immunity have been required for all electronic devices produced in Europe since early 1996. Because distortion is caused in part by electrostatic discharge (ESD), the European Community has issued a directive forcing manufacturers to protect their devices against ESD as well.

Semiconductor manufacturers have increasingly turned their attention to ESD protection. Protecting RS-232 and RS-485 serial-interface networks, for instance, is especially important because their interface drivers are usually accessible to users and the ESD charge they carry. Unfortunately, designing protection circuitry for serial-interface networks and other applications is often hampered by uncertainties in estimating the level of anticipated overvoltage.

Where do dangerous voltages come from?

Most people have been exposed to an overvoltage discharge. A handshake, for example, in a room with low air humidity sometimes produces a spark when hands touch. This effect is amplified if the handshakers are standing on a carpet. Walk with leather-soled shoes on that carpet and body capacitance can charge up to 25 kV.

Bringing two different materials together and then separating them always produces an electrostatic charge, in which the level of voltage depends on the air humidity and the charge affinity between the two materials, among other factors. It also depends on how the materials are brought together and for how long. Rubbing cat fur on amber or plastic, for instance, produces an exchange of charges between different materials. A spark to a nearby grounded metallic object proves that a charge was generated. Similarly, drawing a cable over a carpet creates charge—probably quite a bit more charge than a cable fixed within a wiring harness.

In general, ESD involves charging a small capacitance to a very high voltage. This voltage becomes dangerous when discharged (for instance) into an accessible interface pin. Thus, it's never easy to predict the amount of electrostatic charge or the level of voltage produced. Nor should you underestimate the potential for damage when a user touches the accessible pins in an interface plug.

Cause and effect

You seldom find a high ohmic resistance to limit failure during electrostatic discharge into an IC. The resistance of a human body is estimated at 1500Ω, which limits discharge current when a person touches an IC pin. But the ohmic-resistance opposing discharge at the instant of plugging in a cable is nearly zero. The consequence is a very short peak current, flowing into the

affected IC pin, that measures several tens of amperes. The current level depends on the level of voltage across the cable capacitance.

High current generates various forms of severe damage in a monolithic IC. Local heat generation can even melt the silicon. Typical effects after electrostatic discharge are damaged metallization connections and ruptured passivation; you'll also find transistors damaged by electrothermal migration.

An ESD discharge can also cause latchup, which results from the activation of triac-like structures within a CMOS device. High electrostatic voltage can activate these structures, allowing the flow of high current, mostly from the power supply to ground. Interface drivers can exhibit latchup currents as high as 1A, and this current can be interrupted only by switching off the power supply. By that time, however, the IC is usually damaged by heat.

Errors and related costs

Normally, an interface device damaged by ESD is not reliable because it may introduce data errors. (In the worst case, no further data traffic is possible.) To analyze the effect of such damage, Maxim collected RS-232 interface drivers from different manufacturers, subjected them to ESD events, and then examined each for malfunction.

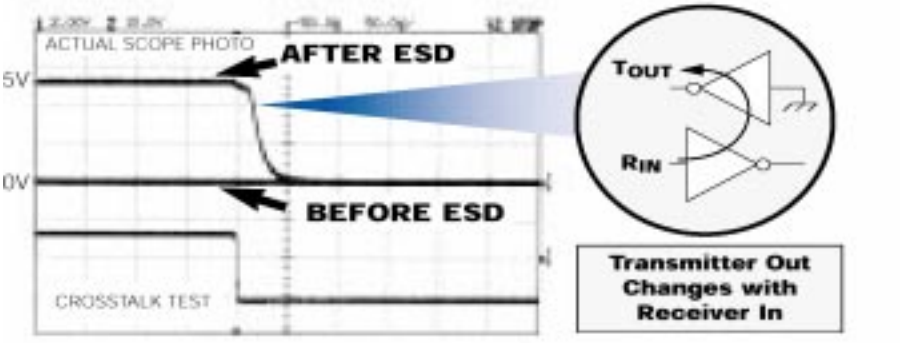

Figure 1: Received signal can couple to a driver output after ESD damage.

After an overvoltage discharge, the typical cause of communication problems is crosstalk, in which a signal on the receiver input feeds through to the output of an adjacent transmitter. Thus, unintended coupling of the receiver signal to an adjacent transmitter (**Figure 1**) causes data errors. Other examinations reveal inadmissible current paths through the IC, allowing (for example) RS-232 signals at the receiver input to feed through to the power-supply pin. If the power supply is unable to maintain its nominal output voltage by sinking this current, it can produce overvoltage that damages other parts of the circuit (**Figure 2**). In other cases, the interface drivers are so heavily damaged that they no longer function, and the interface is no longer usable.

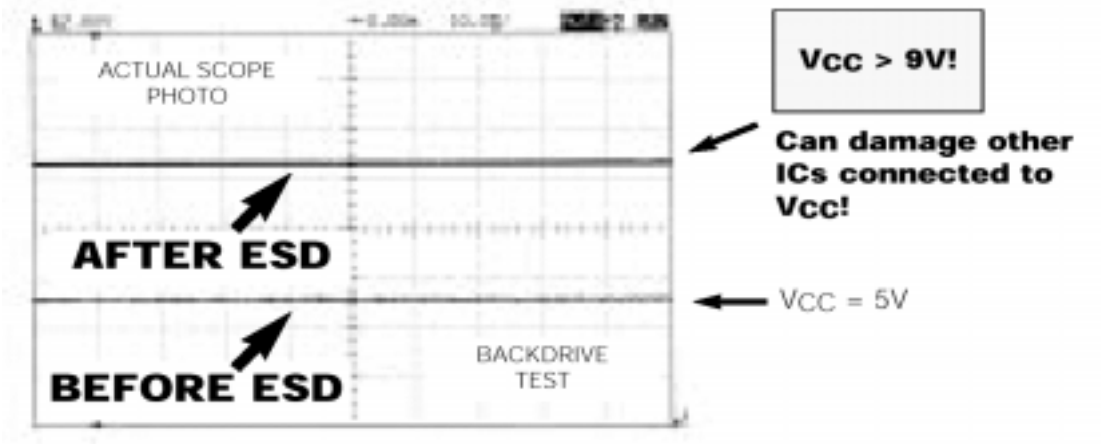

Figure 2: An IC damaged by an ESD event can feed through the received signal to the supply voltage.

The damage described above can cause field and production failures at the interface connectors of desktop computers, notebooks, modems, and other communication devices. Making the repairs or exchanging pc boards after a long search for the failure reason costs a lot of time and money. The cost of effective ESD protection in the production stage, however, is only a fraction of that sum.

Protection

Depending on the type of interface and its mode of operation, several approaches have proven effective in protecting valuable interface circuits against electrostatic discharge. The simplest, perhaps, is a resistor/capacitor combination in front of every driver and receiver. The resistor connects in series with the cable to limit peak currents, and the capacitor connects directly between ground and the driver or receiver to limit short-term voltage peaks.

The advantage of this circuit is its very low cost, but the protection it provides is not very effective. The danger of ESD damage is lower but still exists because the RC combination doesn't really limit voltage peaks. It only limits the voltage slew rate. What's more, the use of RC combinations on both the receiver and transmitter sides generates signal distortion that limits the cable length and reduces the maximum data rate. Finally, these additional parts consume board space.

In another widely used technique, you can add avalanche suppressors or TransZorb diodes at every transmitter output and receiver input. This protection is very effective; ICs are no longer subject to ESD damage. Disadvantages include the need for more board space to accommodate the additional components. Also, the components add significant capacitance to the transmission line. Finally, TransZorbs are expensive (about 25¢ each). A typical COM port with three drivers and five receivers needs eight protection diodes costing as much as $2.

Choose interface drivers with integrated ESD protection for the most effective and lowest cost approach. Prices are higher than for unprotected drivers, but the cost is lower than for external protection diodes. Integrated protection normally does not increase the input or output capacitance of any pin, and it saves board space.

Test methods

To properly evaluate devices with internal ESD protection, you should note the voltage levels at which they are tested and the method by which these voltages are determined. Manufacturers should test these ICs in a thorough manner, applying ESD levels that step up in sufficiently small increments from 0V to the maximum rating.

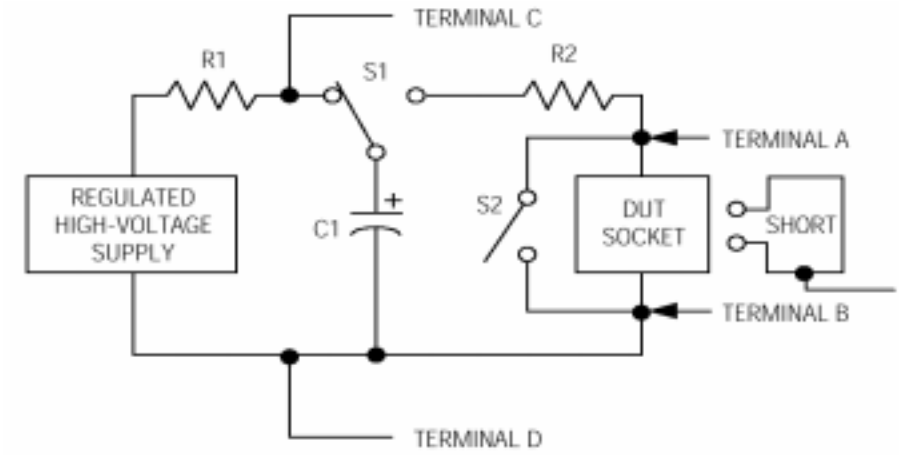

Figure 3: The Human Body Model and the IEC1000-4-2 test method specify the same test circuit but with different component values.

One feature common to all test methods is a test circuit that determines the maximum voltage for which the device under test (DUT) is immune to ESD damage (**Figure 3**). This circuit consists of a high-voltage source whose adjustable output charges a capacitor (C1) via a high-valued resistor (R1). Flipping the switch S1 or using an ESD gun (see below) allows the capacitor to discharge into the DUT via the discharge resistor (R2). Values for the capacitor, charge resistor, and discharge resistor vary according to whether IEC1000-4-2 or the Human Body Model (HBM) is applied (**Table 1**). Because the IEC1000-4-2 discharge resistance (R2) is lower and its capacitance (C1) is higher, the IEC1000-4-2 test circuit generates currents significantly higher than those created using the HBM circuit for a given voltage (**Table 2**).

Table 1— Test circuit component values

COMPONENT	HUMAN BODY MODEL	IEC1000-4-2
Charge resistor R1 (Ω)	1M to 10M	50M to 100M
Discharge resistor R2 (Ω)	1500 ±1%	330
Capacitor C1 (pF)	100 ±10%	150

Pins and voltage ranges

In principle, all I/O pins should be tested because they have contact with the outside world (they can be touched, and cables connected to them can be plugged or unplugged). For accurate results, you should connect the DUT the same way it will be configured in the target system, allowing ESD currents to flow as they will in the field.

An effective ESD test checks the entire voltage range up to the maximum specified voltage level. Unfortunately, some ICs show no failure after testing at 10 kV only, but exhibit ESD damage when subjected to lower voltages. Such an IC should not receive a ± 10-kV ESD rating, despite its ability to handle a 10-kV spike. HBM and IEC-1000-4-2 test methods prescribe that you test the entire voltage range in small steps of 200V. You also need to test positive and negative levels at each step. This procedure ensures that no gaps within the voltage range escape testing. The DUT above, for example, would be tested at ±200V, then ±400V, then ±600V, etc. The IC is then specified at the maximum voltage withstood by the weakest pin without damage.

To cover all possible situations, test an ESD-protected part in all possible operational modes. You should apply one test sequence with power applied and another with power off. If testing an IC that can be shut down (for example, an interface driver), test that mode with another sequence.

Repetitive testing and the criteria for success

All relevant test methods specify that each pin gets zapped 10 times at each voltage level, and with both positive and negative polarities—that is, 20 zaps for each voltage step. Various DUT parameters are tested after each voltage discharge. Maxim, for example, checks for constant supply current (a supply-current increase may indicate latchup), checks whether the driver output voltage is within the specified range, and checks whether the receiver input resistance is within the specified norm (a normal range is 3 kΩ to 7 kΩ). Testing proceeds only if all measurements are normal.

Human Body Model

The HBM is a modification of Method 3015.7, MIL-STD-883. Normally, this method provides that each pin of an IC is tested versus all other pins. The HBM method, which was developed to support the packaging and handling of electrostatically sensitive ICs, specifies that only input and output pins need testing. HBM test-circuit values (**Table 1**) simulate the resistance and capacitance of the human body.

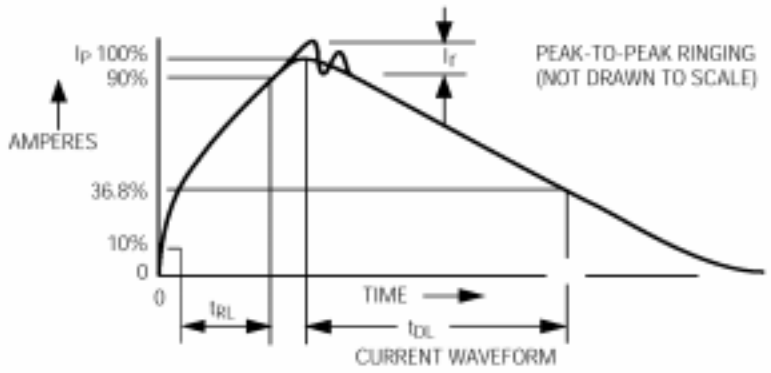

Figure 4: This current waverform illustrates a typical ESD event according to HBM.

Figure 4 shows a typical current waveform during an ESD event. The waveform represents ESD discharge when someone touches an IC. The duration of this discharge when tested according to the HBM is approximately 150 nsec. Peak currents in the HBM waveform are lower than in the corresponding IEC1000-4-2 discharge waveform, because the HBM test-circuit resistance (1500Ω) is higher. **Table 2** summarizes the peak-current estimates for both test methods. For HBM testing, Maxim uses a Model 4000 ESD tester from IMCS (Oryx Technology Corp, Fremont, CA).

Table 2—Estimated peak currents during an ESD event

APPLIED VOLTAGE (kV)	PEAK CURRENT (A) HUMAN BODY MODEL	PEAK CURRENT (A) IEC1000-4-2
2	1.33	7.5
4	2.67	15.0
6	4.00	22.5
8	5.33	30.0
10	6.67	37.5

The IEC1000-4-2 Model

This test method, created by the International Electrotechnical Commission (IEC), tests only input and output pins (as with the HBM method). Tests performed with the IEC1000-4-2 model are harder to pass than those using the HBM. IEC1000-4-2 models ESD events that occur when a person carrying a metallic object touches an interface contact with it. Accordingly, the discharge resistor (R2) is reduced to 330Ω from the HBM's 1500Ω, and the human body capacitance is increased to 150 pF (vs. 100 pF for HBM).

During discharge, the current waveform exhibits a faster slew rate than that of the HBM, and the peak currents are five times as high (**Figure 5).** Because the time constant of discharge resistor and body capacitance is lower, the current waveform's approximate duration is only 100 nsec.

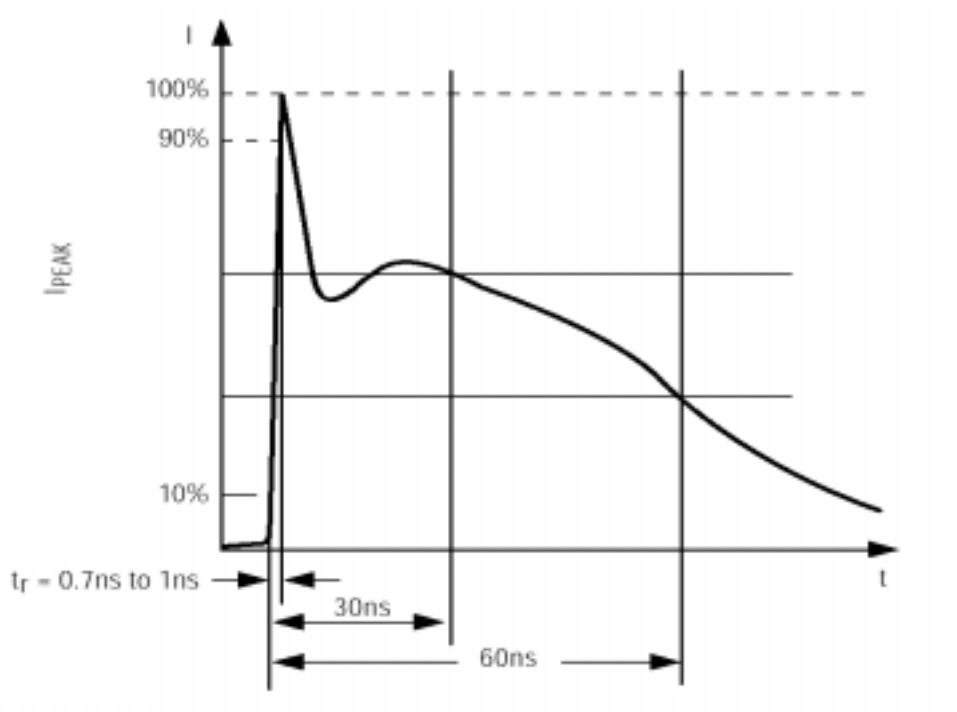

Figure 5: This current waveform illustrates a typical ESD event according to test method IEC1000-4-2.

IEC1000-4-2 distinguishes four maximum discharge voltages (**Table 3**). In addition to the contact discharge test required by the HBM test method, this method also specifies an air-gap-discharge test. Moving the test electrode rapidly and (if possible) in line with the pin to be tested, the air-gap-discharge technique approximates the so-called "ESD pistol." It causes a spark discharge at a certain distance from the pin. In the contact-discharge technique, the ESD pistol is brought in contact with the pin to be tested before initiating the discharge. For IEC1000-4-2 testing, Maxim uses a Model NSG435 ESD pistol from Schaffner Instruments.

Table 3—The IEC1000-4-2 classification of four voltage ranges

IEC1000-4-2 CLASS	MAX. TEST VOLTAGE (kV) CONTACT DISCHARGE	MAX. TEST VOLTAGE (kV) AIR GAP DISCHARGE
1	2	2
2	4	4
3	6	8
4	8	15

Danger increases with long cables

The methods above offer very good tools for approximating the danger caused by ESD initiated during the handling of ICs or by touching interface pins (that connect to IC pins). They are not sufficient, however, to examine a long, electrostatically charged cable. It's common to interconnect racks and shelves with cable, especially in telecomm equipment. Such cables can be 10m in length or more. Cables for the ubiquitous serial interface are sometimes longer than the 1 to 2m normally used to connect two devices. Finally, the RS-232 specification allows driver loads as high as 2500 pF in parallel with a 3-kΩ resistor. Assuming 100 pF per meter, the capacitance of a long cable might be 1 nF or higher—clearly more than that mentioned in the test methods above.

Cables are particularly vulnerable to electrostatic charging. Pulling a long cable over the floor (which in the worst case is covered with carpet) generates a dangerous charge. When you plug that cable into a connector, it discharges into the circuitry attached to the connector—with virtually no ohmic resistance to limit the resulting discharge current. (The test methods above include a 1500Ω or 330Ω current-limiting resistor.) When that cable is connected between two racks of equipment, a potential difference between the two racks can contribute additional current.

Interface-driver users therefore require a test model that respects this issue. Called the "cable discharge model," it specifies a test circuit similar to those of the methods already described, but one that reduces the discharge resistor to 0Ω. Zero resistance models the condition that prevails when you plug in a cable, with no ohmic resistance to limit current flow in the shield and other conductors.

Surge pulses vs. ESD events

The phenomenon of surge pulses is often associated with electrostatic discharge. Usually caused by high-voltage switching events, surge pulses have much lower peak voltages than do electrostatic discharges, but surge pulses contain more energy due to their longer duration. Depending on the class of surge event, surge pulses can last up to several hundred milliseconds. The energy content of such a pulse is about 30,000 times the energy of an electrostatic discharge. If HBM and IEC1000-4-2 test circuits were driven with surge pulses, the waveforms pictured in **Figures 4** and **5** would typically be 3000 times wider.

The main candidates for protection against surge pulses are pc boards connected to lines that go outside a building (regulated telecomm equipment, for instance). On-chip protection elements cannot protect against surge pulses; larger and more robust devices are necessary, such as gas discharge tubes, often in conjunction with suppressor diodes. These elements can dissipate a lot of power. **Table 4** compares the phenomena of electrostatic discharge and surge pulses (as specified in IEC1000-4-5).

Table 4—Comparison of ESD and SURGE

	FRICTION BETWEEN DISSIMILAR MATERIALS	LIGHTNING, SWITCH EVENTS
Resulting phenomenon	ESD	SURGE
Voltage	Up to ±15 kV	Up to 4 kV
Energy at maximum charge voltage	Less than 10 mJ	300J
Repetition rate	Single pulse	Up to 6 pulses per minute
Frequency limit	Approximately 1 GHz	Approximately 350 kHz
Susceptible hardware	Metallic objects subject to touch by people	AC lines, measurement lines, signal and data lines

Integrate protection

You need ESD protection for ICs because an electrostatic discharge jeopardizes any accessible electronic pins. The best such protection is integrated within the IC. If you include integrated ESD protection qualified according to the Human Body Model and IEC1000-4-2 specifications, you will significantly enhance the reliability of circuits exposed to ESD events.

Author's biography

Michael Krickl is senior application engineer at Maxim GmbH in Germany. He provides technical support and design-in work with large German customers. When he's not on the job, Krickl enjoys surfing the web and riding his motorcycle.