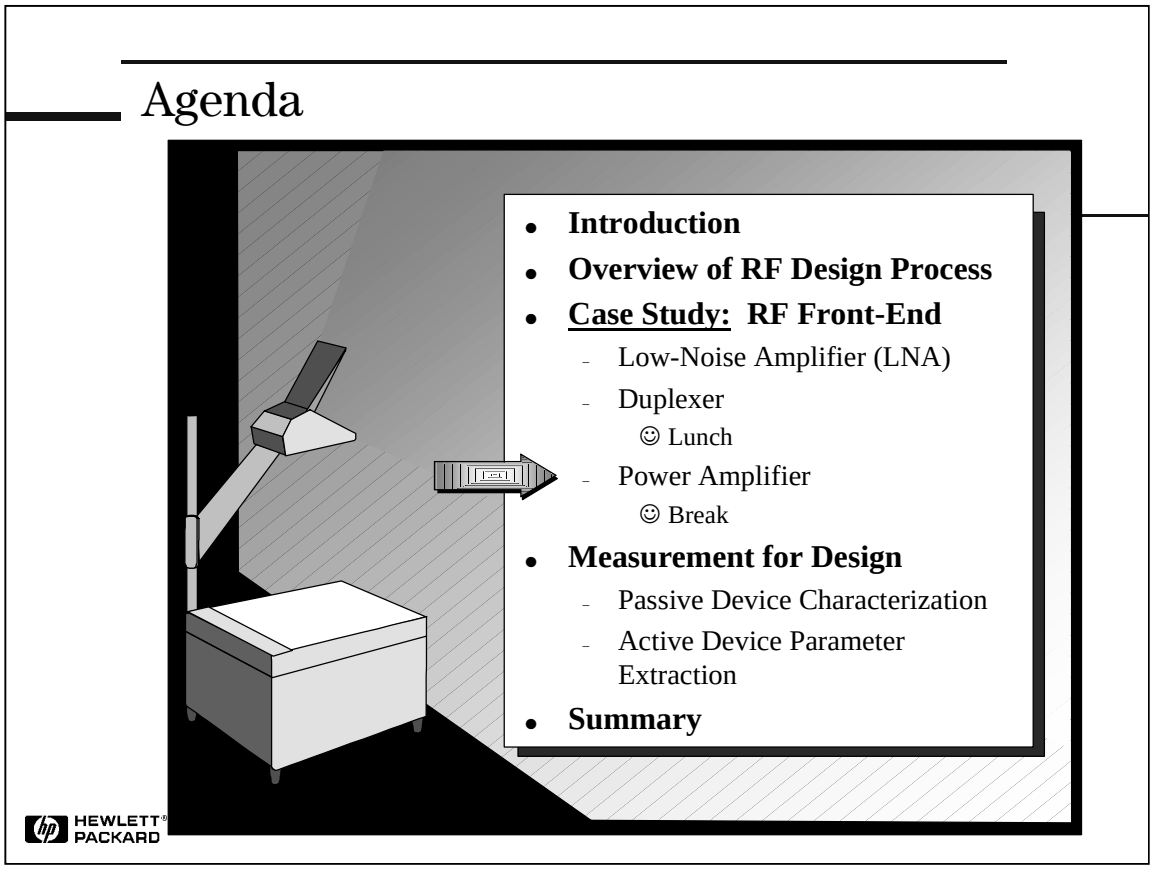
RF Design and Measurement Seminar

Slide #73



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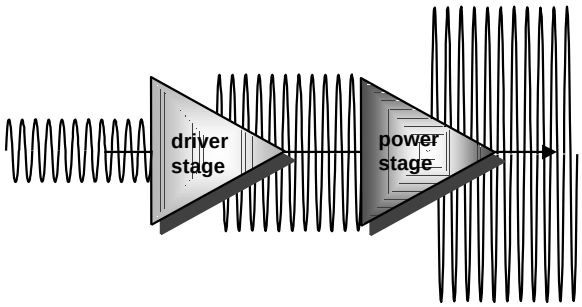
Slide #74

Power Amp Design

1.88 GHz PCS-Band Amplifier
- Gain > +24 dB
- 1-dB-compression > +25 dBm
- Psat > +27 dBm

Main challenge: designing for maximum power output

During brainstorm process, decided:
- two stages needed to get desired gain
- stage one:
  - silicon transistor
  - passive bias
- stage two:
  - power FET
  - active bias



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The design of the power amplifier portion of our PCS-band transceiver presented a different set of challenges from those encountered with the LNA. Because the output stage of most power amplifiers is designed to deliver maximum output power (rather than maximum small-signal gain), normal linear design techniques do not apply.

During the early brainstorm process of the design, we looked at different transistors and their specifications. We decided on a power field-effect-transistor (FET), an Avantek ATF45101, that would meet our design goal of 0.5 Watt (> +27dBm) output power. We also decided to use active biasing for reasons explained in the next slide. A single stage such as this could not be designed with the necessary gain (> +24 dB). Therefore, a driver stage was added, consisting of a single silicon transistor with conventional passive bias. The design of this driver stage is a preamp design very similar to that of the LNA, so it will not be covered in detail. Some interesting behavior was discovered when the two stages were connected together (which we will get to later).

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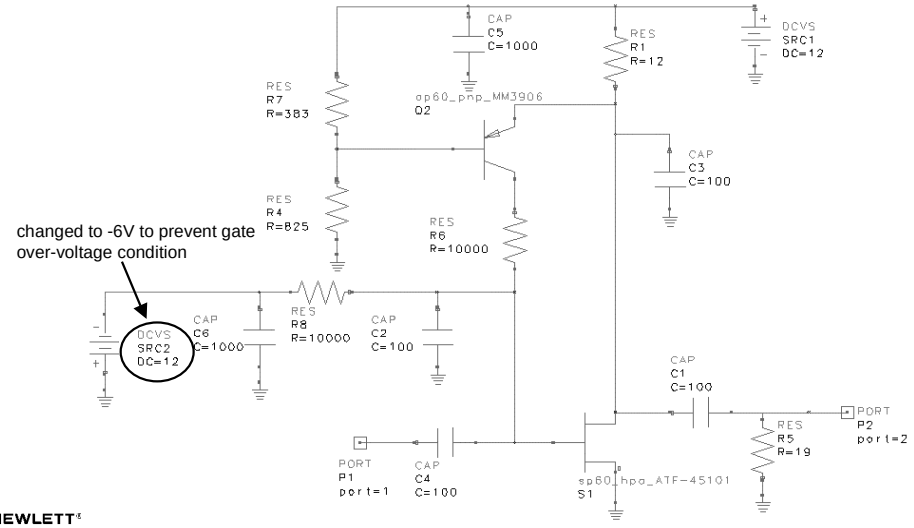
Slide #75

Bias Considerations - Active vs. Passive

- passive - simpler, less space, cheaper but not as well controlled
- active - extra circuitry, but more repeatable
- hint: watch out for over-biasing junctions (FET gate-bias example)



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While slightly more complicated than passive bias, active bias was chosen for the output stage because it is a very good way to guarantee a stable bias current for the power FET without the need for manual adjustments. Typically, FETs are loosely specified for drain-saturation current (Idss) and gate pinch-off voltage (Vp), so accurate bias using passive circuitry involves adjusting the gate voltage until the desired current is achieved. With active biasing, feedback is used to generate the correct drain-bias current. A low-frequency pnp transistor is used in the feedback loop.

Plus and minus 12 volt power supplies were available, and therefore our initial design used these values. All of the bias current comes from the positive supply; the minus supply is only needed so that a negative gate voltage can be generated. Early on, it was realized that if the minus supply was turned on before the plus supply, the gate-to-source voltage presented to the FET would be -12 V. This would have exceeded the specification for maximum Vgs, which would have likely damaged the FET. Since it is difficult to guarantee which supply comes up first when using a dual-output power supply, the minus supply rail was changed to -6 V, which is less than the specification for maximum gate-to-source voltage. In a real-world situation, a -6V power supply may not be readily available. If this were the case for us, we would have implemented additional circuitry to reduce the power supply voltage appropriately. For example, we could have used any of the following to achieve the -6V power supply: resistor divider circuit, 3-terminal regulator, or a Zener diode circuit.

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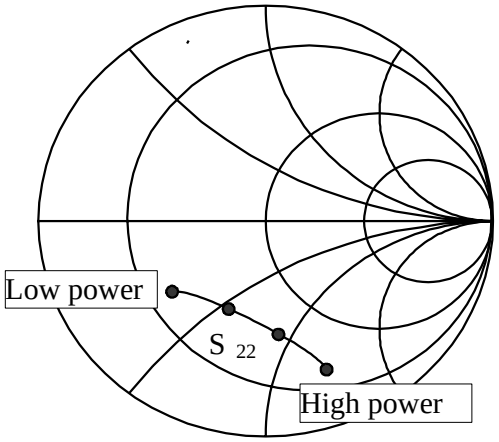
Slide #76

Designing the Output Stage for Maximum Output Power

- output impedance varies as function of output power
- ideal impedance exists for maximum output power
- two technique provides information for output-stage matching
  - load-pull technique
  - load-line analysis



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Designing the output-match network for power amplifiers is different from the complex-conjugate-matching technique used for small-signal linear amplifiers. This is because the output impedance (s22) of power devices varies as a function of output power. In general, an ideal termination impedance exists which maximizes the output power available from the amplifier. The goal of the output-match network is to transform 50 ohms into this ideal impedance. Unlike, the conjugate match technique used to maximize gain, here we trade-off gain for the purpose of achieving maximum output power.

There are two basic ways to find the ideal output impedance that must be presented to the power device of the amplifier. One is to perform a load-pull analysis (either simulated or with actual measurements) and the other is to design a matching network based on the physical model of the output device, load-line analysis.

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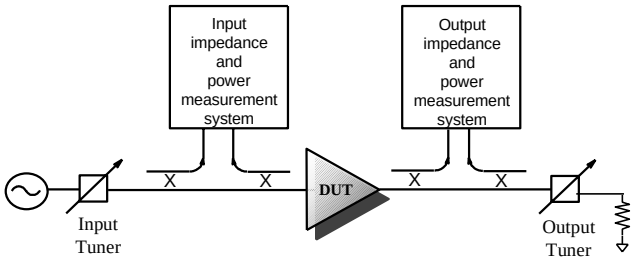
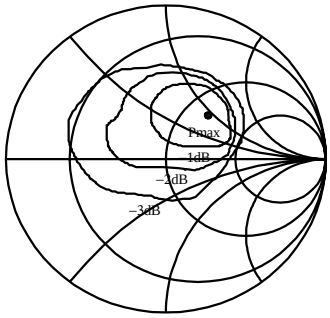
Slide #77

Load-Pull Technique

- vary magnitude and phase of load presented to circuit
- power output is measured at each impedance point
- can use behavioral model (based on measurements)





Constant output power contours versus output load impedance (input power constant)

Can be very expensive and time-intensive

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A load-pull measurement system can be very expensive. Typically, only companies that specialize solely in designing power amplifiers would invest in such a system.

The load-pull measurement technique is based on the measured behavior of an amplifier. Detailed understanding of the physical models of the devices involved is not necessary. The procedure for performing a load-pull analysis is to present the output of the amplifier with a variety of load impedances while simultaneously measuring the output power. The input match is adjusted each time as well to ensure a well-matched condition at the input of the amplifier.

This process is repeated with several different input-power levels. After all of the data is taken, contours of constant output power are plotted on the Smith chart. If the input power presented to the amplifier was large enough, a single point on the Smith chart appears where the output power was at a maximum. This is the impedance that we must present to the output of the amplifier.

The tuners used to vary the input and output matches can be based on mechanical-slug tuners or pin-diode-based electronic tuners. Mechanical tuners excel in high-power applications and, because of their inherent low loss, when it is necessary to characterize an amplifier with highly reflective impedances. Electronic tuners provide very fast and repeatable measurements.

In the majority of cases, designers will typically use either a load-line analysis or the preferred load-pull simulation technique. Let's look at both methods in more detail.

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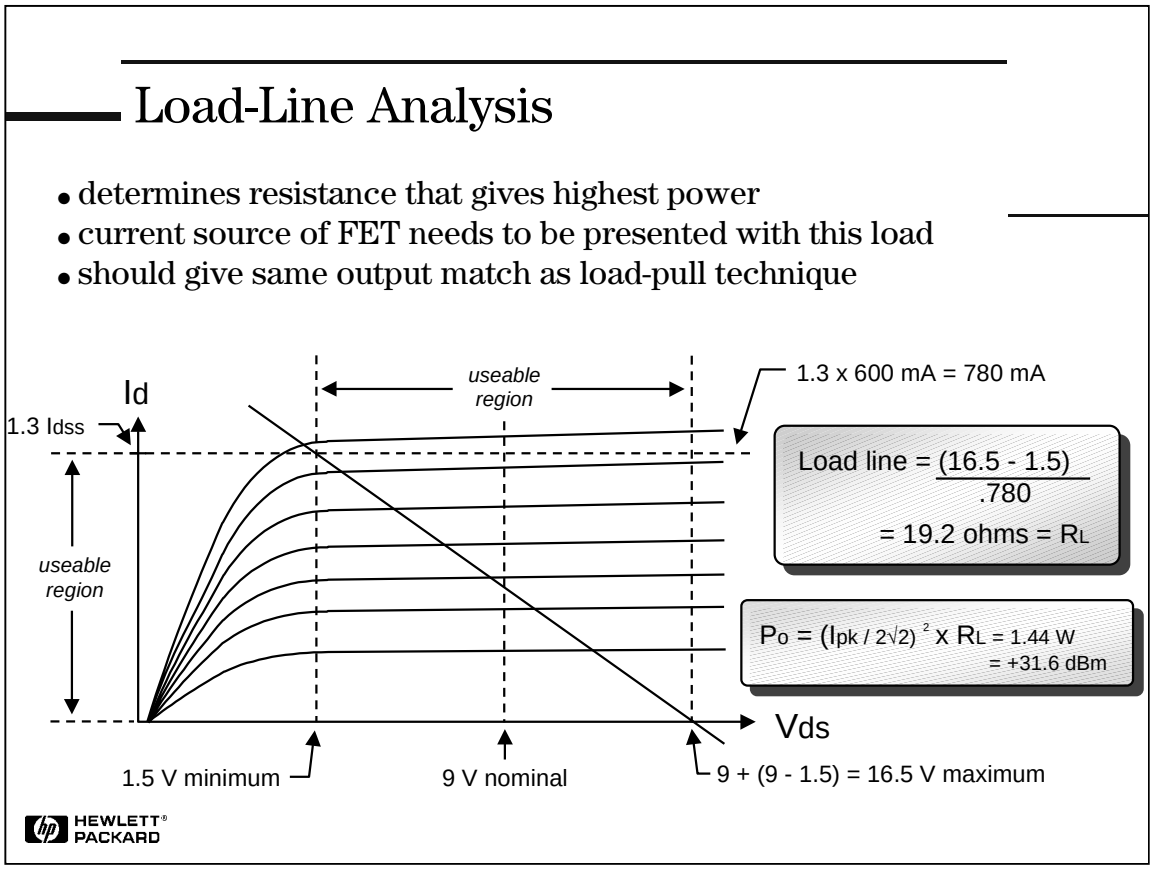
Slide #78



A load-line analysis is an alternate technique for finding the optimum impedance to present to the output stage of the power amplifier. If we look at the I-V curves for a FET, we see that there is a useable region for both drain current and drain-to-source voltage. For drain current, we generally use the region between 0 and 1.3 x Idss (this is somewhat arbitrary). To keep the output voltage within the (mostly) linear region of the FET, we have to avoid the steep-sloped areas of the I-V curves. For the FET we chose, this meant restricting the minimum drain-to-source voltage to 1.5 V. Since the manufacturer recommended a nominal bias point of 9 V, the upper voltage of the output waveform would be 9 + (9 - 1.5) = 16.5 V. Drawing a line between these two points (1.5 V / 780 mA and 16.5 V / 0 mA) and calculating the slope results in a resistance of 19.2 ohms. This is the impedance value that we must present to the ideal current source in the FET.

We can also calculate the theoretical maximum output power under these conditions since we know the bias point and the load impedance. In this example, the maximum output power is +31.6 dBm. This value matches fairly closely the value the manufacture specifies for the maximum output power of the FET, so we know we have arrived at a reasonable value for load resistance.

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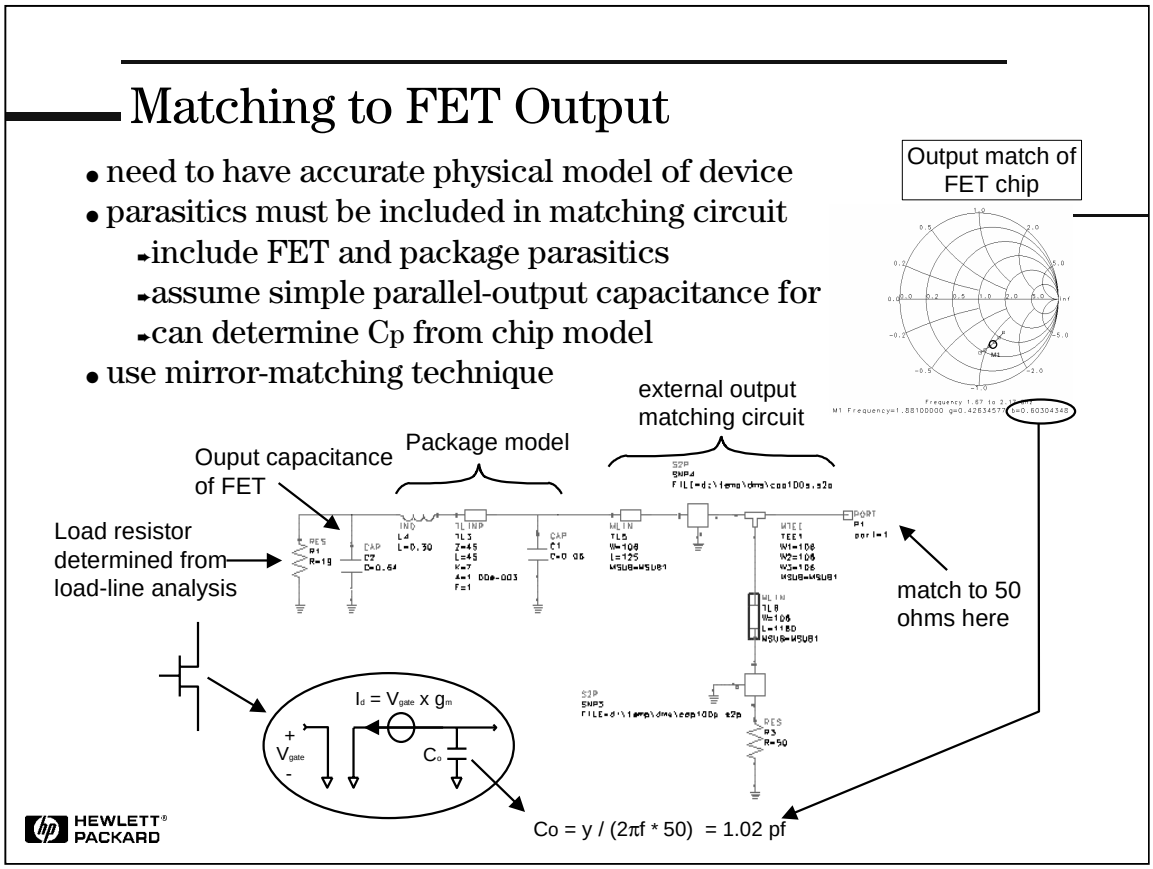
Slide #79



Now that we know what load resistance the current source of the FET should drive into, we must design a matching circuit that will transform 50 ohms to this value. However, we must include all of the reactances that are present in the circuit, including the output reactance of the FET itself (generally capacitive), and the parasitics of the package. Package parasitics can be hard to come by. Some manufacturers (like Avantek) give information in their catalogs about package parasitics. The output reactance of the FET can be determined approximately from s22 of the device. We can assume a simple model for the FET – namely that the output looks like an ideal series current source and a shunt capacitance. We can convert the imaginary part of the output admittance (which can be read from an admittance Smith chart) into an equivalent capacitance. This capacitance then becomes part of our matching circuit.

The output match used for our example amplifier was derived from a single transmission-line tuning stub. A very useful way to optimize the output network is to use the mirror technique. This is accomplished by inserting a resistor of the value we want the current source to see (19 ohms in this case) at the FET side of the matching circuit, and then optimizing the stub lengths until we achieve a good 50-ohm match at the output side of the matching circuit. For the actual circuit, the 19-ohm resistor is removed since a 50-ohm load would transform precisely to this value.

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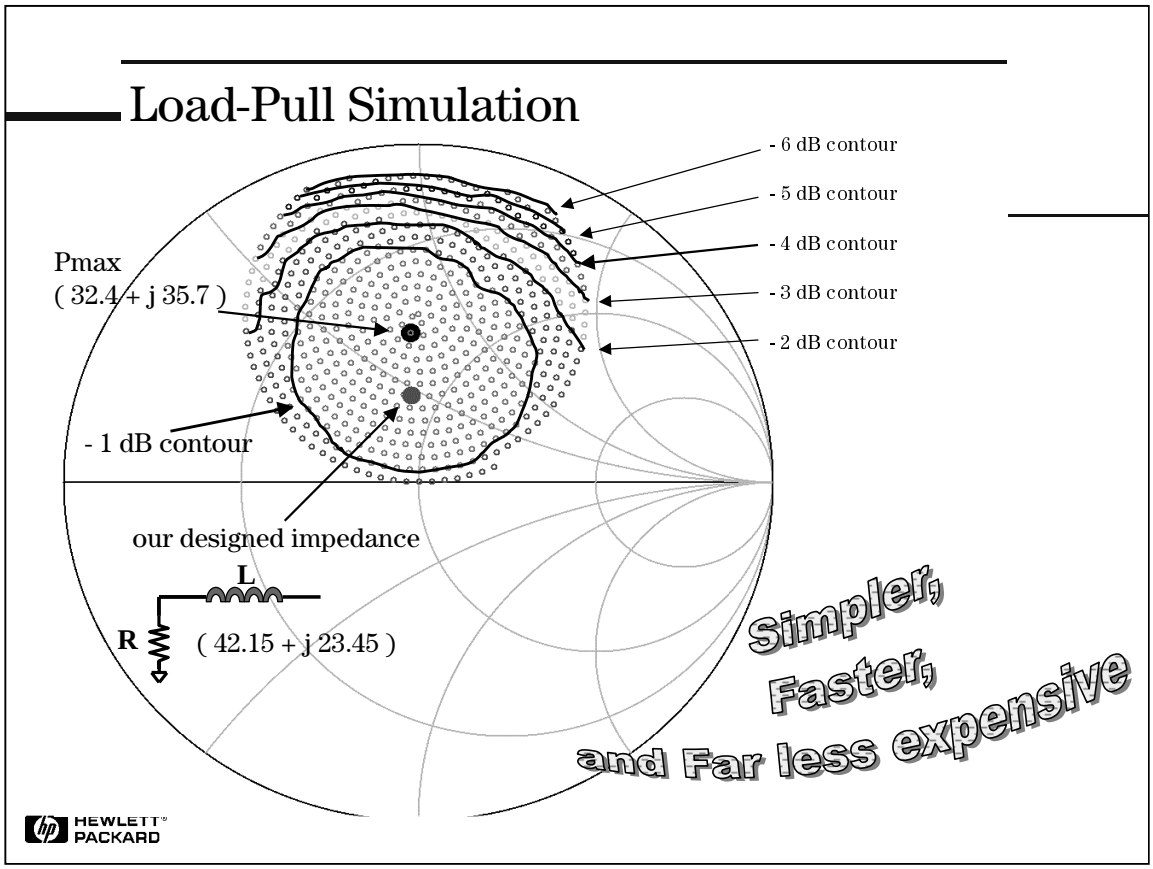
Slide #80



The easiest alternative to either a load-line analysis or a load-pull measurement is a load-pull simulation. Load-pull simulation is easier, faster, and usually more accurate than the load-line analysis. Load-pull simulation is simpler, quicker and far less expensive than a load-pull measurement system.

EDA tools, such as the HP Advanced Design System, can perform a load-pull analysis. An accurate non-linear model of the DUT is needed to perform an accurate analysis. Illustrated above is the load-pull analysis of the FET device used in the power stage of our designed power amplifier.

For each specific impedance value, the HP Advanced Design System evaluates the corresponding output power level and displays it as a colored dot on the Smith Chart. As shown, the boundaries of these colored dots form the power contours.

For our power amplifier, we initially designed for the maximum output power. However, in order to ensure stability, we ended up trading off about 0.5 dB of output power. Our final design impedance is as shown above.

Now, let's look at how we designed the matching network from this load-pull simulation data.

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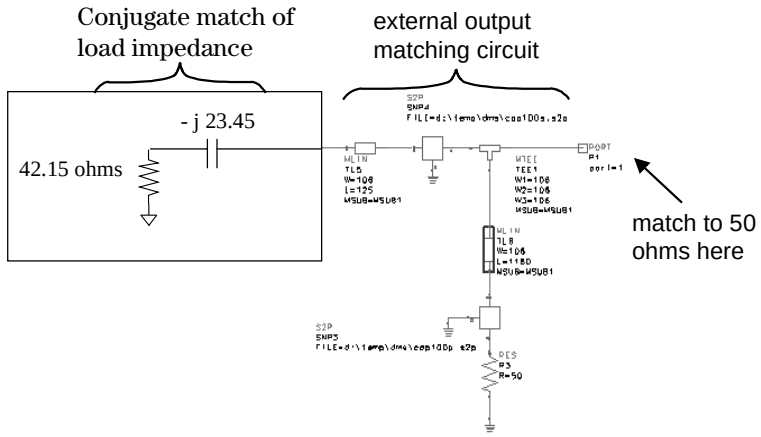
Slide #81

Using data from the load-pull simulation to design a matching network

- No need to model parasitics of FET or package
- Use mirror-matching technique
- Easier and faster



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The load-pull simulation gives us the load impedance value with which we should terminate our FET. The model used in the load-pull simulation is the packaged FET model, therefore, the resulting load impedance has parasitics of the FET and package automatically built in to the analysis. Since modeling parasitics is not required, the procedure for determining the matching circuit is much simpler and faster than using data from the load-line analysis. In general load-pull simulation, is more accurate than load-line analysis, provided that we have an accurate non-linear model for the amplifier. There are advanced measurement systems that can characterize active components, providing very accurate non-linear models. One such system is discussed in the "Measurement for Design -- Active Device Parameter Extraction" Section.

Again, we used the mirror-matching technique. We placed the conjugate of the load impedance on the FET side of the matching network and optimized for 50 ohms, as shown. After optimization, looking into the matching network from the FET side, you would see the desired load impedance of (42.15 +j 23.45) ohms.

The matching network is very similar to that obtained with the load-line analysis, but as described, the design is quicker, simpler, and much more time-efficient using data from a load-pull simulation.

Now, it is time to build our prototype.

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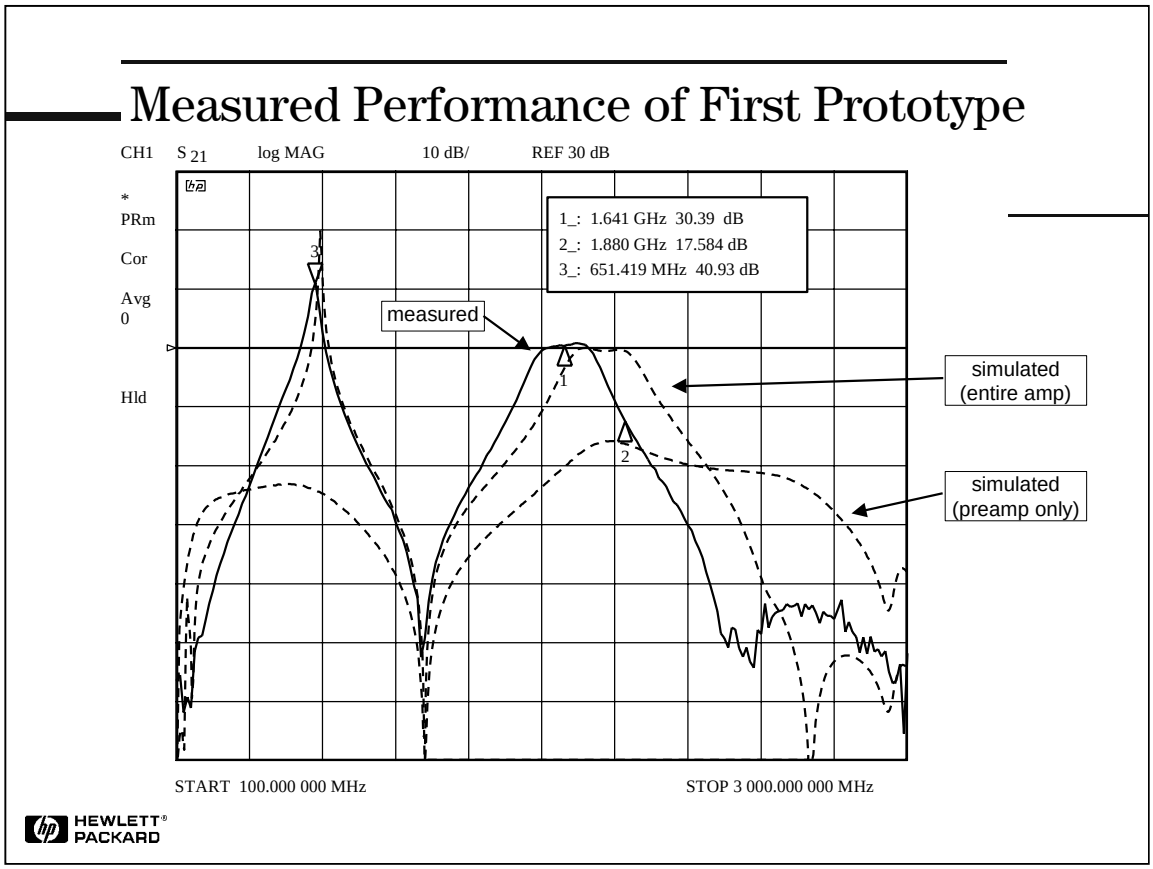
Slide #82



Here is the simulated and measured linear performance (S21) of our first amplifier prototype. Notice the huge gain peak around 650 MHz. This indicates that the amplifier will likely oscillate at this frequency (which it did!).

In this design, we had two designers: one for the driver stage (preamp) and the other for the power stage. Each circuit was simulated and its individual performance met circuit specifications. At an intermediate point, the designers did simulate their circuits together and the combined amplifier response looked fine. However, a few days remained before the final design due date, and therefore each designer continued to fine-tune his individual circuits. The two stages were not simulated together again before the final design was submitted for the first prototyping.

Had they been simulated together at this final stage, the HP Advanced Design System would have very accurately predicted that the two stages would interact quite significantly. As shown, ADS predicted a narrow-band high gain peak at around 650 MHz. At high frequencies, even very minor changes can result in dramatic effects. This example illustrates the importance of always verifying system performance, whether you are designing a relatively simple amplifier or a large, complex system.

Another problem is that the center frequency of the amplifier is about 240 MHz too low.

We have two significant deviations from expectations. Before we can begin to redesign our power amplifier, we must first modify our circuit design file so that simulated results match measured results. Once this match is achieved, we will have a more accurate circuit design file in which to improve our power amplifier design.

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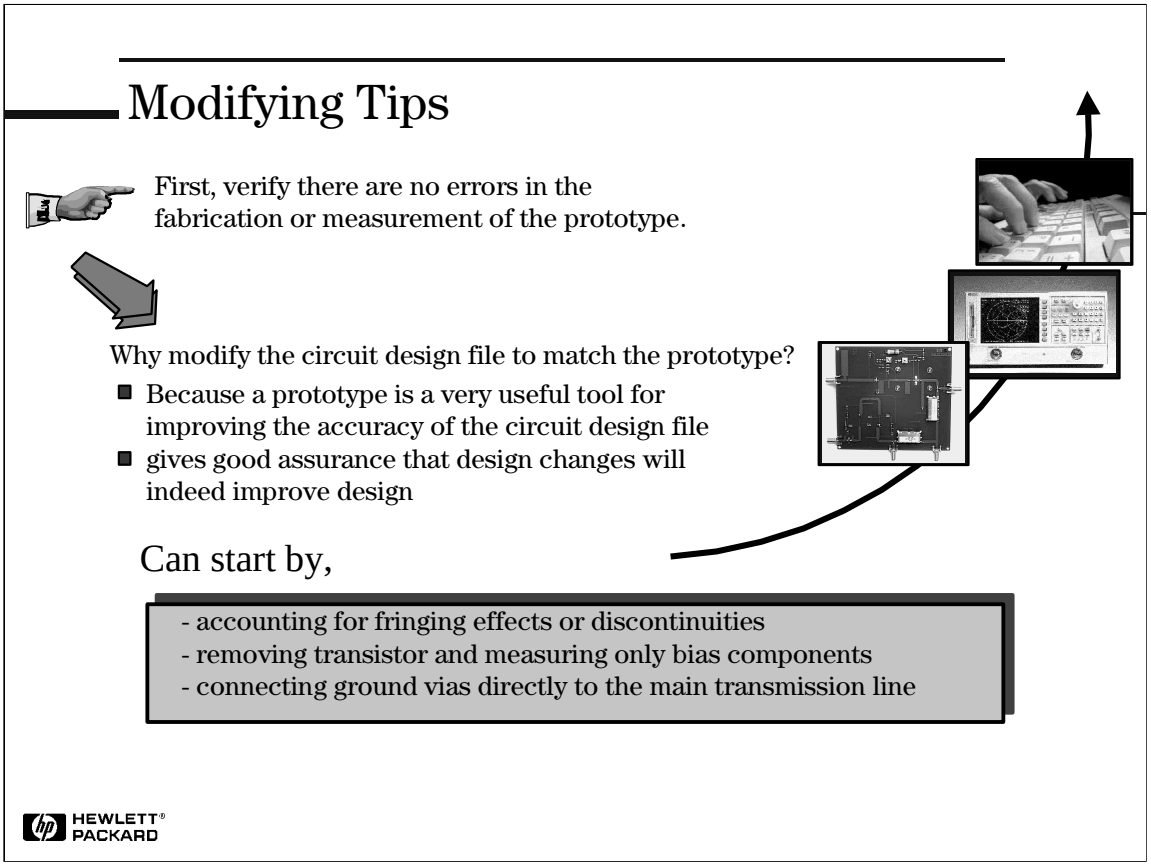
Slide #83



Before we make any changes to our circuit design file, we must first verify that no mistakes were made in the fabrication or measurement of our prototype. Once we are confident that the prototype has been built as intended, the prototype becomes a very useful tool for improving the accuracy of our circuit design file.

Any discrepancies in the measured and simulated results indicate that we need to improve the accuracy of our circuit design file. As shown in the slide, the recommended path is to build a physical prototype, measure its performance with a vector network analyzer, and then continue with design iterations on software. The measured data of the physical prototype is first used to create a more accurate circuit design file, before design refinements are added. The alternative route is to bypass the physical prototype and measurement stage, continuing to refine the design in software only. The risk of using this method is that without a verification check, via the physical prototype, you may be spending valuable time perfecting a less-than-accurate circuit design file.

You might start the matching process by accounting for fringing effects and discontinuities that were neglected in the first pass. Once you've changed all you can in the circuit design file and there's still no match, the next step is to make changes directly to the physical prototype. This will help you gain more insight. For example, you might remove a transistor on the physical prototype and measure the reflection response of the biasing circuitry. Do the same in the HP Advanced Design System, simulate the s_{11} response, and see if the two agree. If not, make changes in the circuit design file to try to match them. Or you might connect a ground via directly to the main transmission line in order to measure the parasitic inductance. You can use this measured data to properly model this parasitic effect in HP Advanced Design System.

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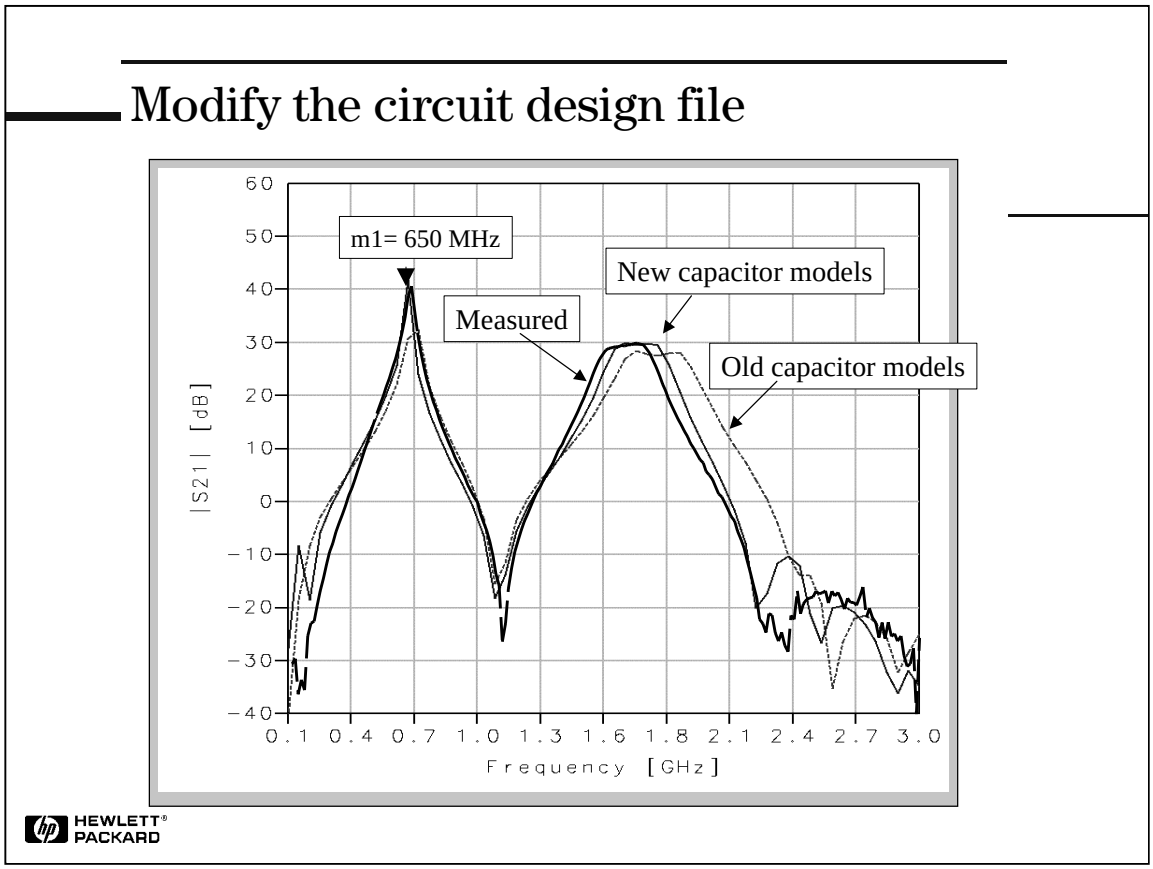
Slide #84



The next step of our design process is to modify our circuit design file so that simulated results match measured results. We were able to achieve the match by modifying the models of our measured capacitors. As shown, the new circuit design file produced simulated results that very closely agreed with our measured results.

However, we see that the match is not exact. This illustrates a typical trade-off that designers face: there's a law of diminishing returns that states that at some point the time required to further refine the circuit design file outweighs the expected increase in accuracy. Since the match was close enough, we decided to continue with our design refinement using this improved model.

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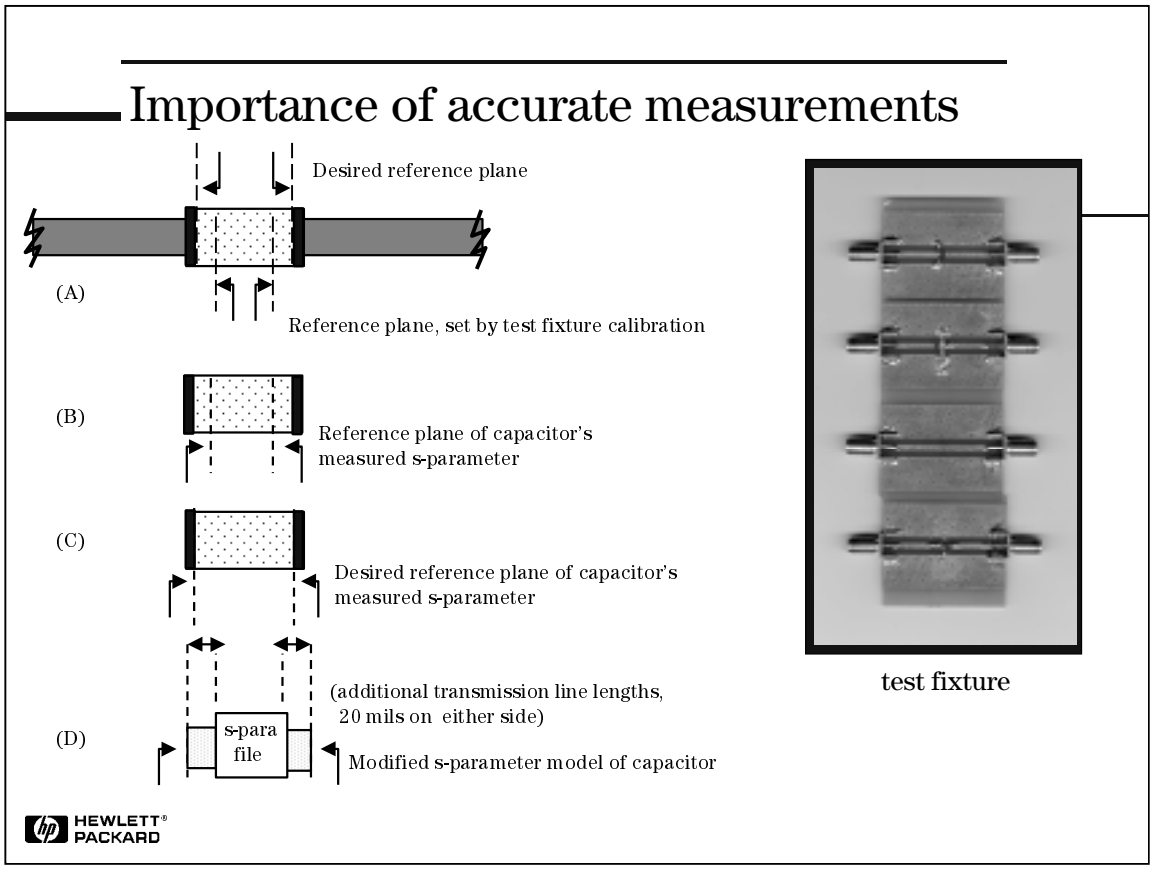
Slide #85



We used measured s-parameter data as models for our capacitors. We chose to measure certain capacitors since there were specific transmission lines that were very sensitive to dimension. The dimensions of the capacitors were comparable to those of these critical transmission lines.

In order to accurately measure these capacitors, an in-fixture calibration was performed. Shown above, the test fixture contains the required in-fixture SOLT (short, open, load, through) standards used in the calibration. The bottom connection of the test fixture provided the point at which to measure the capacitors. The test fixture will be discussed in more detail later.

The reference plane is set by the short circuit. Therefore, the two transmission lines of the bottom connection should each be equal to the length of the short circuit, with adequate space in between to connect a capacitor. Unfortunately, an error was made in the fabrication of the lengths of these transmission lines. Each transmission line length was short by about 20 mils.

Therefore, on either side of the transmission lines, the reference plane extended 20 mils past the desired reference point, as shown in Figure (A). The reference plane used to measure the capacitor's s-parameters is as shown in Figure (B). These are the s-parameters we used to represent the capacitors in our initial circuit design file. As shown in Figure (C), the desired reference plane is at the endpoints of the capacitor. If we had used this desired reference plane, then the s-parameters would have contained the correct phase (or electrical length) information. In order to compensate for this offset of the reference plane, we added additional 20 mils of transmission lines on each side of the s-parameter data, as illustrated in Figure (D). This is essentially the same as adjusting the phase (or electrical length) information of the s-parameter data.

An alternative technique is to use the network analyzer feature called "port extension" to reset the reference plane to the desired point. Port extension is discussed further in the "Measurement for Design" section.

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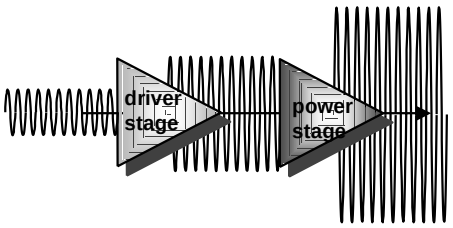
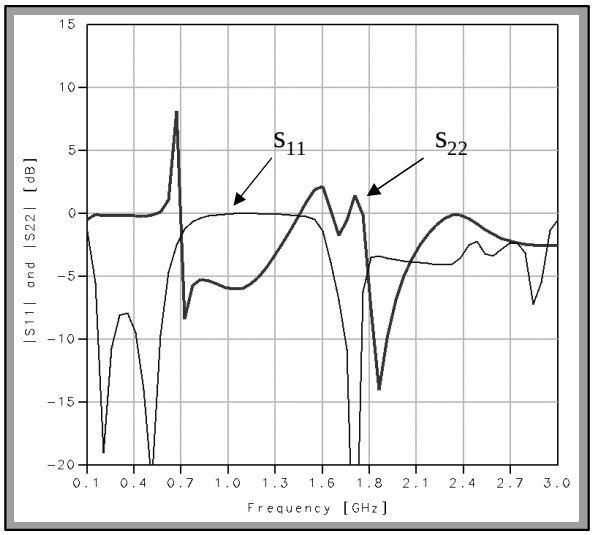
Slide #86

Design Refinement



2 gain stages, oscillation can be caused by:
.. driver stage
.. power stage
.. both stages

----> Need to separate each stage and examine



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At this point, we were confident that we had an accurate circuit design file and that simulated results would agree with measured results fairly well.

Now it is time to improve the oscillation problem. As shown, the amplifier is potentially unstable as indicated by $s_{22} > 0$ dB.

There are two gain stages in the amplifier. Oscillation could be caused by the first, second, or the combination of the two (i.e. if one stage is conditionally stable and the other stage presents a load in its unstable region). We needed to separate each stage and examine its s-parameters, stability factor, and source and load stability circles.

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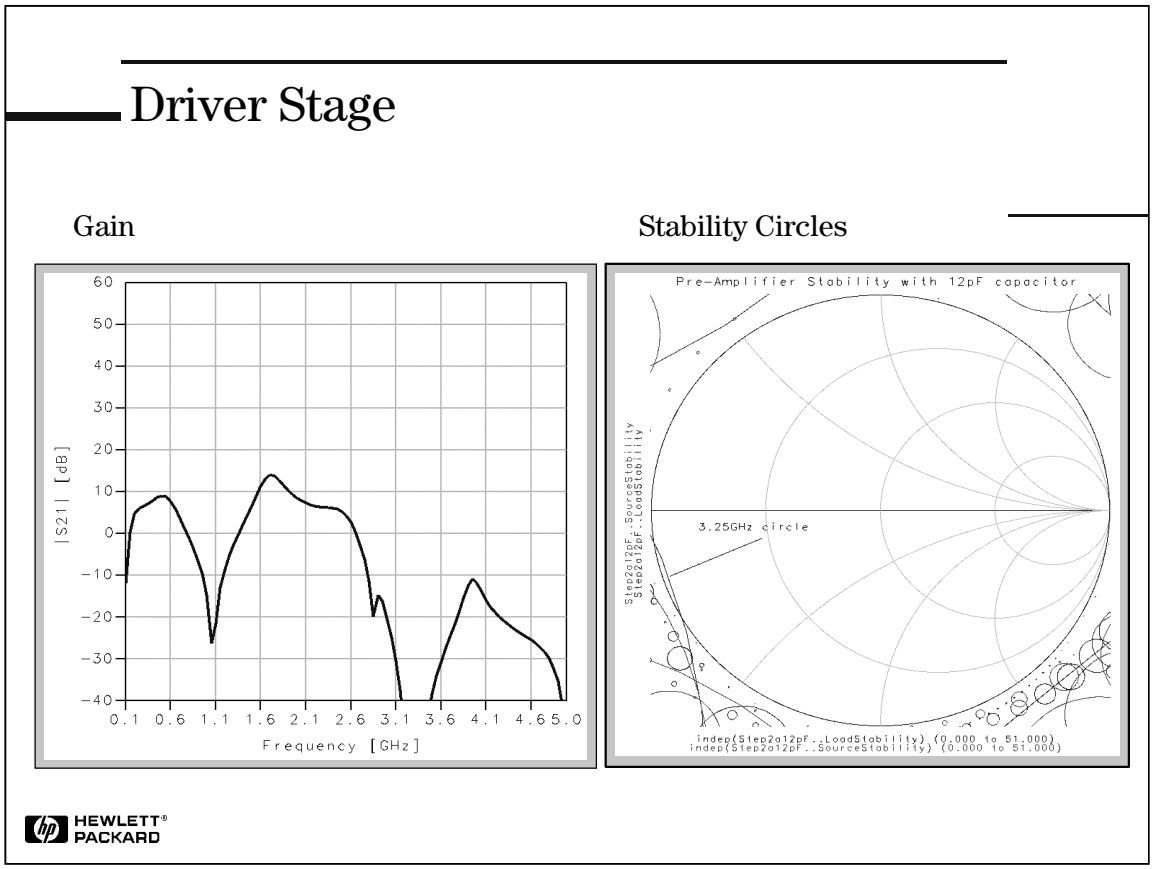
Slide #87



We began by looking at the driver stage. The first plot shows that the driver stage has an acceptable gain response.

The second plot shows stability circles for the driver stage's source and load impedances. A stability circle maps the boundary between stability and instability. Once the stability circles are draw, the next step is to determine which side of the circle is stable. Typically, the side that contains the center of the Smith Chart is the stable side.

The stability circles indicate that the driver stage is unconditionally stable, except at 3.25 GHz. At this frequency, the design is potentially unstable, but only over a very small range of impedances. Note that it is important that stability analysis be carried out over a much wider frequency range than the actual bandwidth of the amplifier. Basically, we need to ensure stability over the entire range for which the amplifier has significant gain.

The driver stage looks acceptable, although the low frequency gain could be further reduced. The center frequency also needs to be re-adjusted at a later point. From here, we left the driver stage and continued on to the power stage.

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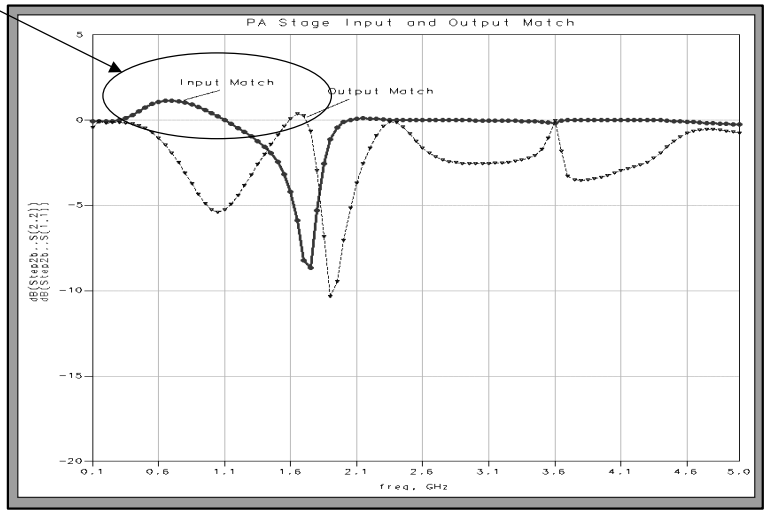
Slide #88

Power Stage: Input & Output Match

Potentially Unstable



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Another way of analyzing stability is to look at input and output match. Here are the power stage's input and output match. Since the s11 and s22 responses are greater than 0 dB, the power stage is potentially unstable at these lower frequencies. We needed to stabilize the power stage.

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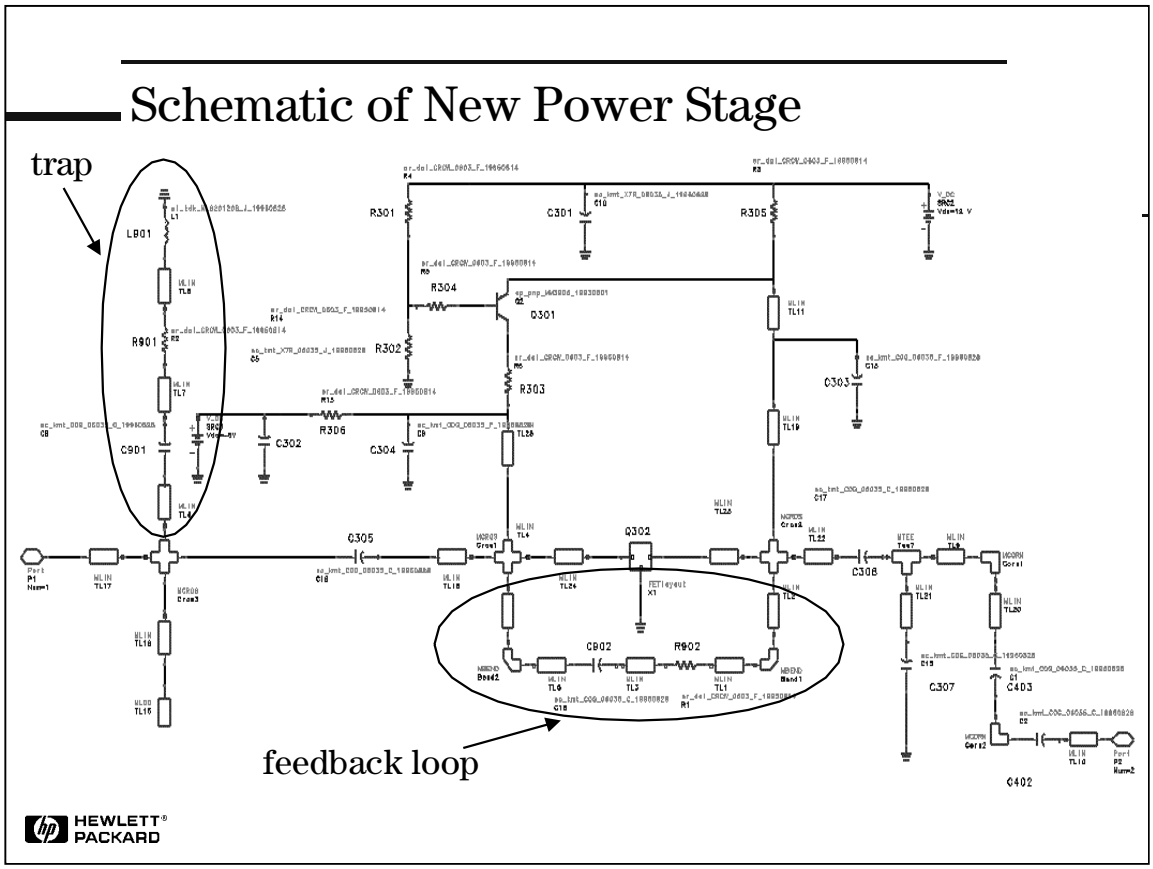
Slide #89



To make this stage more stable, we implemented a feedback loop, a series LCR resonance trap, and changes to certain capacitors in order to improve input and output match.

The feedback loop was designed such that the feedback signal will add out-of-phase with the input signal to the FET. The feedback loop consisted of a capacitor, resistor and transmission lines. The capacitor influences the phase of the feedback signal. The resistor affects the gain and stability. If the resistor is too small, this reduces the gain too much. If the resistor is too large, gain is not significantly reduced and, correspondingly, stability is not significantly improved. Here, we traded off some gain for increased stability at the lower frequencies.

With this new design, the power stage is much more stable. The oscillation problem is reasonably resolved. Using this improved circuit design file, we re-tuned the matching circuits of both the pre-amp and power stage for a center frequency of 1.88 GHz. The redesign of the power amplifier is completed!

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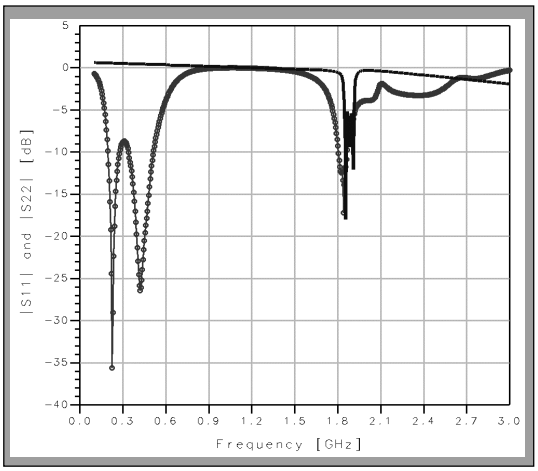
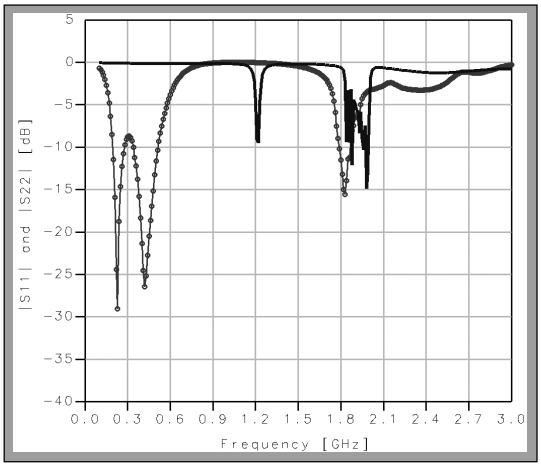
Slide #90

Completed amplifier's s_{11} and s_{22} responses with duplexer filter connected

Analysis using filter s-parameter file, obtained over a narrow frequency band



Analysis using filter s-parameter file, obtained over an appropriately wide frequency band



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An important step before fabricating the final prototype is to simulate all parts together to ensure that there will be no unexpected interactions. The power amplifier is followed by the 1.88 GHz duplexer filter. This filter will appear as a highly-reflective load with rapidly varying reactance at the out-of-band frequencies. It's particularly important to ensure this termination does not cause the amplifier to oscillate.

The first plot shows that the s_{11} response looks fine, but s_{22} is larger than 0 dB at the lower frequencies. Does this mean we need to refine our design further? Thankfully no. In this analysis, we used measured data for the filters which only went down to 1.67 GHz. The other necessary data points were extrapolated. There's no way to predict precisely how the data will behave outside the measured range. We needed to use actual measured filter data that covered the entire frequency range of interest.

In the second plot, the analysis was performed using actual measured filter data that extended down to the lower frequencies. Now, s22 is less than 0dB throughout the frequency range and we are confident that the amplifier is stable when terminated with the duplexer filter.

This example illustrates the importance of using data files that cover the entire frequency range of analysis in order to achieve the most accuracy.

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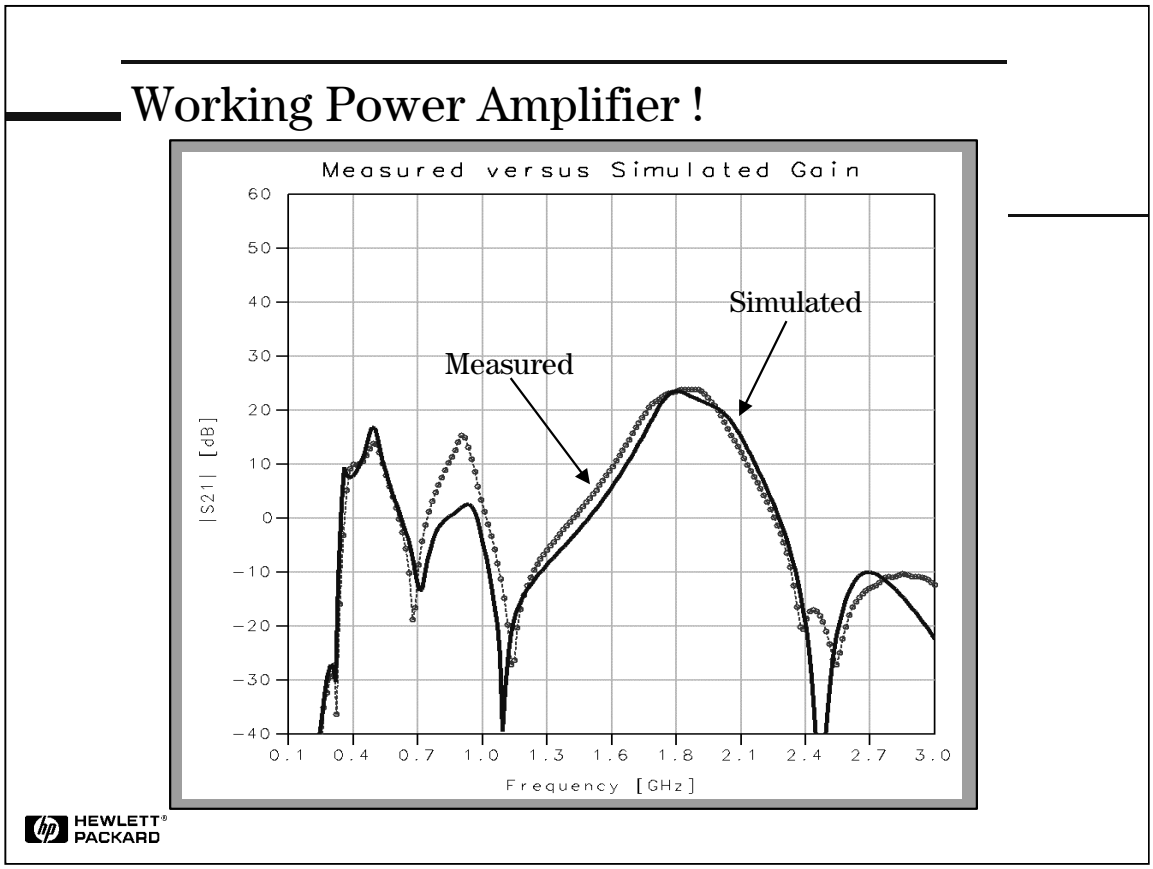
Slide #91



Upon fabrication of the second prototype, we found that measured and simulated results agreed fairly well. The gain at the lower frequencies was significantly reduced. The center frequency was successfully re-adjusted to the desired 1.88 GHz.

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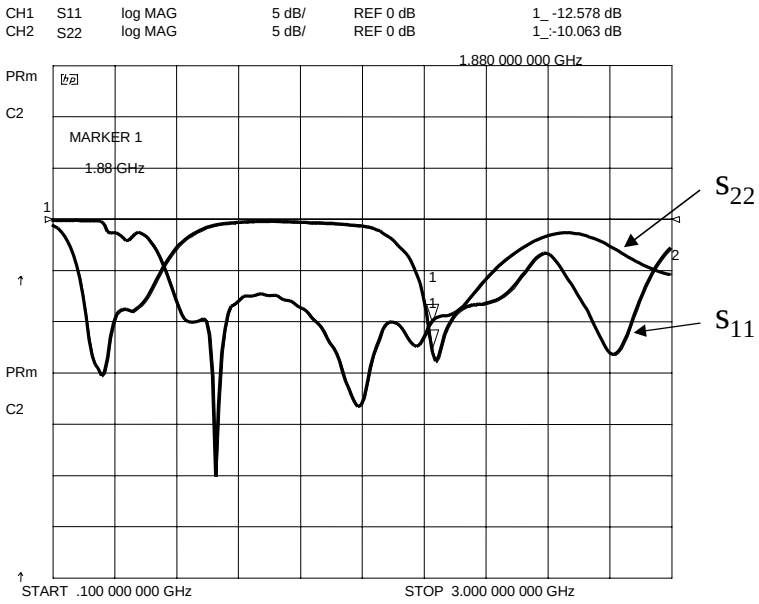
Slide #92

Input and Output Match



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Measurements of the input and output matches reveal that the power amplifier is stable.

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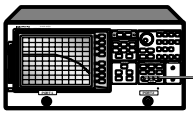
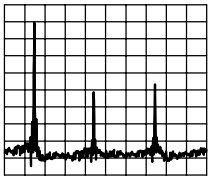
Slide #93

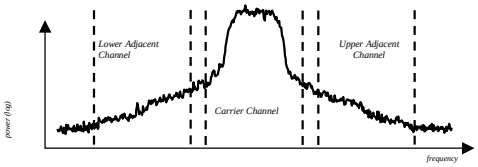
Characterizing Nonlinear Behavior

Power amplifiers require additional measurements to characterize nonlinear behavior

- power sweeps (using network analyzer)
  - gain compression
  - AM to PM conversion
- single-tone harmonic
  - second harmonic
  - third harmonic
- multi-tone intermodulation
  - third-order intercept using two tones
  - high-order intermodulation using many carriers
- digital modulation
  - adjacent-channel power







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While we have only shown the linear performance of the amplifier so far, we must also characterize its nonlinear behavior.

Typically, a vector network analyzer is used for linear measurements, however, with its power sweep capability, it can also perform non-linear measurements, such as gain compression or AM to PM conversion. While we will discuss gain compression in more detail, a description of AM to PM conversion measurements can be found in the Appendix Section. AM to PM conversion can also be simulated in HP Advanced Design System.

Other non-linear characterizations include harmonic and intermodulation measurements, typically performed using a spectrum analyzer. For more complete characterization of nonlinear behavior, we would need more complex stimulus (for example, multiple carriers or a digitally-modulated carrier). Digital modulation measurements will be discussed in much more detail later.

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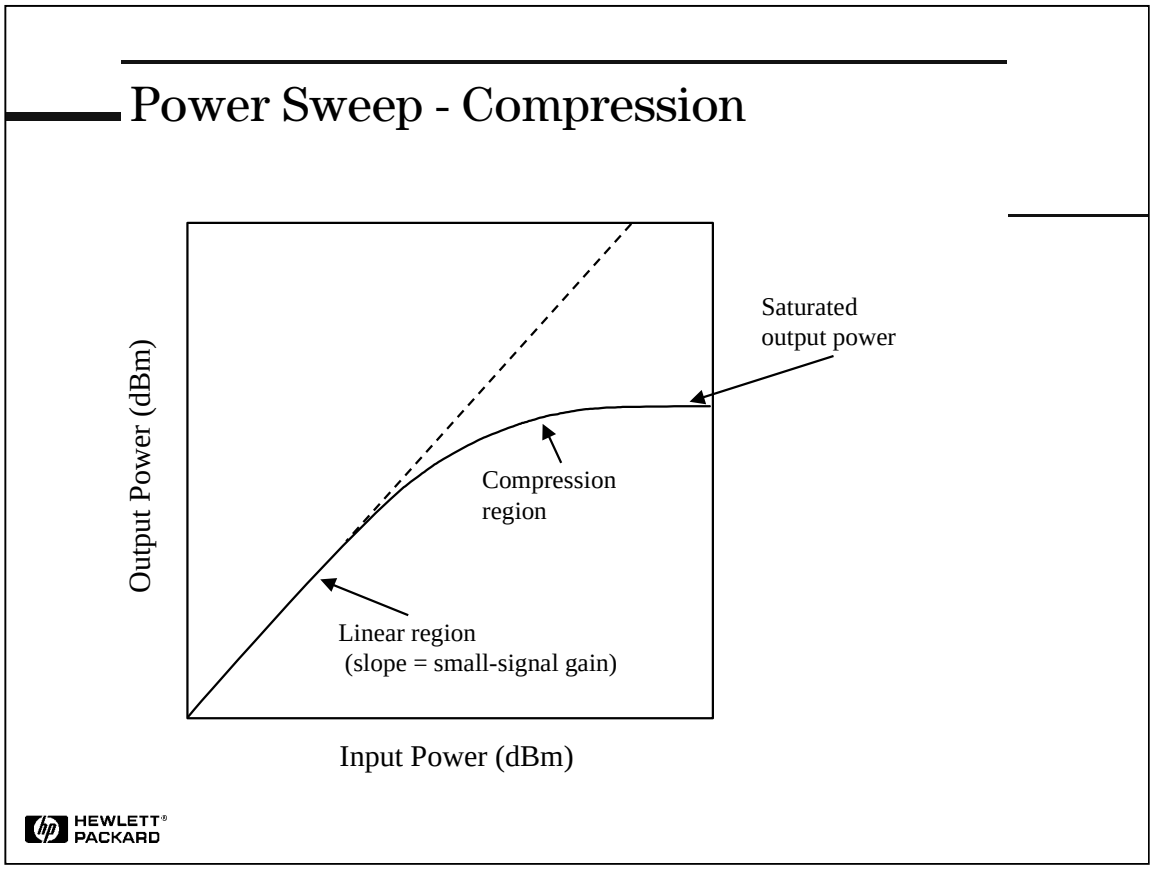
Slide #94



Many network analyzers have the ability to perform power sweeps as well as frequency sweeps. Power sweeps help characterize the nonlinear performance of an amplifier. Shown above is a plot of an amplifier's output power versus input power at a single frequency. Amplifier gain at any particular power level is the slope of this curve. Notice that the amplifier has a linear region of operation where gain is constant and is independent of power level. The gain in this region is commonly referred to as small-signal gain. At some point as the input power is increased, the amplifier gain appears to decrease, and the amplifier is said to be in compression. Under this nonlinear condition, the amplifier output is no longer sinusoidal -- some of the output power is present in harmonics, rather than occurring only at the fundamental frequency.

As input power is increased even more, the amplifier becomes saturated, and output power remains constant. At this point the amplifier gain is essentially zero (in linear terms, but negative infinity in logarithmic terms), since further increases in input power result in no change in output power. Saturated output power can be read directly from the above plot.

To measure the saturated output power of an amplifier, the network analyzer must be able to provide a power sweep with sufficient output power to drive the amplifier from its linear region into saturation. A preamp at the input of the amplifier under test may be necessary to achieve this.

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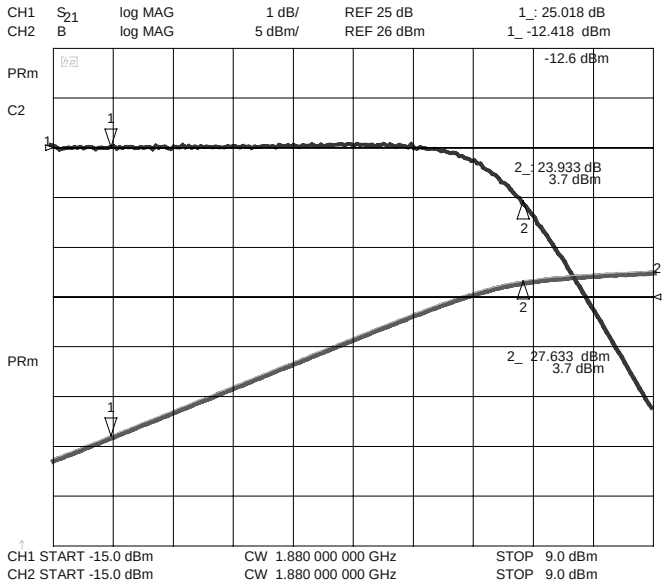
Slide #95

Measured Gain Compression



1 dB compression: input power resulting in 1 dB ***drop*** in gain

- ratioed measurement
- output power available (non-ratioed measurement)
- use power-meter calibration for best accuracy

1dB Compression Results:
Input power: 3.7 dBm Output power: 27.633 dBm Gain,1dB : 23.933 dB

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The most common measurement of amplifier compression is the 1-dB-compression point, defined here as the input power1 which results in a 1-dB decrease in amplifier gain (referenced to the amplifier's small-signal gain). The easiest way to measure the 1-dB-compression point is to directly display normalized gain (B/R) from a power sweep. The flat part of the trace is the linear, small-signal region, and the curved part on the right side corresponds to compression caused by higher input power. As shown above, the 1-dB-compression point of our PCS-band power amplifier is 3.7 dBm (tested at a CW frequency of 1.88 GHz).

It is often helpful to also know the output power corresponding to the 1-dB-compression point. Using the dual-channel feature found on most modern network analyzers, absolute power and normalized gain can be displayed simultaneously. Display markers can read out both the output power and the input power where 1-dB-compression occurs. Alternatively, the gain of the amplifier at the 1-dB-compression point can simply be added to the 1-dB-compression power to compute the corresponding output power. As seen above, the output power at the 1-dB-compression point is 3.7 dBm + 23.933 dB = 27.633 dBm. The absolute power measurement in channel two indicates 27.633 dBm. A more accurate absolute power reading could be obtained by performing a power-meter calibration of the network analyzer.

It should be noted that the power-sweep range needs to be large enough to ensure that the amplifier under test is driven from its linear region into compression. Modern network analyzers typically provide power sweeps with 15 to 20 dB of range, which is more than adequate for most amplifiers. As illustrated above, wider power ranges can also be achieved. It is also very important to sufficiently attenuate the output of high-power amplifiers to prevent damage to the network analyzer's receiver. For our example, a 20 dB attenuator was placed at the output of the amplifier.

[1] The 1 dB compression point is sometimes defined as the output power resulting in a 1-dB decrease in amplifier gain (as opposed to the input power).

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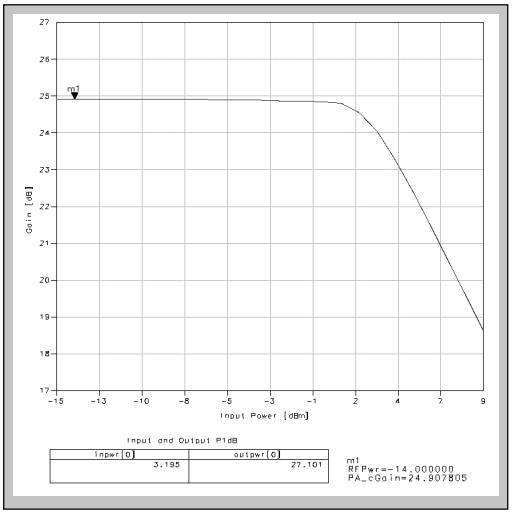
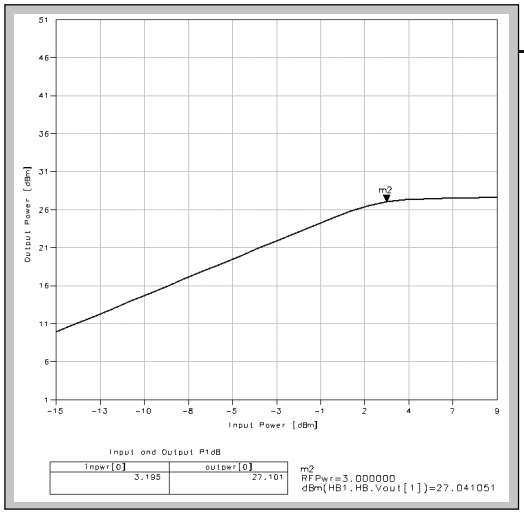
Slide #96

Simulated Gain Compression





1dB Compression Results:
Input power: 3.195 dBm **Output power: 27.101 dBm** **Gain, 1dB : 23.907 dB**

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The simulated gain compression results matched very closely with the measured results.

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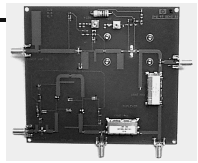
Slide #97

Amplifier Specification Sheet

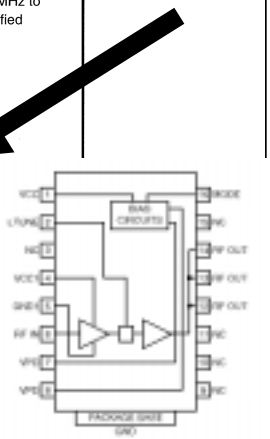


RF MICRO·DEVICES

Preliminary **RF2152**

DUAL-MODE CDMA/AMPS OR TDMA/AMPS 3V POWER AMPLIFIER

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.5V, Freq=824MHz to 849MHz unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849		MHz	
		877-925		MHz	
Linear Gain	28	30	33	dB	Pout=28dBm
Second Harmonic (including second harmonic trap)	-32	-38	-42	dBc	
Max CW Output Power	31	31.5	32	dBm	
Total Efficiency (AMPS mode)	45	50	60	%	
Maximum Linear Output Power (CDMA Modulation)	28	28.5	29	dBm	Tuned for CDMA
Total Linear Efficiency	30	35	38	%	
Adjacent Channel Power Rejection	-44	-46	-50	dBc	ACPR @ 885kHz
Adjacent Channel Power Rejection	-56	-58	-62	dBc	ACPR @ 1980kHz
Input VSWR		< 2:1			
Output Load VSWR			10:1		No oscillations



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We've simulated and measured the traditional amplifier specifications such as gain, output match, and 1 dB compression, but if we were going to use this amplifier in a digital communication application, what additional simulation and measurements should we make? Above is an example of a specification sheet for an amplifier used in a Code Division Multiple Access (CDMA) application. This manufacturer specifies gain, input and output match, but they also specify the output power under CDMA modulation and something called adjacent channel power rejection (ACPR). Before we dive into the simulation and measurement of digital modulation, lets first review the basics of digital modulation.

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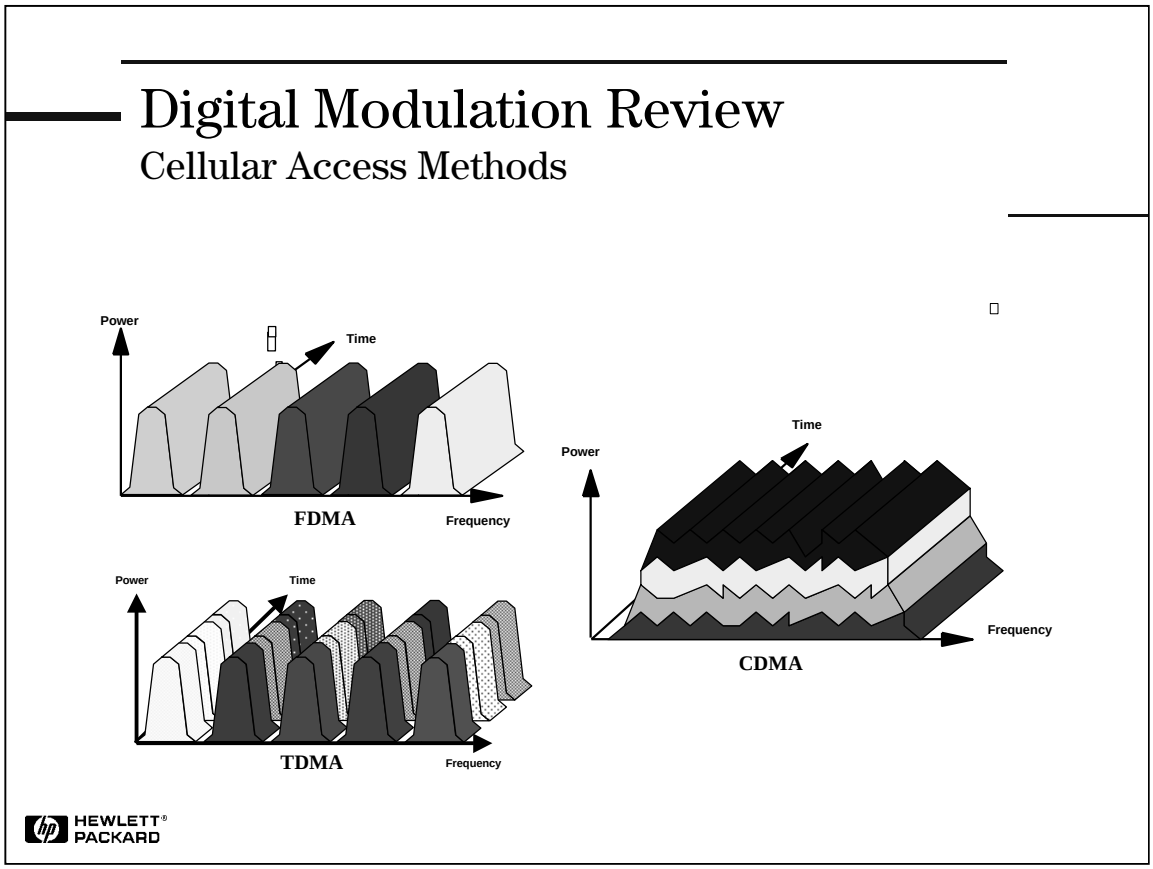
Slide #98



The first piece of the digital communication puzzle is multiplexing (sometimes called channelization). Multiplexing is used to separate different users of the spectrum. Most communications systems use a combination of frequency, time, code, and geography multiplexing.

Frequency division multiple access (FDMA) splits the available frequency band into smaller fixed frequency channels. Each transmitter or receiver uses a separate frequency. This technique has been used since around 1900 and is still in use today. Transmitters are narrowband or frequency-limited. A narrowband transmitter is used along with a receiver that has a narrow-band filter so that it can demodulate the desired signal and reject unwanted signals, such as interfering signals from other radios.

Time-division multiplexing involves separating the transmitted signals in time so that they can share the same frequency. The simplest type is time division duplex (TDD). This multiplexes the transmitter and receiver on the same frequency. TDD is used, for example, in a simple two-way radio where a button is pressed to talk and released to listen. This kind of time division duplex, however, is very slow. Modern digital radios like CT2 and DECT use TDD but they multiplex hundreds of times per second. Time division multiple access (TDMA) multiplexes several transmitters or receivers on the same frequency. TDMA is used in the GSM digital cellular system and also in the US NADC-TDMA system.

CDMA is an access method where multiple users are permitted to transmit simultaneously on the same frequency. Frequency division multiplexing is still performed but the channel is 1.23 MHz wide. In CDMA, a single user's channel consists of a specific frequency combined with a unique code. CDMA also uses sectored cells to increase capacity. One of the major differences in access is that any CDMA frequency can be used in all sectors of all cells. The correlative codes allow each user to operate in the presence of substantial interference.

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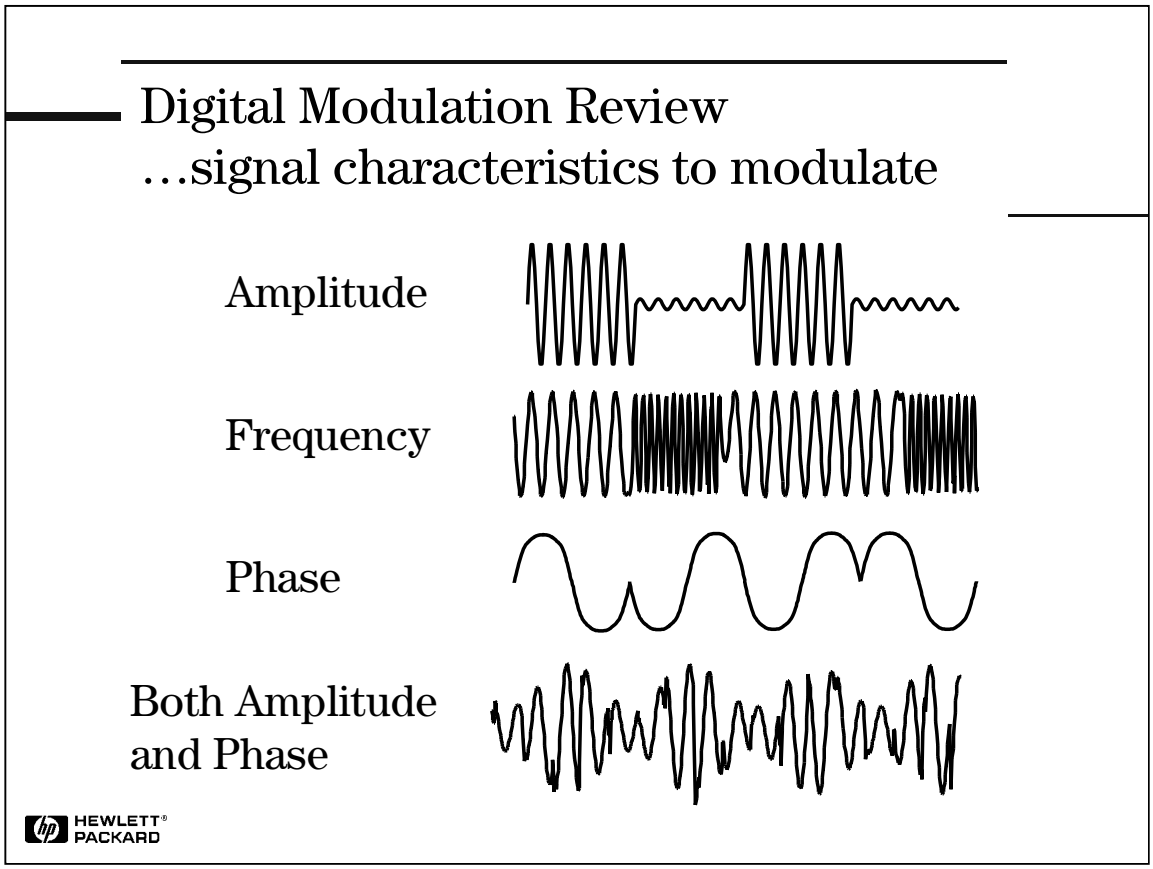
Slide #99



The only difference between analog modulation and digital modulation is that digital modulation restricts the modulating baseband signal to discrete states rather than allowing the modulating signal to take on any value between a maximum and a minimum value.

When AM, FM or PM are used in a digital modulation scheme the names become ASK, FSK and PSK. The SK stands for shift keying and is derived from the telegraph key. The modern use implies shifting between discrete states. These discrete states are created by the digitizing of voice using an analog to digital (A/D) converter.

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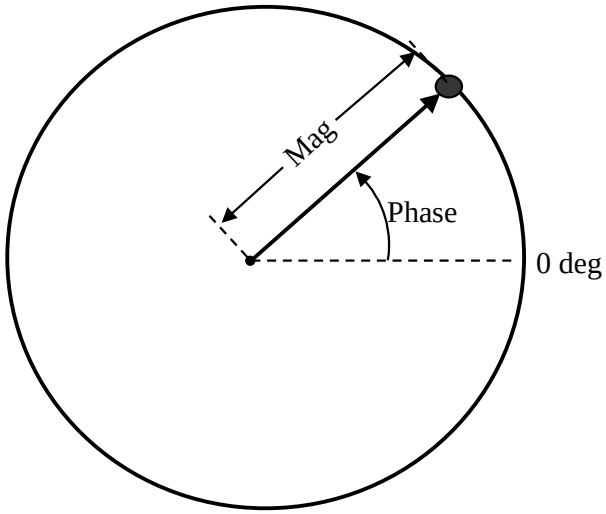
Slide #100

Digital Modulation Review

Polar Display: Magnitude & Phase Represented Together



- Magnitude is an absolute value
- Phase is relative to a reference signal

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A simple way to view amplitude and phase is with the polar diagram. The carrier becomes a frequency and phase reference and the signal is interpreted relative to the carrier. The signal can be expressed in polar form as a magnitude and a phase. The phase is relative to a reference signal, the carrier in most communication systems. The magnitude is either an absolute or relative value. Both are used in digital communication systems. Polar diagrams are the basis of many displays used in digital communications.

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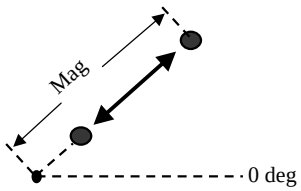
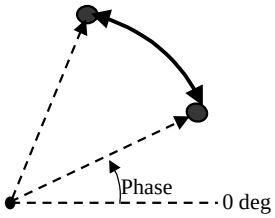
Slide #101

Digital Modulation Review

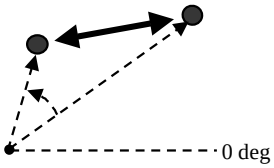
Signal Changes or Modifications



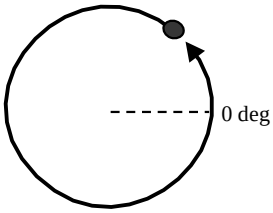
Magnitude Change



Phase Change



Both Change



Frequency Change

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This figure shows different forms of modulation in polar form. Magnitude is represented as the distance from the center and phase is represented as the angle. Amplitude modulation (AM) changes only the magnitude of the signal. Phase modulation (PM) changes only the phase of the signal. Amplitude and phase modulation can be used together. Frequency modulation (FM) looks similar to phase modulation, though frequency is the controlled parameter, rather than relative phase. As we will see later, CDMA uses a form of phase modulation, and GSM uses a form of frequency modulation.

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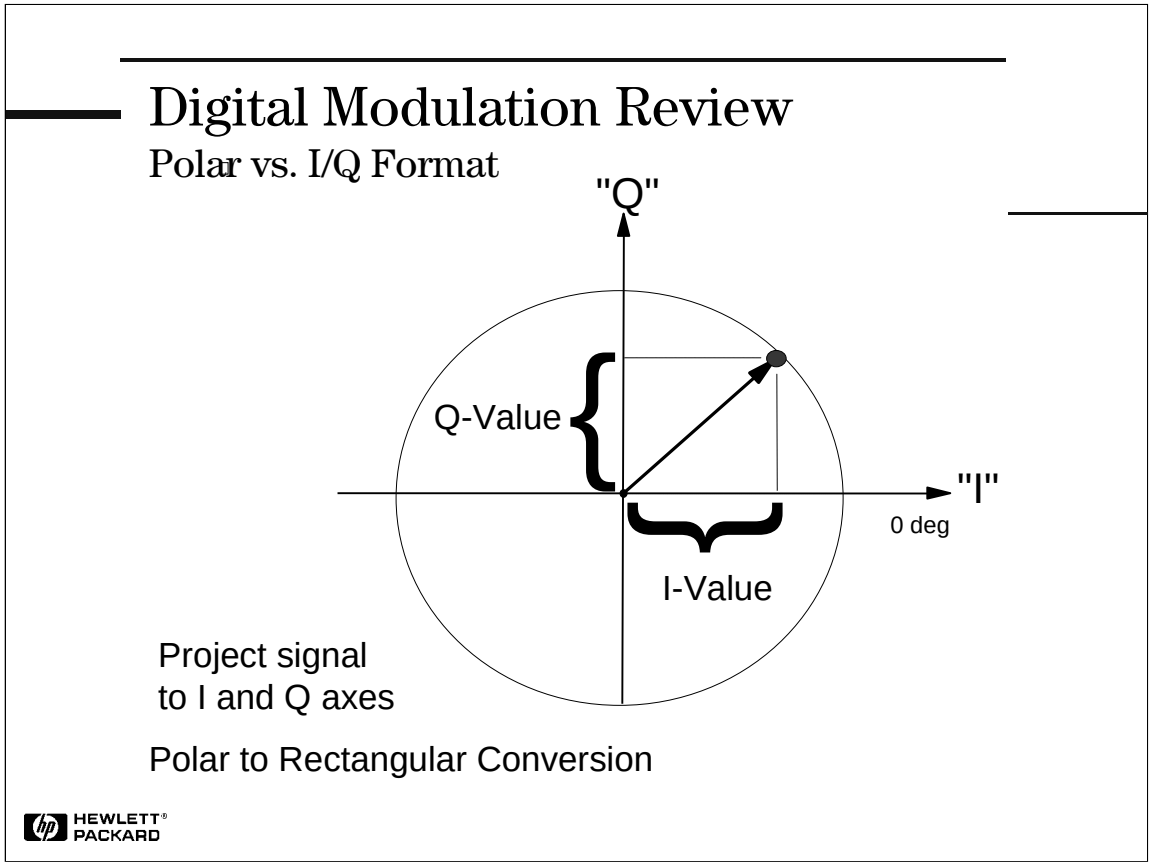
Slide #102



Polar diagrams are the basis of many displays used in digital communications, although it is common to describe the signal vector by its rectangular coordinates of I (In-phase) and Q (Quadrature). This is a rectangular representation of the polar diagram. On a polar diagram, the I axis lies on the zero degree phase reference, and the Q axis is rotated by 90 degrees. The signal vector's projection onto the I axis is its "I" component and the projection onto the Q axis is its "Q" component. I/Q diagrams are particularly useful because they mirror the way most digital communications signals are created using an I/Q modulator. Most digital modulation maps the data to a number of discrete points on the I/Q plane. These are known as constellation points. As the signal moves from one point to another, simultaneous amplitude and phase modulation usually results.

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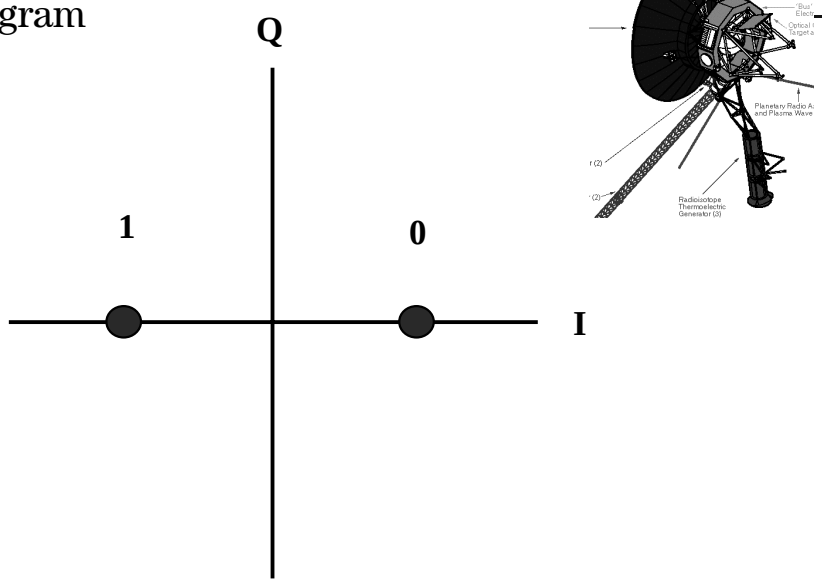
Slide #103

Digital Modulation Review

Binary Phase Shift Keying (BPSK)

I/Q Diagram



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Now that we have introduced the I/Q diagram, let's use it to review some digital modulation formats. One of the simplest forms of digital modulation is binary or binary phase shift keying (BPSK). One application where this is used is for deep space telemetry. The phase of a constant amplitude carrier signal moves between zero and 180 degrees. On an I and Q diagram, the I state has two different values. There are two possible locations in the state diagram, so a binary one or zero can be sent. The symbol rate is one bit per symbol. This is the form of digital modulation being used today to communicate with the Voyager deep space probe, which is more than two billion miles from earth. The advantage of BPSK is it's immunity to noise. The disadvantage of BPSK is it's bandwidth efficiency, it only transmits one bit per symbol. Now let's look at a format that gives us two bits per symbol.

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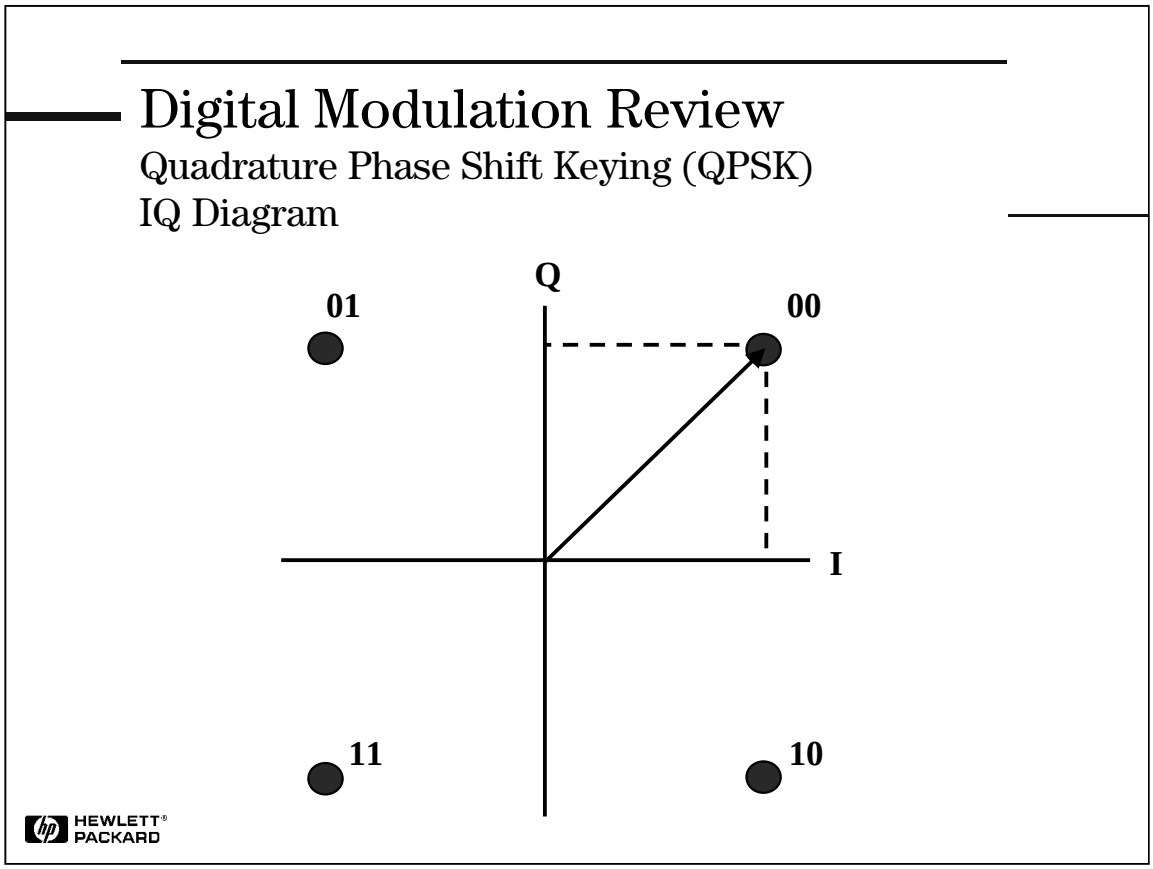
Slide #104



A more common type of phase modulation is quadrature phase shift keying (QPSK). It is used extensively in applications including CDMA cellular service, Iridium (a voice/data satellite system) and digital video broadcasting -satellite (DVB-S). Quadrature means that the signal shifts between phase states which are separated by 90 degrees. The signal shifts in increments of 90 degrees from 45 to 135, –45, or –135 degrees. These points are chosen as they can be easily implemented using an I/Q modulator. Only two I values and two Q values are needed and this gives two bits per symbol. There are four states therefore it is a more bandwidth-efficient type of modulation than BPSK.

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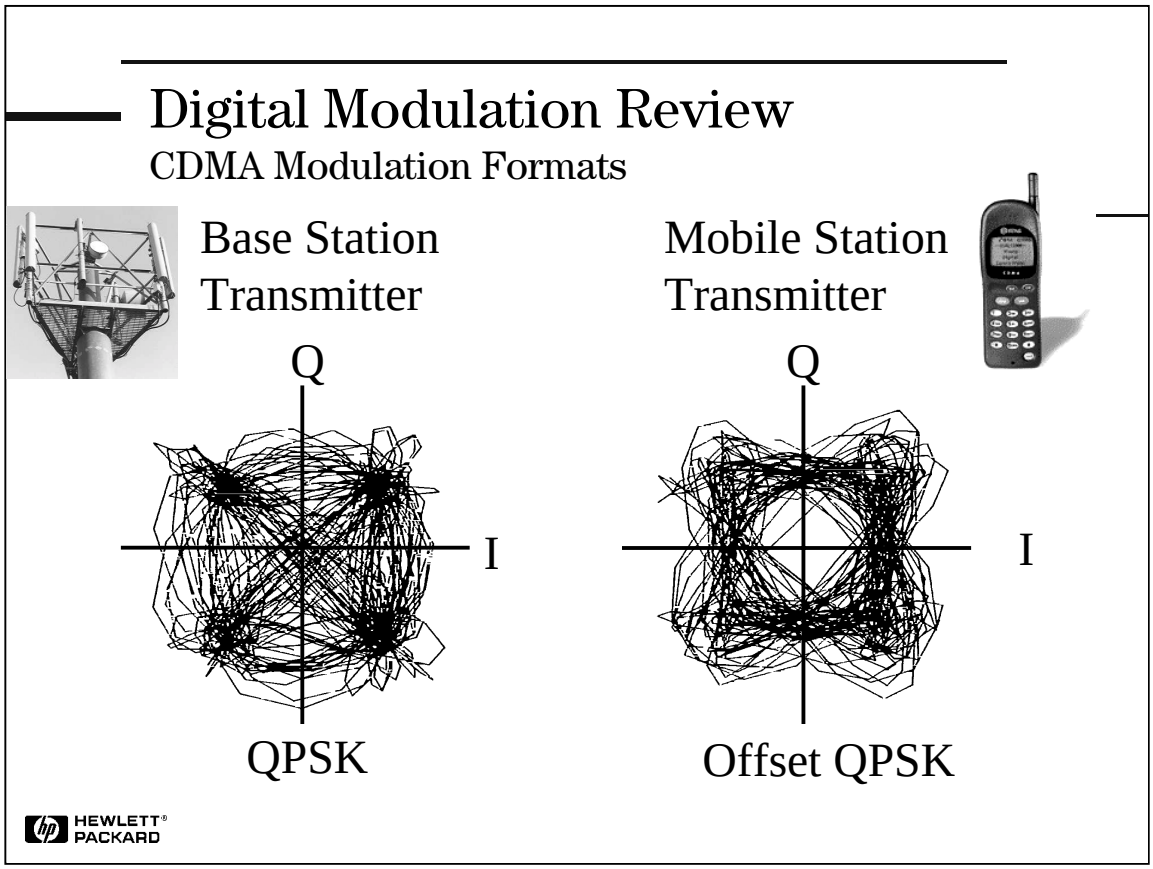
Slide #105



CDMA uses quadrature phase shift keying (QPSK) modulation during the forward link (base station to mobile) and offset QPSK during the reverse link. In a QPSK signal, the phase of the carrier is varied between one of four different phase states. Recall that the origin of the I/Q diagram means no RF is present. If a phase transition were to go through the origin, the RF would be pulsed on and off briefly. This would produce spectral splatter and require more expensive power amplifiers to handle the wide dynamic range.

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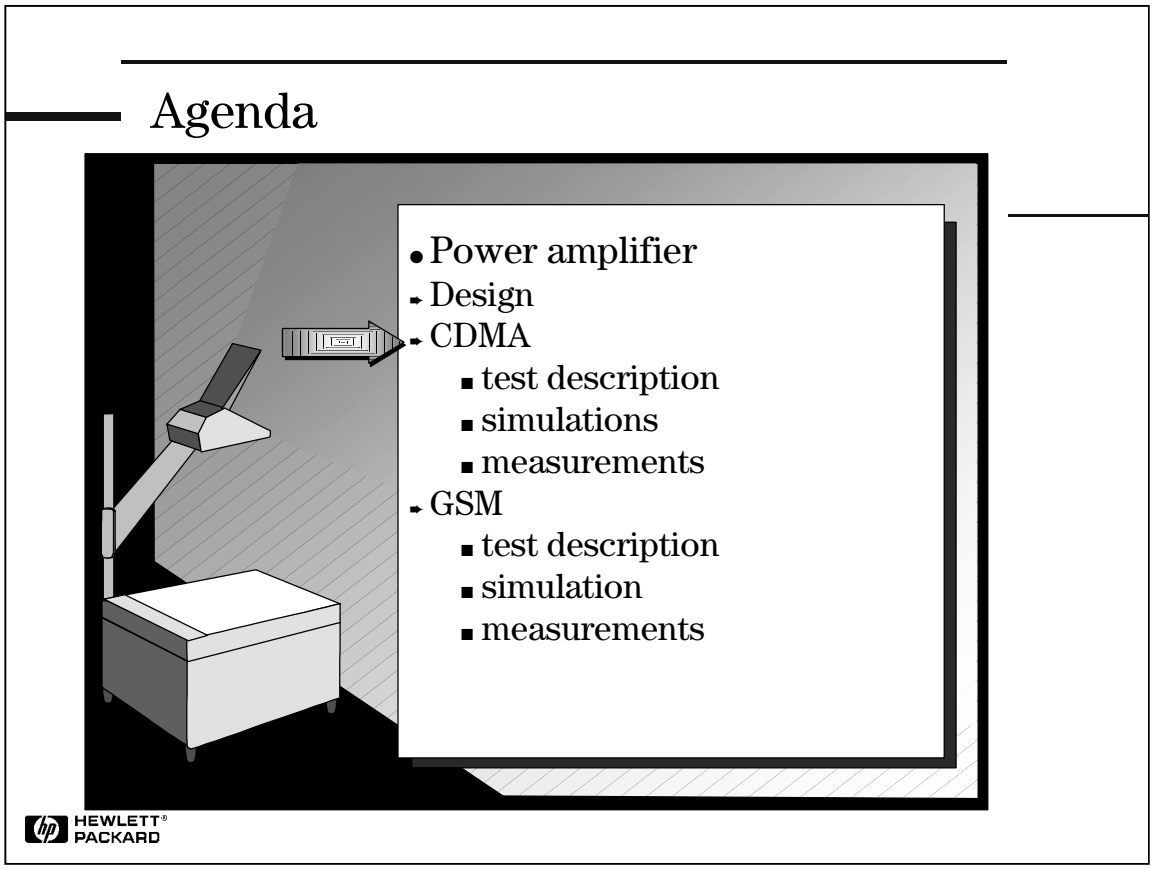
Slide #106



In the remainder of the Power Amplifier section, we will simulate and measure our amplifier using digital modulation. We will start with CDMA, and then cover GSM.

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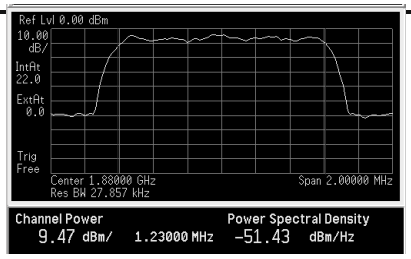
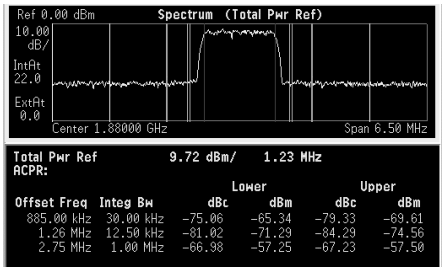
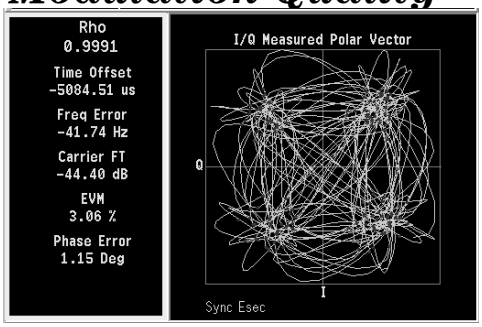
Slide #107

CDMA Tests



- ***Channel Power***
- ***Adjacent Channel Power Ratio (ACPR)***
- ***Modulation Quality***





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As we saw in the previous specification sheet, the important amplifier specifications are channel power and adjacent channel power ratio (ACPR). We will introduce Modulation Quality to get a better system understanding and examine some modulation impairments. Let's look at each specification in more detail.

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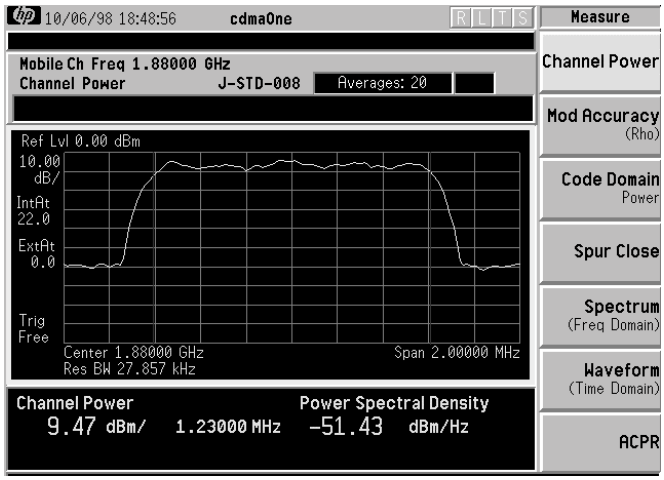
Slide #108

CDMA Tests

Channel Power is band limited to 1.23 MHz



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Power amplifiers used in digital communication systems must be characterized under their operating conditions. This means that we must simulate and measure the output of our amplifier using the 1.23 MHz wide, spread spectrum CDMA signal. Measuring this channel power is not as straightforward as it may seem. CDMA signals are very noise-like and therefore require averaging to improve accuracy and repeatability. The output power cannot be measured using a power meter without a filter because it will measure additional power outside the channel bandwidth. We will first simulate output power and then measure the amplifier using the HP VSA series transmitter tester. The VSA automatically uses digital filtering techniques to band-limit the power to 1.23 MHz.

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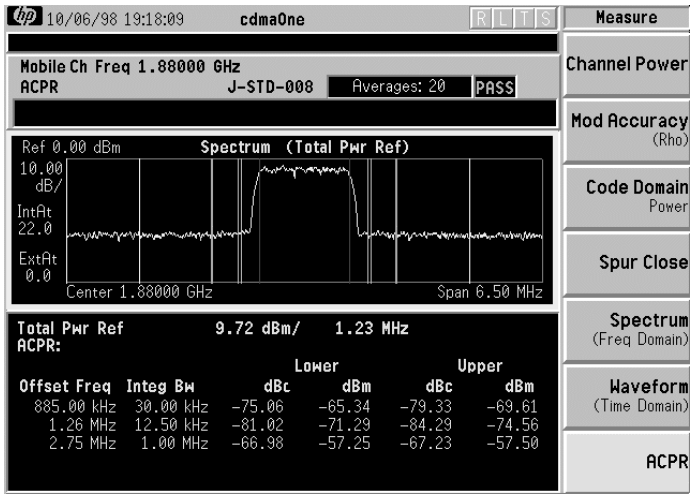
Slide #109

CDMA Tests

ACPR compares in-channel power to out-of-channel power



HEWLETT PACKARD ***Base Station Spec <-45 dBc @ 885 KHz***

Adjacent channel power ratio (ACPR) has become one of the most important tests of a CDMA amplifier. ACPR tests the out-of-channel performance of the amplifier and is closely linked to the amplifier's linearity. Amplifier linearity is critical to the performance of CDMA systems. In these systems, the transmitted power experiences high peak to average variations which can drive amplifiers into saturation. Traditionally, characterizing the linearity performance of a high-power amplifier required a two-tone intermodulation distortion (IMD) measurement, and was sufficient for analog FM systems such as AMPS cellular. While this test is well understood and uses more common test equipment, adjacent-channel power has become the accepted measurement for measuring linearity of power amplifiers used in digital modulation systems.

The IS-95 (cellular) and ANSI J-STD-008 (PCS) specifications for ACPR are below:

IS-95	Base Station	IS-95	Mobile
<-45 dBc	> 750 KHz	<-42 dBc	> 900 KHz
<-60 dBc	> 1.98 MHz	<-54 dBc	> 1.98 MHz

ANSI J-STD-008 Base Station		ANSI J-STD-008 Mobile	
<-45 dBc	> 885 KHz	<-42 dBc	> 1.26 MHz

RF Design and Measurement Seminar

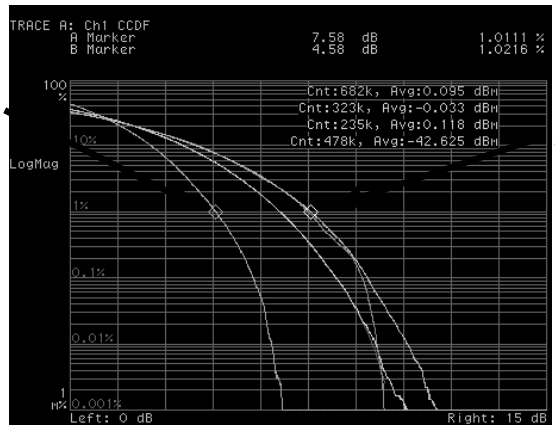
Slide #110

CDMA Tests

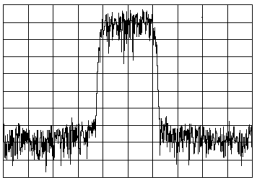
HP E4433B ESG Generator

What's CCDF?

Less stressful



More stressful



Assures adequate test signal for ACPR

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It is important to test ACPR using realistic CDMA signals. It is possible to produce a CDMA like signal by filtering additive white gaussian noise (AWGN) to a 1.23 MHz bandwidth. This is the simplest way of simulating CDMA since it only requires a noise diode and a filter. The IS-95 specification states that an appropriate signal for emulating real-world CDMA includes one pilot, sync, and paging channel and six traffic channels. It is possible, in fact, for an amplifier pass the ACPR test with one source, and fail with another. Using a complementary cumulative distribution function (CCDF) a designer can gauge the peak-to-average variations of the test signals. The CCDF plot the percentage of time the signal reaches a given peak. The figure above compares signals that have a 4.6 dB peak (lightly-loaded cell) and 7.6 dB peak (heavily loaded cell) 1% of the time. Depending upon the data and specific traffic channels selected, CDMA signals can have crest factors of up to 14 -15 dB.

We used the HP ESG series digital signal generator with options UN5 and UND as our CDMA source. The source provides preloaded waveforms which simplify CDMA signal generation. For example, the specified 9-channel waveform with pilot, paging, sync and 6 traffic channels is already preloaded into the generator.

The HP 89400 series measurement system allows complete characterization of the CDMA signal, including time domain statistics of the signal using the CCDF measurement. The CCDF measurement will characterize the peak-to-average statistics of the signals, aiding your CDMA transmitter designs.

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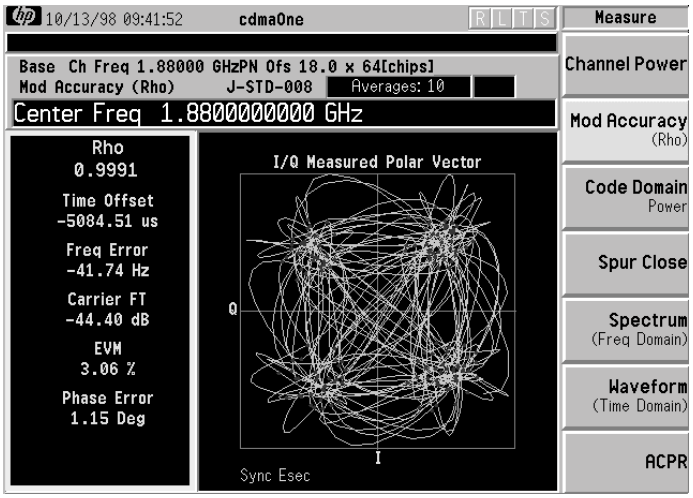
Slide #111

CDMA Tests

Modulation Quality (EVM & Rho)



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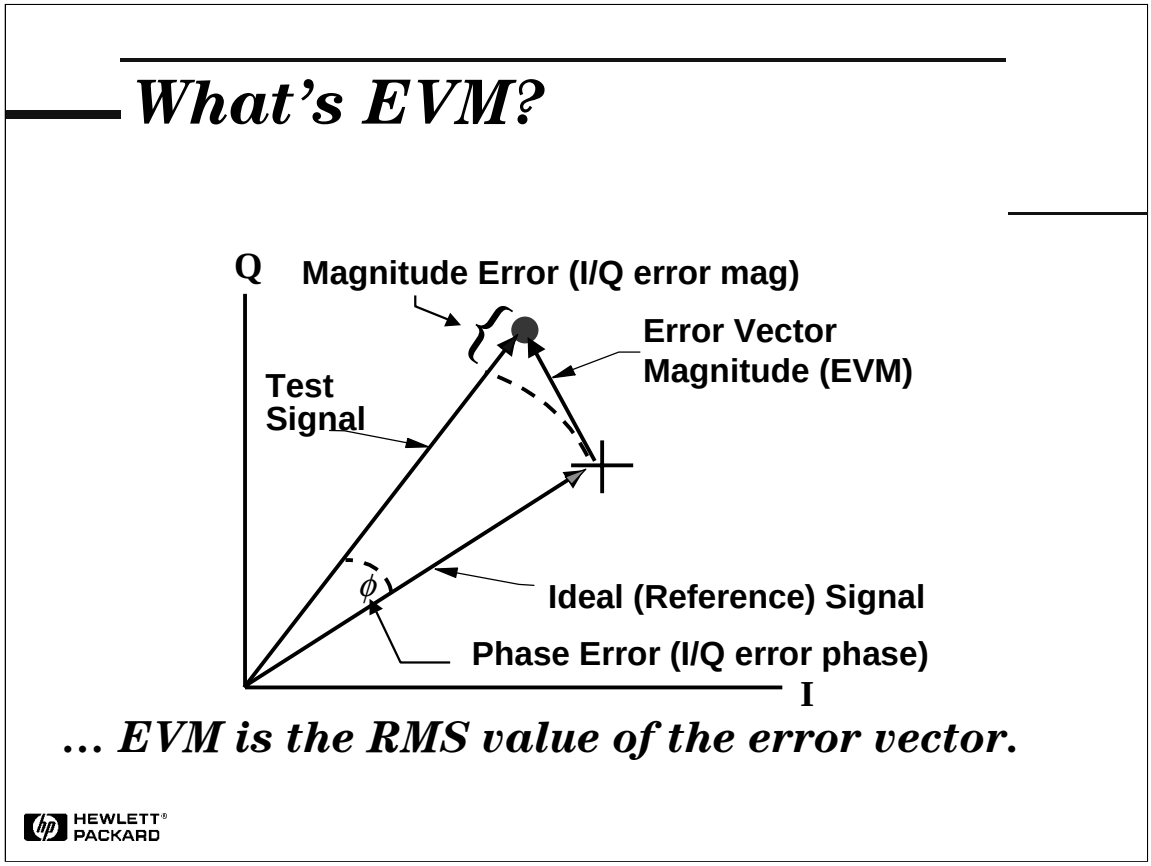
All communications systems specify modulation quality or accuracy. FM systems specify peak deviation and distortion. North American digital cellular (NADC) TDMA systems specify error-vector magnitude or EVM. GSM specifies the phase error or global phase trajectory. CDMA systems specify modulation quality in terms of a correlation coefficient, rho.

RF Design and Measurement Seminar

Slide #112



The I/Q constellation of our digitally modulated signal provides a wealth of information. First recall the basics of digital modulation: Digital bits modulate an RF carrier by varying the carrier's magnitude and phase such that, at each data clock transition, the carrier occupies any one of several unique phase and amplitude locations on the I/Q plane. Each location encodes a specific data symbol, which consists of one or more data bits. A constellation diagram shows the valid locations at the decision time (i.e., the magnitude and phase relative to the carrier) for all permitted symbols, of which there must be 2^n, given n bits transmitted per symbol. Thus, to demodulate the incoming data, one must accurately determine the exact magnitude and phase of the received signal for each clock transition.

At any moment, the signal's magnitude and phase can be measured. These values define the actual or "measured" phasor. At the same time, a corresponding ideal or "reference" phasor can be calculated, given knowledge of the transmitted data stream, the symbol clock timing, baseband filtering parameters, etc. The difference between these two phasors provides both the signal error vector magnitude (EVM) and the phase error. By convention, EVM is reported as a percentage of the ideal peak signal level, usually defined by the constellation's corner states. EVM and phase error are two principal parameters for evaluating the quality of a digitally modulated signal.

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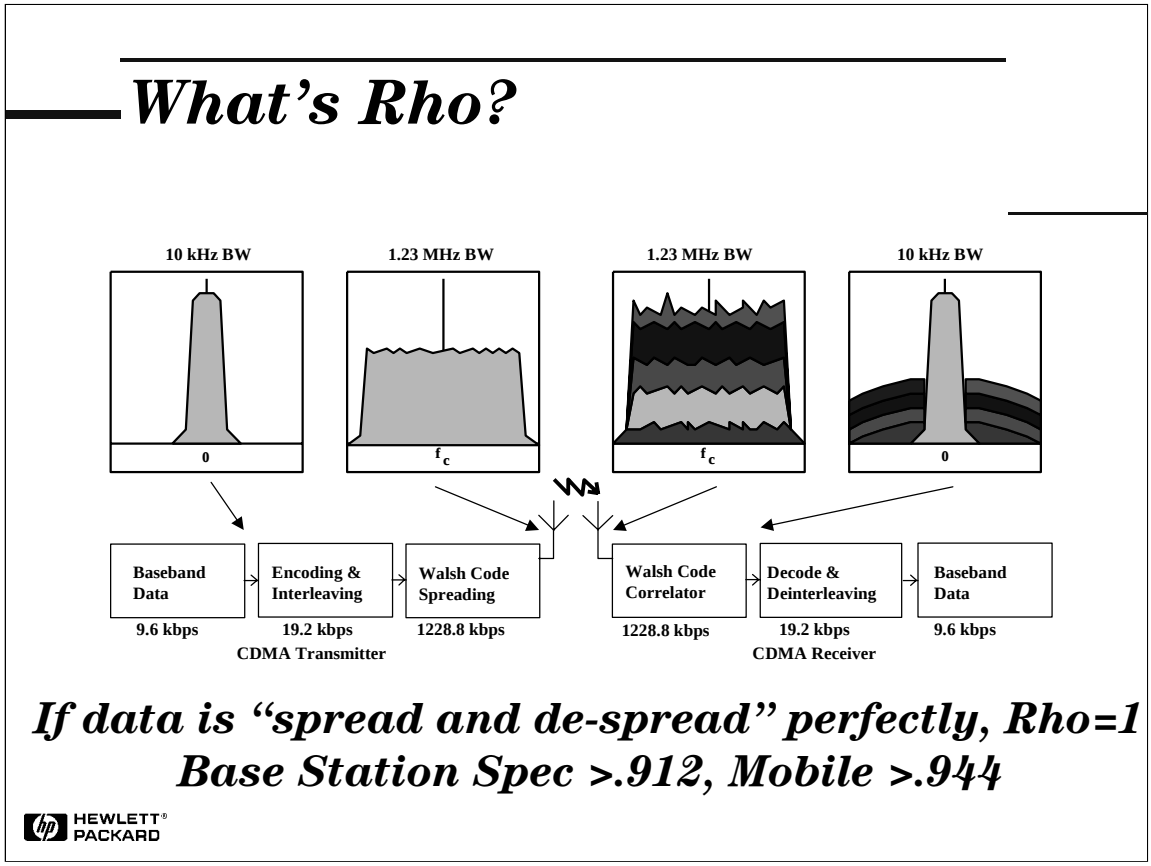
Slide #113



CDMA specifies its modulation quality in terms of a correlation coefficient, rho. Rho can be thought of as the fraction of power that contains useful information. Since CDMA uses correlative receivers, the waveform quality is based on splitting the transmit power into correlated and uncorrelated components. Rho is defined as the ratio of correlated power versus total power. If some of the transmitted energy does not correlate, this excess power will appear as added noise that may interfere with other users on the system. Poor rho will affect each cell's capacity. Because the uncorrelated power appears as interference to the mobiles, causing the signal on the traffic channels to be raised to overcome the interference. At some point, the site will have to shed calls in order to supply the remaining calls with an adequate signal-to-interference ratio. The waveform quality measurement is made on only one code channel. The IS-95 and ANSI J-STD-008 forward link (base station to mobile) specifications is >.912, and the reverse link (mobile to base station) specification is >.944.

Now that we have introduced channel power, ACPR, CCDF, EVM, and rho, let's set up the CDMA simulation in the Advanced Design System.

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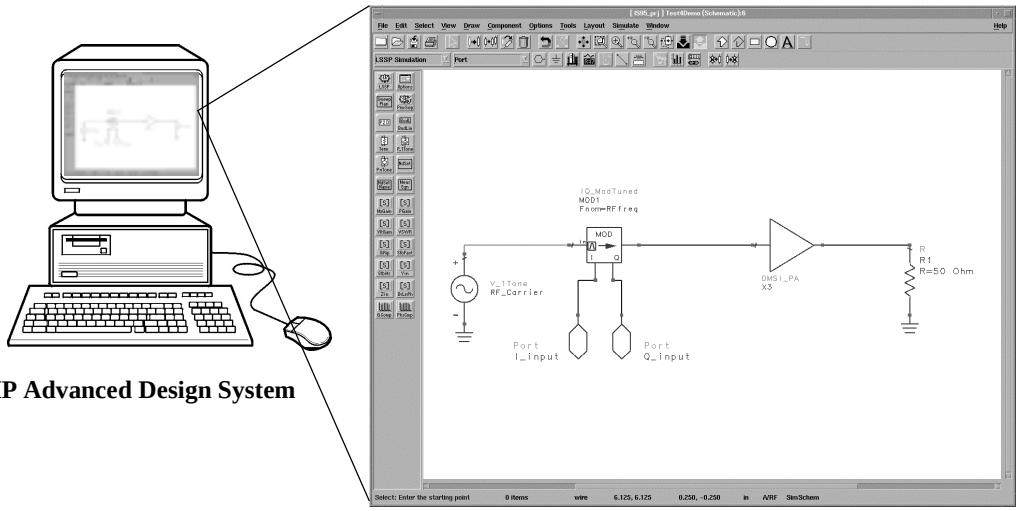
Slide #114

CDMA Tests

Simulation Setup



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The CDMA simulation setup uses an RF source for the carrier, I/Q bit streams to represent the data being modulated onto the carrier, the device under test (DUT) and an output termination. The characteristics of the I and Q modulating signals are what determine the quality of the CDMA test signal. There are several projects in HP's Advanced Design System example directories that demonstrate ways of creating test signals for both forward and reverse links to help you get started.

We used a CDMA test signal with extremely low residual ACPR (on the order of -100dBc) and built-in measurement equations to calculate ACPR, EVM and channel power. Rho was calculated from EVM.

RF Design and Measurement Seminar

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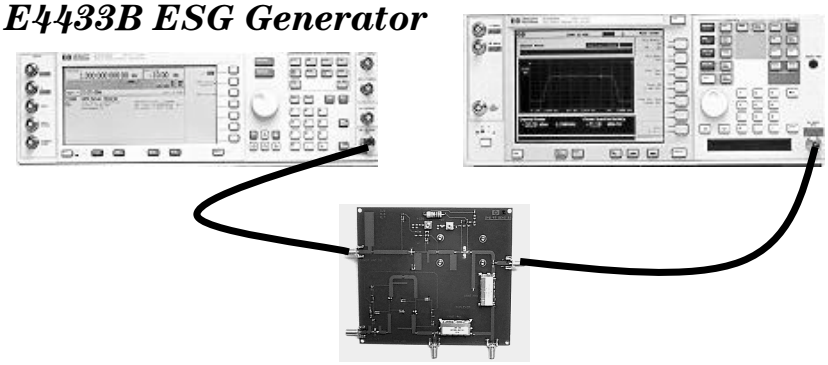
CDMA Tests

Measurement set-up

HP E4433B ESG Generator

HP E4406A VSA Analyzer



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We used the HP ESG series digital signal generator with Options UN5 and UND as our CDMA source, and the VSA series transmitter tester with Option BAC as our CDMA analyzer.

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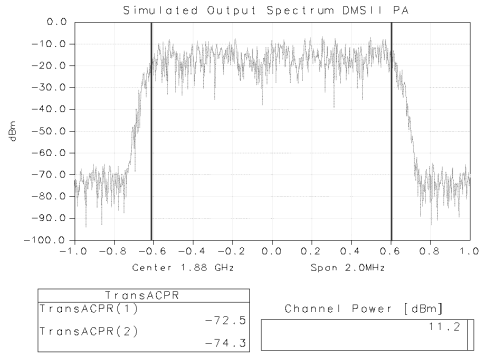
Slide #116

CDMA Tests

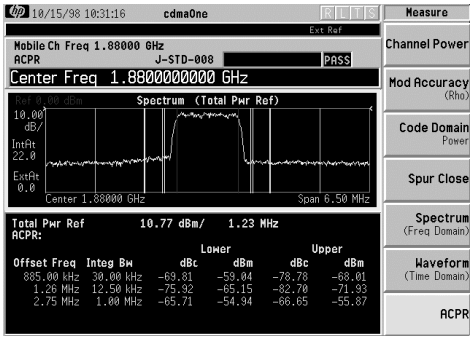
Channel Power and ACPR

Simulation



Pwr = 11.2 dBm
ACPR < -70 dBc

Measured



Pwr = 10.8 dBm
ACPR < -70 dBc

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Using our amplifier, we simulated channel power of 11.2 dBm with a –13 dBm CDMA reverse modulated signal input. The measured channel power (accounting for cable losses) was 10.8 dBm which agreed with the simulation within 1 dB. The ACPR was simulated at ±885 KHz away from the channel, integrated over a 30 KHz bandwidth. The simulation and measured ACPR results agreed within 5 dB.

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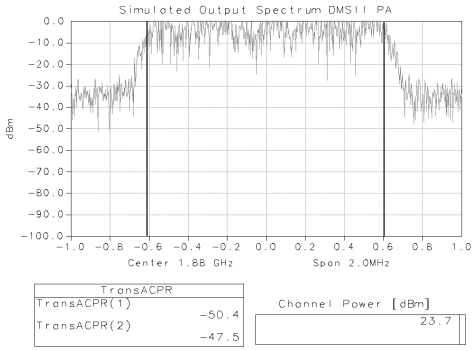
Slide #117

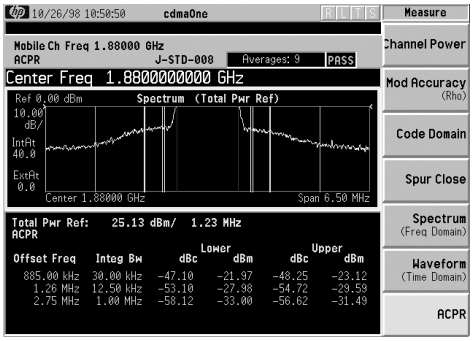
CDMA Tests

Channel Power and ACPR in Saturation

Simulation



Measured



Pwr = 23.7 dBm
ACPR < -47 dBc

Pwr = 23.2 dBm
ACPR < -47 dBc

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To further test the correlation between simulation and measured results, we increased the power input to saturate the amplifier. With 0 dBm input, the ACPR increases but does not fail the J-STD specification. The ACPR measurement will fail if 32 coded channels are used instead of the single pilot channel.

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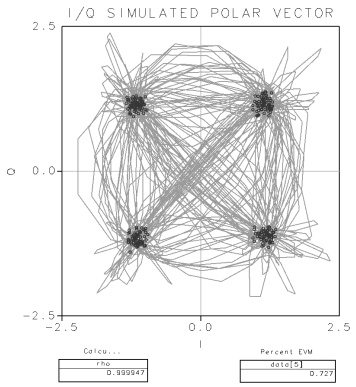
Slide #118

CDMA Tests

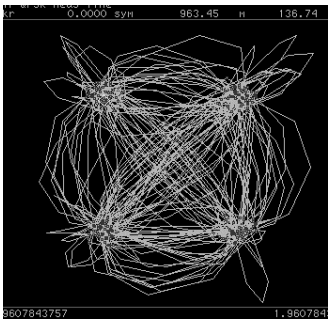
EVM and Rho - No Saturation

Simulation



EVM = .7%
Rho = .999

Measured



EVM = 1.5%
Rho = .999

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Although EVM and Rho are not typically specified for an individual component, we simulated and measured both as a system exercise. In the linear region of the amplifier, we found no degradation of the pilot signal modulation quality. Advanced Design System compares the output of the amplifier to the input and computes the added distortion generated in the amplifier. With a -10 dBm input, the amplifier added less than 1% EVM. We then calculated rho using the following approximation:

$$\rho \cong \frac{1}{1+\left(EVM\right)^2}$$

This approximation is only valid when the error signal does not correlate to the ideal signal. It will overestimate Rho for error signals caused by delayed multipath or intermodulation distortion.

The VSA series transmitter tester makes a direct measurement of rho and EVM. With a -10 dBm input, we measured the EVM of our source which has a typical EVM of 1.5% and a Rho greater than .9996.

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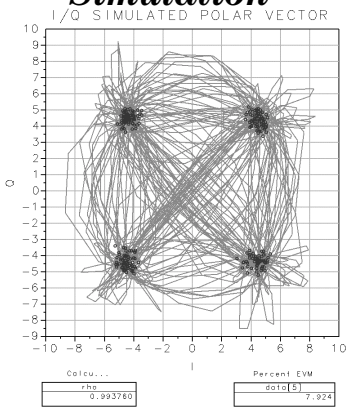
Slide #119

CDMA Tests

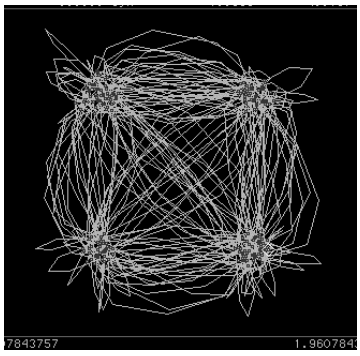
EVM and Rho In Saturation

Simulation



EVM = 8%
Rho = .994

Measured



EVM = 5%
Rho = .997

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To verify that our simulation would hold, we drove the amplifier into saturation, which degraded the modulation quality. With an input power of 3 dBm, the EVM simulation still correlated to the measured result.

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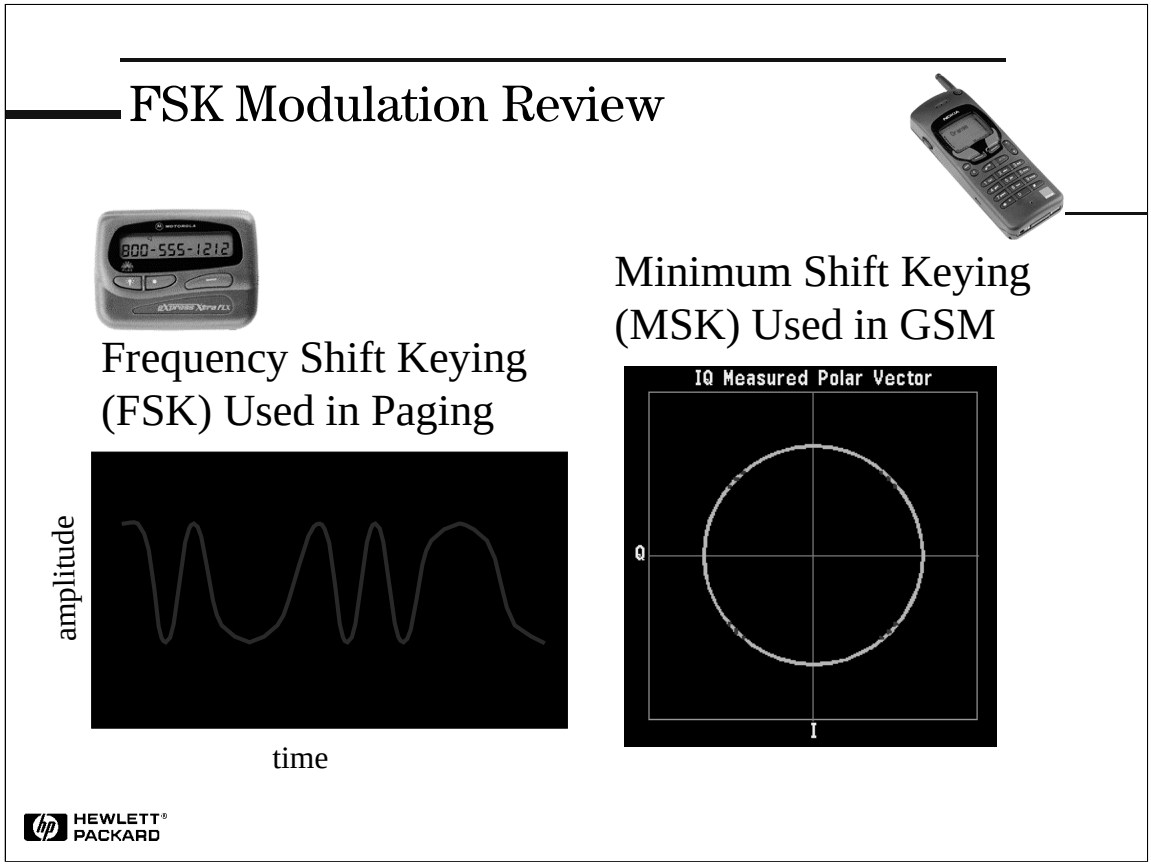
Slide #120



Now that we have simulated and measured our amplifier using phase modulation, lets now examine frequency modulation. Frequency modulation and phase modulation are closely related. A static frequency shift of +1 Hz means that the phase is constantly advancing at the rate of 360 degrees per second, relative to the phase of the unshifted signal. Frequency shift keying (FSK) is used in many applications including cordless and paging systems. Some of the cordless systems include digital enhanced cordless telephone (DECT) and cordless telephone 2 (CT2). In FSK, the frequency of the carrier is changed as a function of the modulating signal (data) being transmitted. Amplitude remains unchanged. In FSK a "1" is represented by one frequency and a "0" is represented by another frequency.

Since a frequency shift produces an advancing or retarding phase, frequency shifts can be detected by sampling phase at each symbol period. Phase shifts are easily detected with an I/Q demodulator. At even numbered symbols, the polarity of the I channel conveys the transmitted data, while at odd numbered symbols the polarity of the Q channel conveys the data. This orthogonality between I and Q simplifies detection algorithms and hence reduces power consumption in a mobile receiver. The minimum frequency shift which yields orthogonality of I and Q is that which results in a phase shift of ± 90 degrees per symbol. FSK with this deviation is called minimum shift keying (MSK). The deviation must be accurate in order to generate repeatable 90 degree phase shifts. MSK is used in the GSM cellular standard. A phase shift of +90 degrees represents a data bit equal to "1", while –90 degrees represents a "0".

FSK and MSK produce constant envelope carrier signals, which have no amplitude variations. This is a desirable characteristic for improving the power efficiency of transmitters. Amplitude variations can exercise nonlinearities in an amplifier's amplitude-transfer function, generating spectral regrowth, a component of adjacent channel power. Therefore, more efficient amplifiers (which tend to be less linear) can be used with constant-envelope signals, reducing power consumption.

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Slide #121

GSM Amplifier Specification Sheet

CELERITEK

CMM0335

Advanced Product Information
September 1996 *(1 of 2)*

890 to 915 MHz
6V, 35 dBm, GSM
Power Amplifier

Electrical Characteristics

Unless otherwise specified the following specifications are guaranteed at room temperature with drain voltage ($+V_d$) = 5.8 V and P_{IN} = +8 dBm, in Celeritek test fixture.

Parameter	Condition	Min	Typ	Max	Units
Frequency Range		890		915	MHz
Pout	PIN = +8 dBm	34.5	35.5		dBm
Efficiency	35 dBm output meeting GSM template	50	55		%
Gain		30	34		dB
Harmonics	2nd @ Pout = +34.5 dBm 3rd @ Pout = +34.5 dBm			-30 -30	dBc dBc
Return Loss	In Celeritek test fixture		10		dB
Negative Supply Current				3	mA
Supply Current			950		mA
Quiescent Current	No RF		250		mA

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Here is an example of an amplifier used in a GSM application. Note the amplifier is specified to meet the GSM template or mask. Let's now look at the in-channel and out-of-channel simulations and measurements that constitute meeting this specification.

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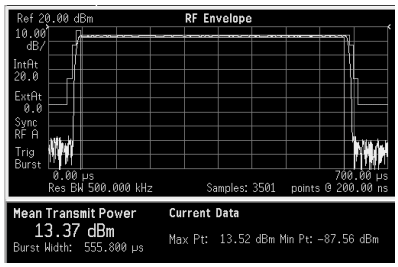
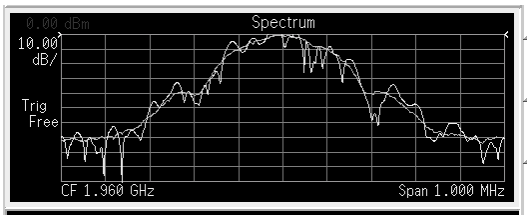
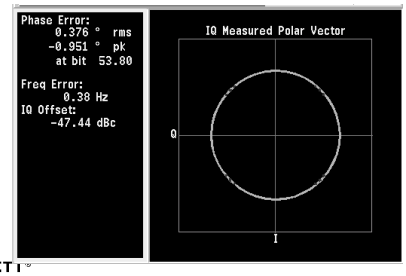
Slide #122

GSM Tests

- ***Power Vs. Time***
- ***Output RF Spectrum***
- ***Phase and Freq. Error***







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GSM is the global system for mobile communications. It was originally designed to standardize and add digital capability to the cellular market in Europe. Since then it has expanded to become one of the primary digital cellular formats in the world. Currently, there are three major GSM systems, GSM900, DCS1800 and PCS1900. They are essentially the same system, differing only by the frequency bands in which they operate. GSM900 works around the 900 MHz band , DCS1800 the 1800 MHz band, and in North America, due to available spectrum restrictions, PCS1900 in the 1900 MHz band. The GSM system uses time division multiple access (TDMA) and frequency division multiple access (FDMA) to provide additional capacity.

As with CDMA, to qualify our amplifier for a GSM application, we are concerned with in-channel, out-of-channel, and modulation quality specifications. The in-channel measurement for GSM is carrier power and power versus time. The out-of-channel measurement is output RF spectrum, and the modulation quality specification provides limits for phase and frequency error. Let's look at each simulation and measurement in detail.

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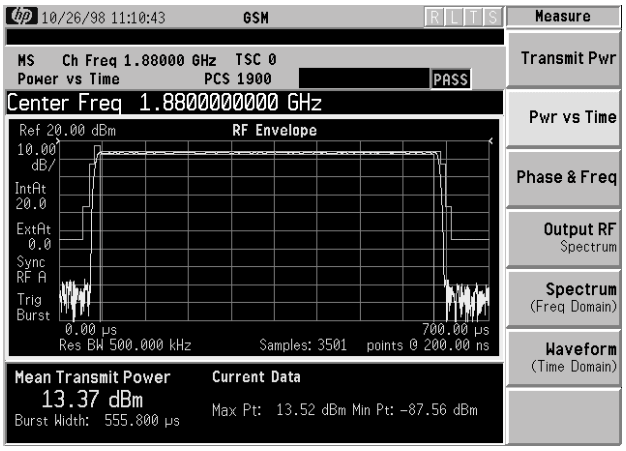
Slide #123

GSM Tests

Power vs. Time Measurements Verify Flatness and Timing of the RF Burst.



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Carrier power is the measure of in-channel power for GSM systems. Mobiles and base stations must transmit enough power, with sufficient modulation accuracy, to maintain a call of acceptable quality without leaking into frequency channels or timeslots allocated for others. GSM systems use dynamic power control to ensure that each link is maintained with minimum power. This power control gives two fundamental benefits: overall system interference is kept to a minimum and, in the case of mobile stations, battery life is maximized.

GSM is a time division multiple access (TDMA) multiplexing scheme with eight time slots, or bursts, per frequency channel. If the burst of information does not occur at exactly the right time, or if the burst is irregular, then other adjacent channels can experience interference. As a result, industry standards specify a tight mask for the fit of the TDMA burst.

Measuring the output power from a GSM transmitter is complicated by the TDMA multiplexing scheme. Each frequency channel is shared among eight users by TDMA. The mobile transmitter turns on only during its active timeslot. During the central part of the TDMA burst when data is being transmitted, the mobile has to control its transmitter output to within ±1 dB relative to the mean value.

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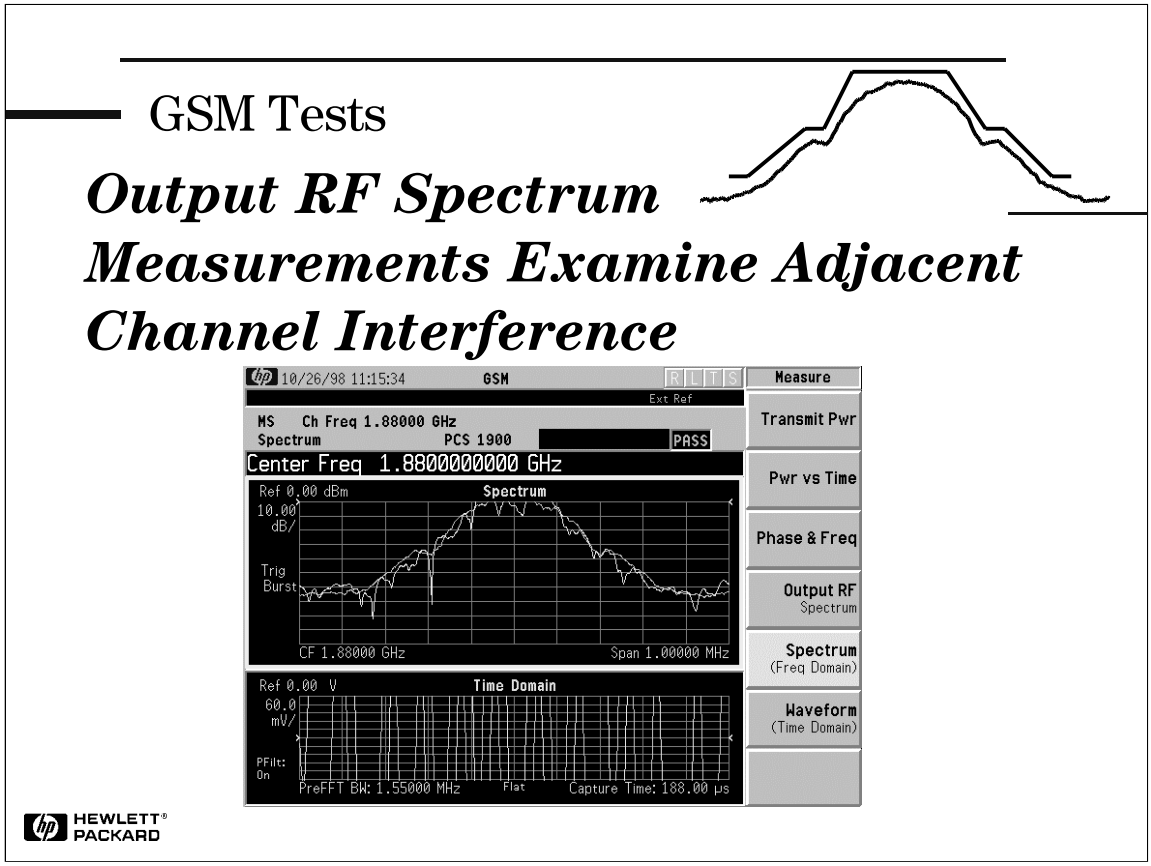
Slide #124



GSM mobiles need to be able to operate in the presence of interference from other GSM channels and other non-GSM users of the radio spectrum. Strong signals in adjacent bands often cause intermodulation products in the receive section of a mobile unit causing a dropped call. There are three GSM specifications that cover interference: output RF spectrum, spurious emissions, and intermodulation attenuation. We will simulate and measure Output RF spectrum, which is essentially an adjacent channel power measurement. GSM frequency channels are 200 KHz wide, so the GSM specification regulates the amount of power in 200 KHz channel increments. The GSM base station (11.21 version 4.6.0) specification for < 33 dBm output power is listed below:

Offset	Specification	Condition
200 KHz	<-30 dBc	30 KHz BW
250 KHz	<-33 dBc	30 KHz BW
400 KHz	<-60 dBc	30 KHz BW
600 KHz	<-60 dBc	30 KHz BW
1200 KHz	<-63 dBc	30 KHz BW
1800 KHz	<-65 dBc	100 KHz BW
>6000 KHz	<-80 dBc	100 KHz BW

This -80 dBc specification challenges the dynamic range of most test equipment presently available.

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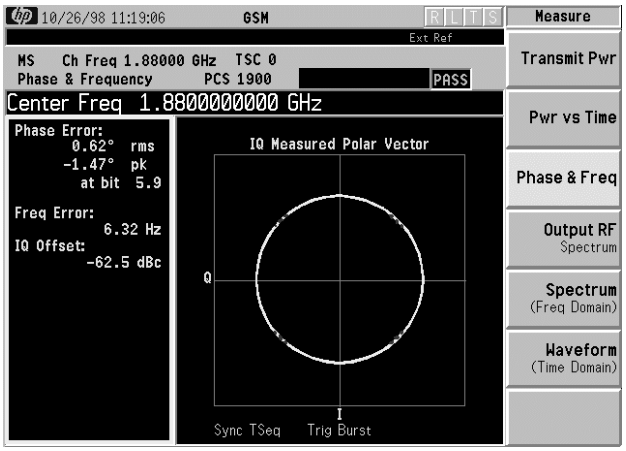
Slide #125

GSM Tests

Phase and Frequency Error Determine the Quality of Modulation



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Phase and frequency error determine the quality of GSM modulation. GSM uses 0.3GMSK (Gaussian Minimum Shift Keying) as its modulation format . The 0.3 describes the bandwidth of the Gaussian filter with relation to the bit rate.

GMSK is a special type of digital FM. Ones and zeros are represented by shifting the RF carrier by ± 67.708 KHz. Modulation techniques which use two frequencies to represent one and zero are denoted frequency shift keying (FSK). In the case of GSM, the data rate of 270.833 Kbit/sec is chosen to be exactly four times the RF frequency shift. This ratio has the effect of minimizing the modulation spectrum and improving channel efficiency. FSK modulation, where the bit rate is exactly four times the frequency shift is Minimum Shift Keying (MSK). The modulation spectrum is further reduced by applying a Gaussian pre-modulation filter. This slows down the rapid frequency transitions which would otherwise spread energy into adjacent channels.

While 0.3GMSK is not phase modulation, the receiver measures phase to extract the data. It is useful to try to visualize GMSK on an I/Q diagram. Ones are seen as a phase increase of 90 degrees. Zero's cause the same phase change in the opposite direction. When Gaussian filtering is applied, the phase makes slower direction changes, but may reach higher peak velocities to catch up again.

The exact phase trajectory is very tightly controlled. GSM specifies that the phase error shall be no more than 5 degrees rms or 20 degrees peak and that the mean frequency error across the burst shall not exceed 0.05 PPM (approximately 100 Hz at PCS frequencies).

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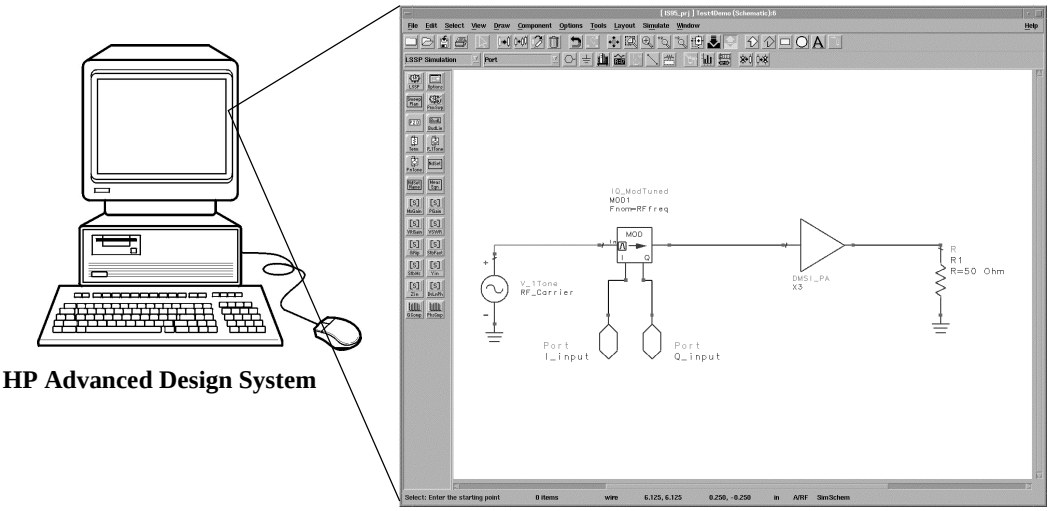
GSM Tests

Simulation Setup



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The GSM simulation setup uses a standard GSM source from the component library. The source was pulsed to simulate TDMA, and measurement equations were used to calculate Power versus Time, Output RF spectrum, and Modulation quality.

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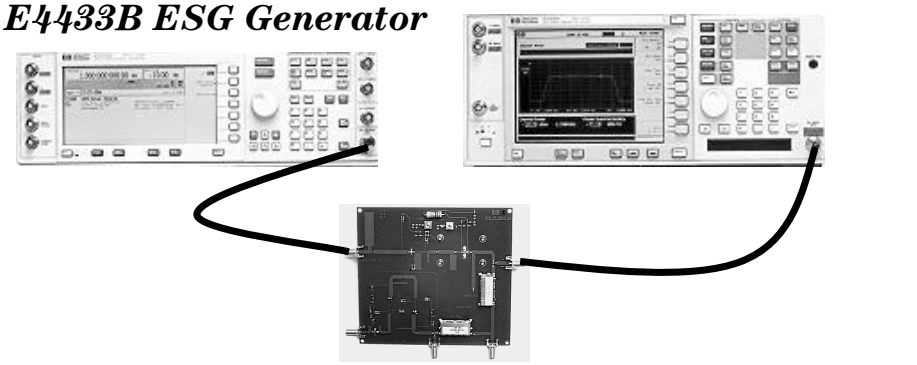
Slide #127

GSM Tests

Measurement Setup

HP E4433B ESG Generator

HP E4406A VSA Analyzer



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The GSM simulation can be verified using a GSM source and analyzer. We used the HP ESG-D series signal generator with Option UN8 and the HP VSA series transmitter tester with Option BAH.

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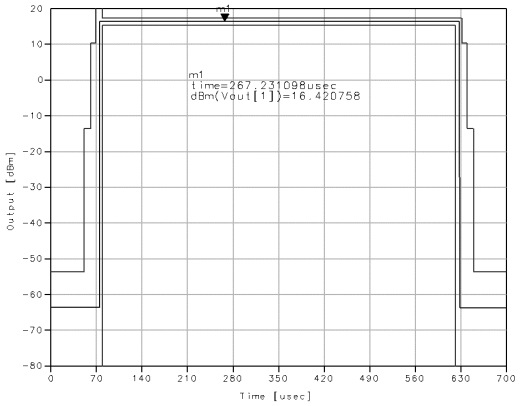
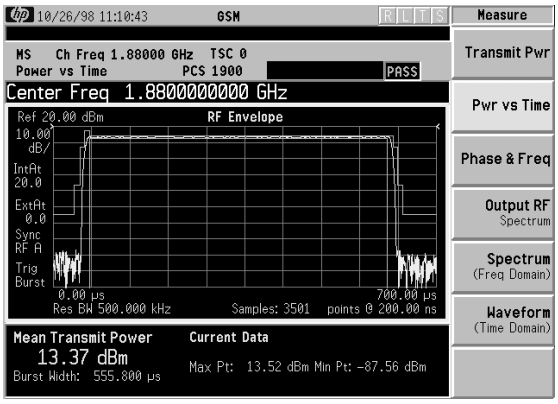
GSM Tests

Power versus Time

Simulation



Measured



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In the Advanced Design System we set up the simulation using a pulsed RF signal. We set the Pulse width = 577 µsec, period = 4.615 msec, and on/off ratio of 80 dB. With the amplifier operating in the linear range, the output pulse is a perfectly scaled version of the input. Notice the power versus time mask in both the simulation and measured results. Typically amplifier manufacturers do not list the rejection at each time offset: they only report that the output power meets the GSM mask. In our simulation we did not filter the pulse using the .3 Gaussian filter, which resulted in higher power for the simulation.

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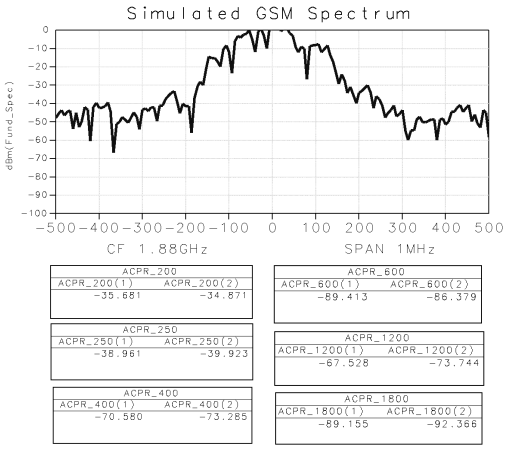
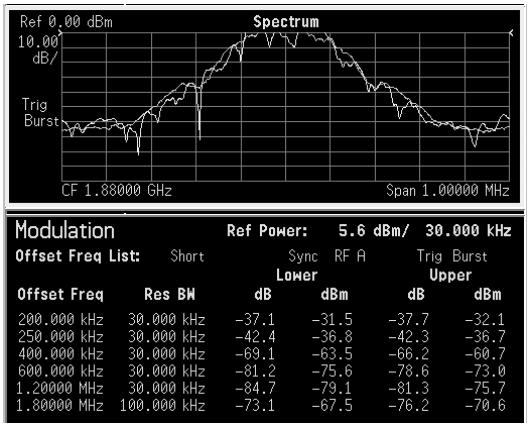
GSM Tests

Output RF Spectrum

Simulation ***Measured***





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In the Advanced Design System we calculated the RF spectrum performance at the required GSM offsets. The simulation predicted that the amplifier would meet the GSM specification, and our measurement confirmed this. As with the Power vs. Time measurement, amplifier manufacturers do not list the rejection at each offset, they only report that the output power meets the GSM mask.

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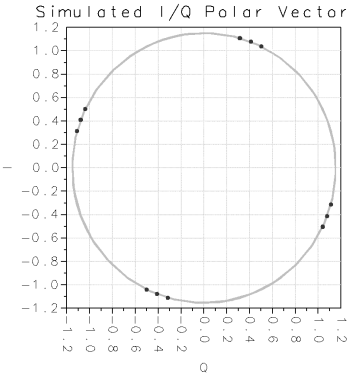
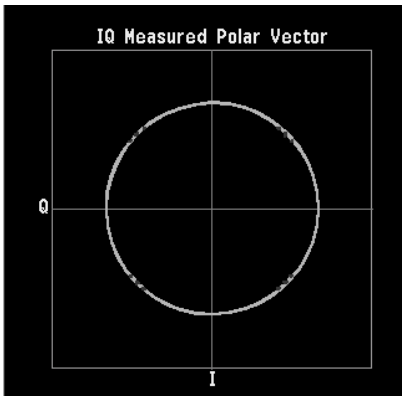
GSM Tests

Phase and Frequency Error

Simulation



Measured



Phase Error < 1deg
Freq. Error < 5 Hz

Phase Error < 1deg
Freq. Error < 5 Hz

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Although Phase and frequency error are not typically specified for an amplifier, we simulated and measured both to demonstrate system level specifications. In the linear region of the amplifier, we found no degradation of the modulation quality. The Advanced Design System simulated a phase error less than 1 degree, and a frequency error less than 5 Hz. GSM specifies that the phase error shall be no more than 5 degrees rms or 20 degrees peak and that the mean frequency error across the burst shall not exceed 0.05 PPM (approximately 100 Hz at PCS frequencies).

Our measurements met the GSM specification and agreed with simulated results.

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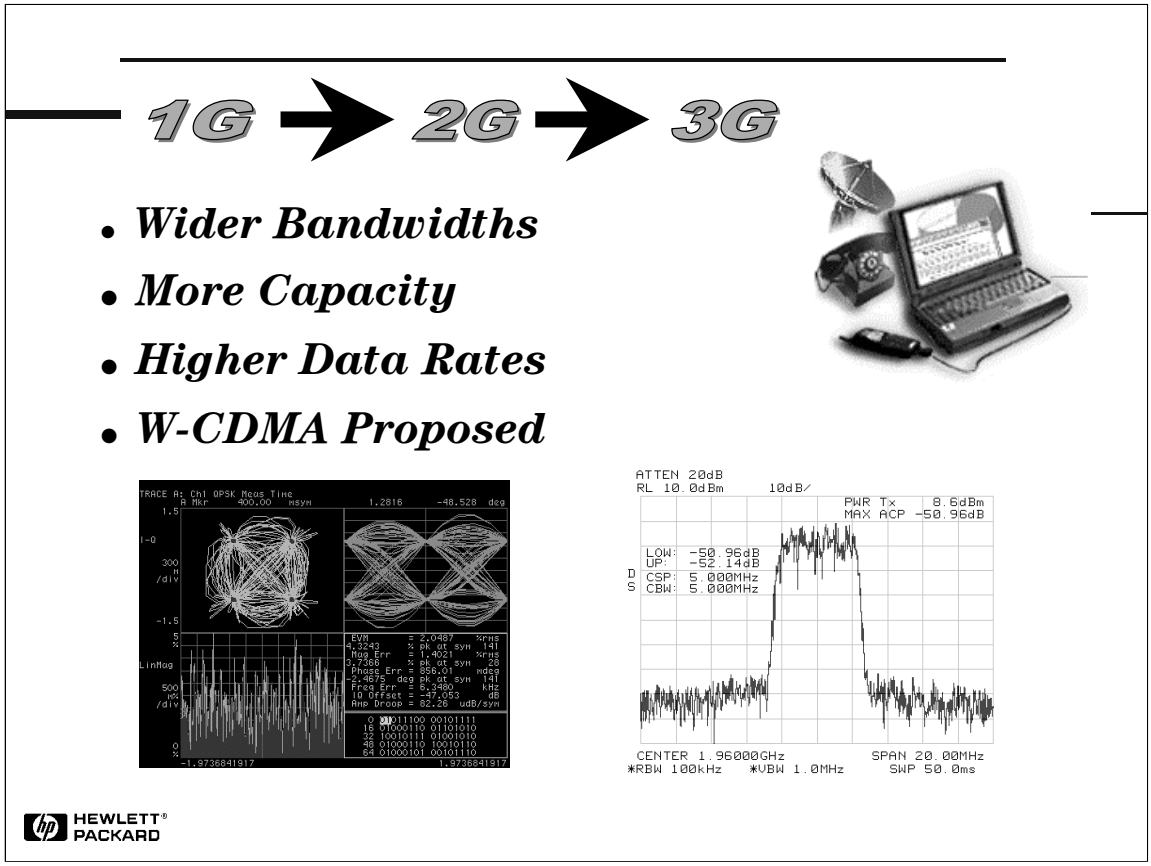

The desire for added capacity and higher bit rate services has fueled the development of third generation cellular systems (3G). One of the more popular technologies being proposed for 3G is wideband - CDMA. As the name applies, W-CDMA is a wider bandwidth (4.1 vs. 1.23 MHz) version of CDMA, and although the standards are still developing, HP offers a suite of W-CDMA solutions now. These current solutions, based on the W-CDMA experimental system specification, will evolve as commercial 3G standards are developed.

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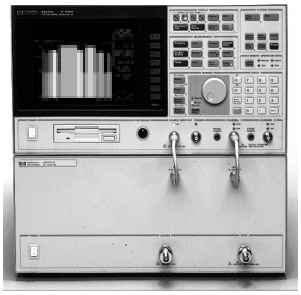
HP W-CDMA Solutions

HP ESG D-series RF Signal Generator with Option H97 Multi-code channel W-CDMA Personality, Option UND Dual Arbitrary Waveform Generator, Option H98 W-CDMA Real-time coding and Option H99 enhanced ACPR.

HP 8563E Option K35 Spectrum Analyzer and W-CDMA ACPR Test Set



HP 89400 Series W-CDMA Measurement System

HP E8851A Communications Systems Designer + W-CDMA Design Library

HP 71910P Wideband Receiver
HP 89410A Vector Signal Analyzer for 20 MHz demodulation bandwidth

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HP offers a comprehensive and connected suite of W-CDMA solutions now. These current solutions, based on the W-CDMA experimental system specification, will evolve as commercial 3G standards are developed.

HP ESG D series signal generators provide accurate and stable broadband signals to test your W-CDMA system designs. The built-in arbitrary waveform system, and other options give you the capability to test your systems with W-CDMA signals up to 10 MHz wide and with the required ACP performance. You can generate signals with multiple code channels and variable symbol rates. In addition, two fully coded channels with real-time random data is provided as a separate option.

HP 8563E Option K35 W-CDMA adjacent channel power ratio (ACPR) test set increases the dynamic range of the HP 8560E series spectrum analyzers to at least 70 dB while testing ACPR. This dynamic range meets the needs of the emerging W-CDMA standards.

HP 89400 series W-CDMA code domain power measurement system for BTS transmitter test automatically determines active channels of any code layer. Use this system to view and measure code domain power for all codes and symbol rates in each of the 16 timeslots. Because it is based on the **vector signal analyzer** you can evaluate and troubleshoot W-CDMA digitally modulated signals with both qualitative displays and quantitative measurements such as error vector magnitude (EVM), rho, and peak-to-average power statistics.

HP communication systems designer (HP E8851A) is a design tool in HP's advanced design system. It links to HP test equipment to tie system simulation together with characterization and troubleshooting of prototype designs. Transfer simulations to HP ESG-D series signal generators with built-in dual arbitrary waveform generators to stimulate your prototype designs with W-CDMA signals. Capture data from your prototypes with the HP 89441A vector signal analyzer. This data can be used to send real measured signals through the rest of your simulation. These "*virtual prototypes*" uncover potential design problems and reduce development bottlenecks.

The **HP 89410A vector signal analyzer** with **Option AY7** and **HP 71910P wideband receiver** combine to make a single wideband measurement system. This system has the capability of analyzing signals with up to a 20 MHz information bandwidth at frequencies up to 26.5 GHz.

RF Design and Measurement Seminar

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References and More Information

- ***CDMA - www.cdg.org***

- ***GSM - www.gsmdata.com***

- ***W-CDMA - www.hp.com***

HEWLETT PACKARD

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