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A 915 MHz CMOS Frequency Synthesizer

A thesis submitted in partial satisfaction of the

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by

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ABSTRACT OF THE THESIS

A 915 MHz CMOS Frequency Synthesizer

by

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A 915 MHz Frequency Synthesizer is designed and tested for use in a low power spread-spectrum communication transceiver. The synthesizer consists of a phase locked loop to control a four stage ring oscillator to output 915 MHz. The four stage ring oscillator naturally provides two sets of quadrature signals for use in a single-sideband modulator (SSB) and requires no external components. The complete Frequency Synthesizer is fabricated in a 1 μm standard CMOS process and at a supply voltage of 4.2 volts, the VCO dissipates 18.8 mW. Finally, the expected noise and speed performance for other technologies is presented.

Chapter 1

System Considerations

1.1 Introduction

The increased use of laptop computers and cellular phones in the last decade demonstrates the growing need for devices that facilitate mobility while allowing constant communication. In the future, analog cellular phones will be replaced with digital modems capable of transmitting and receiving digital modulation formats. This change is motivated by the ability of digital formats to accommodate more users, provide better security, and allow the transmission of digital data. Once this transition is complete, digital formats will allow the laptop computer and cellular phone to merge, making the “mobile office” a reality.

A conventional RF (Radio Frequency) architecture with its discrete external components, expensive SAW filters, and many chips, is not a viable design option

for the wireless market. As an engineer from AMD once said “In the wireless market the four most important things are cost, cost, cost, and power.” (The only reason power ranks fourth was so a cheaper battery can be used.) The difficulty of developing an RF architecture suitable for a standard Digital CMOS process goes beyond achieving high speed circuits with low power supply voltages and low power dissipation. The real challenge exists in providing these elements while still considering what the market demands; low cost.

1.2 UCLA Transceiver Architecture

The aim of the wireless communication design group at UCLA has been to develop an RF architecture that will allow the integration of a complete wireless personal transceiver. The architecture developed at UCLA goes beyond limitations of conventional RF architectures which require external components. Instead, it takes advantage of the properties available to the IC designer to create a transceiver that is void of external componets, easily integrated, and consumes a minimal amount of power.

One technique used to decrease power dissipation and allow full integration is to chose a modulation format with a low power dissipation such as Frequency Hopped Spread Spectrum (FHSS) modulation. Another, is to perform all the complicated processing at baseband and retain only a few circuits that operate at the transmit and receive frequencies. This is accomplished by using a direct conversion

architecture [2].

1.2.1 Spread Spectrum Techniques

Diversity in the frequency domain is used to overcome losses due to multi-path fading in a wireless environment. Presently, there are two spread spectrum formats that are popular. The first is Direct Sequence which is being marketed by Qualcomm Inc., a San Diego based company, and the second is Frequency Hopped Spread Spectrum (FH/SS). The Direct Sequence format spreads the signal in the frequency domain by multiplying the data with a pseudo random string of ones and zeros. The receiver multiplies the modulated signal by the same pseudo random string to recover the original data. To get effective spreading, the pseudo random code must be at least four times faster than the data rate. Unfortunately, requiring circuits in the transceiver to operate four times faster than the data rate will increase power dissipation.

In Frequency Hopped Spread Spectrum, the data is spread in the frequency domain by ‘hopping’ the transmit frequency to different frequency locations. The hopping rate is independent of the data rate. In harsh environments, the hopping rate can be much slower than the data rate so the same data is retransmitted at different frequencies.

1.2.2 Direct Conversion

Both the transmitted and rececived signals are generated using a Direct

Conversion to and from the RF band. The advantages of this type of receiver is that low cost audio circuits can be used instead of high power, high frequency circuits. In addition, the IF (Intermediate Frequency) filter is also reduced to a simple Low Pass Filter (LPF). Best of all, the transceiver can be completely integrated, resulting in lower power dissipation. Some problems encountered with this type of architecture include spurious demodulation due to nonlinearities in the down conversion mixer and baseband spectrum folding. The spurious demodulation is suppressed by using a very linear sub-sampling mixer after the LNA (Low Noise Amplifier) while baseband spectral folding is reduced by using quadrature demodulation to resolve the difference between the upper and the lower sideband of the RF signal.

Quadrature mixing is also utilized to suppress unwanted sidebands. It is expected that the image tone will be rejected by 40 dB using this technique. To achieve this level of attenuation, the similarity of gain between the two channels must match to within 1% [4]. The image attenuation is important because it represents the attenuation of any possible users at the image frequency. Since a log normal distribution of interferers is expected due to the frequency diversity of a FH/SS system, 40 dB attenuation should be adequate. If a log normal distribution could not be assumed, powerful users at the image frequencies would be more of a concern. Finally, a switched capacitor filter will be used to eliminate the SAW filter that is typically used to attenuate unwanted channels after down-conversion.

1.3 Types of Frequency Synthesis

This project seeks to design an integrated Frequency Synthesizer for use in the UCLA wireless architecture. The Frequency Synthesizer (FS) generates a Local Oscillator (LO) signal used in the up-conversion and down-conversion of transmitted and received signals. This signal must meet the frequency stability, precision, and frequency agility required by the architecture. Further, the LO signal must have a spectrum which does not degrade the receiver performance beyond the limits set by the other component of the receiver.

The function of the frequency synthesizer is to translate the performance of a reference oscillator to frequencies that are useful to the user. Various methods are available to generate this carrier frequency. However, many of these are restrictive due to the modulation requirements of the system, the ability of the synthesizer to be integrated, as well as the necessity of limiting power dissipation. Many of these methods are summarized below. Most high performance frequency synthesizers typically combine two or more of the following methods, exploiting the advantages of each.

1.3.1 Direct Analog Synthesis

In direct analog synthesis, the reference frequency is directly translated using analog techniques such as switching, frequency division, multiplication, filtering, and mixing. This form of synthesis offers very high purity at the cost of

very high complexity. What follows is an explanation of each type of synthesis along with advantages and disadvantages in terms of a wireless environment.

1.3.1.1 Frequency Switching

Frequency Switching is the most straight-forward form of frequency synthesis. It consists of a bank of crystals connected through a bank of switches to a crystal-controlled oscillator. While this type of synthesizer has good close-in phase noise purity and the stability of the crystal reference is maintained [4], it also has many disadvantages. These include the high cost of hardware, a limit on output frequency, and the difficulty of integrating such systems. Because a different reference crystal is required for each desired output frequency, the cost is very high. Additionally, the output frequency is limited to the maximum oscillating frequency of a crystal. The maximum output frequency for a crystal oscillator would be about 200 MHz, operating in the 7th mode of oscillation. Finally, with so many external crystals, complete integration becomes impossible.

When designing this type of synthesizer, the switch used to connect the crystals to the oscillating circuit determines the switch settling time and the level of spurious frequencies. Spurious frequencies are generated when non-selected frequency sources leak to the output node and can degrade system performance by limiting the receiver's dynamic range and folding additional noise. These spurious frequencies are attenuated by using a switch that provides greater isolation between the crystal and the oscillating circuit. Typically, there are three basic types of

switches that are used: mechanical, electromechanical, and electronic. Mechanical and electromechanical switches provide the highest level of isolation but tend to be slow, bulky, and expensive. Further, because these switches must be located off-chip, they may lead to higher power dissipation. Alternatively, electronic switches can provide fast settling times, small size, complete integration, and low power dissipation. Electronic switches, however, create a trade-off between size and power consumption versus isolation. Monolithic FET switch arrays are extremely small and have very low power consumption but have relatively low isolation. PIN and conventional diode switches have much higher levels of isolation, but are bulkier and have relatively high power consumption [6].

1.3.1.2 Frequency Division

Another way a generate different output frequencies is by using a frequency divider. In the past, regenerative dividers and injection locked oscillators were a popular choice for this purpose. Now that high speed digital circuits are available, however, most frequency division is accomplished with a digital counter. A digital counter is preferred because, unlike the other methods of dividing, it functions over a wide bandwidth. Unfortunately, a digital counter outputs square waves which have high harmonic content and can once again degrade receiver performance by limiting dynamic range and folding additional noise.

Finally, this type of frequency synthesis can only produce an output frequency less than the input frequency. Since a crystal reference is limited to about

200 MHz, this type of synthesizer is only good for frequencies less than 100 MHz. Further, to produce many frequencies with a fine frequency step size, a large ratio is required by the divider. As a direct result, the output frequency must be even lower in frequency than the output.

1.3.1.3 Harmonic Oscillator or Frequency Multiplication

Frequency multiplication is accomplished by passing an oscillating signal through a highly non-linear element such as a diode, transistor, or a varactor. The nonlinear elements will create tones at the harmonics of the original signal. An impulse oscillator may also be used to generate a short impulse signal that contains both odd and even harmonics. This harmonically rich signal is passed through a very sharp, narrow band filter to attenuate the undesired harmonics. In a well designed synthesizer, up to the 50th harmonic can typically be used. This extends the limited frequency output of the crystal bank synthesizer and many even reduce the number of crystals required [4].

There are many disadvantages to this method. First, the unselected harmonics can be on the order or even greater in magnitude than the desired signal. The undesired harmonics will appear as spurious frequencies and could degrade receiver performance. The only solution to this problem is to use narrow band filters which are expensive and impossible to integrate onto a low cost IC process like CMOS. In addition, the output frequency range is restricted to the passband of the filter, which must be less than the reference frequency. Further, because the settling

time of the frequency synthesizer is inversely proportional to the passband of the filter, slow switching times can result.

The narrow band filters lead to other more subtle problems. For example, the phase stability and the amplitude flatness can be affected by narrow band filters. Additionally, narrow band filters have large group delays which can cause instability if they are used in feedback paths.

1.3.1.4 Frequency Mixing

Frequency mixing utilizes a mixer to multiply two signals together, generating a signal that contains both the sum and the difference of the two input frequencies. Typically only one of these two frequencies is desired. This type of synthesizer has very good noise performance and the same stability as the reference oscillator. Frequency mixing is accomplished by using a nonlinear element such as a diode or a transistor and exploiting the nonlinearities to perform the mixing action. Unfortunately, the nonlinearities tend to produce a signal that contains many spurious tones at various mixing products with the final signal will be a combination of many frequencies with the form:

$$nf_a \pm mf_b \tag{1.1}$$

These spurious frequencies are the basic disadvantage of frequency mixing. Filtering can be used to eliminate these spurs, but can do so only at the price of a narrow frequency range. A wide-band solution to reducing unwanted spurs is to use balanced mixers or quadrature mixers. Quadrature mixers can be easily integrated

and can attenuate spurious frequencies from 20 to 50 dB.

1.3.2 Indirect Analog Synthesis

Indirect synthesis utilizes an oscillator controlled by a Phase Lock Loop (PLL) to generate its output frequency. This frequency can be the extracted clock from a data sequence or it can be a multiple of the reference clock. The PLL can also be used to track a slowly varying signal to perform an FM demodulation. The Phase Locked Loop (PLL) is an attractive alternative to frequency synthesis because it is relatively easy to design, requires few components, many of the components are simple digital circuits, and it is easily integrated.

1.3.2.1 General Phase Locked Loop

Frequency synthesizers that employ one or more PLLs may appear intimidating and difficult to understand. An intuitive understanding of the PLL operation can be explained by converting the PLL section to the general form given in Figure 1-1. Here, the method of frequency translation is not specified and can be anything from a simple digital divider to a single sideband modulator that contains its own PLL. The PLL tunes the Voltage Controlled Oscillator (VCO) until the phases and the frequencies of the signals applied to the Phase Detector (PD) are equal. Expressions are given for the output of the frequency translation devices.

$$f_{ref} = F_r(f_{in}) \qquad f_2 = F_2(f_{out}) \tag{1.2}$$

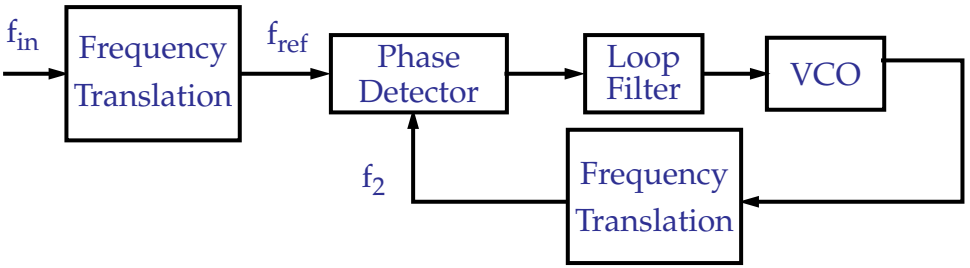


Figure 1-1 Phase Lock Loop Block Diagram

Once the system is 'locked', the output frequency is easily calculated by equating the signals at the input of the PD, yielding the expression in (1.3).

$$f_{ref} = f_2 \quad \rightarrow \quad F_r(f_{in}) = F_2(f_{out}) \tag{1.3}$$

Another advantage of the PLL is the noise suppression it provides. For close-in phase noise, the noise performance of the output signal follows that of the reference oscillator. Any noise outside the bandwidth of the loop is not suppressed and the output signal of the PLL will follow that of the VCO. If the PD has low noise sidebands, the phase noise well within the bandwidth of the loop is given by:

$$\Phi_{\theta oi}(f) = \Phi_{\theta i} \cdot N^2 \qquad f < \frac{\omega_2}{2\pi} \tag{1.4}$$

Where N is the divide ratio of any divider in the feedback path of the PLL.

The major disadvantage of the PLL is the long time it takes to switch from one output frequency to a different output frequency. The switching-speed is limited to ten times the period of f_{ref} (defined in Figure 1-1). This limit arises from setting the PLL bandwidth no wider than one tenth of the reference source. The filter

cannot be widened because of the need to filter the reference source feed-through and to ensure that the loop is stable.

The PLL with an integer divider has a resolution equal to f_{ref}, the signal applied to the input of the PD. For fine resolution, this implies a very low frequency. Because the loop bandwidth can be no larger than one tenth f_1, switching-speed performance will be very poor. Further, the loop will provide less noise suppression to the VCO. For acceptable performance, a low noise VCO is required.

An indirect synthesizer similar to the PLL is the Frequency Locked Loop (FLL). In the FLL, a Frequency Detector (FD) is used to measure the difference in frequency between f_{ref} and f_2. The loop uses this information to tune the VCO until $f_1=f_2$.

The PLL is much more popular in synthesizer applications than the FLL because it has many advantages. The Phase Detectors (PD) used in PLLs are easy to implement using digital techniques, while FDs are narrow-band devices and will only work correctly if the frequencies of the two input signals are within the operating range. Noise in a PLL is converted to phase noise while noise in a FLL is converted to frequency noise. Finally, tighter lock is maintained by a PLL than a FLL because the loop is locked to the phase rather than the frequency of the oscillator.

1.3.2.2 Basic PLL

In a basic PLL, the frequency translation device is a frequency divider,

typically implemented with a digital counter. In Figure 1-2, the reference frequency is divided by M while the output frequency is divided by N.

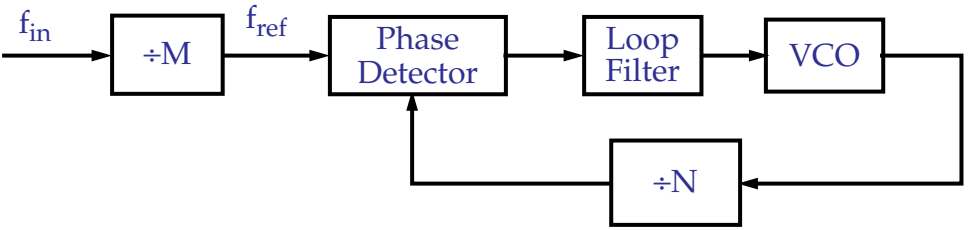


Figure 1-2 Basic PLL Block Diagram

The PLL forces the VCO to oscillated at a frequency where the two divided signals are equal. This relation is given in equation (1.5).

$$\frac{f_{in}}{M} = \frac{f_{out}}{N} \tag{1.5}$$

Solving for f_{out} yields the standard expression for the synthesized signal:

$$f_{out} = \frac{N}{M} \cdot f_{in} \tag{1.6}$$

The basic PLL provides many advantages in a wireless environment. All of the components are easily integrated, low power dissipation is possible, and if the VCO is relatively quiet, good noise performance is possible. However, this loop still has a poor switching time.

1.3.3 Direct Digital Synthesis

A Direct Digital Synthesizer (DDS) produces a smooth, sine-like signal by combining a sine look-up table and a Digital to Analog Converter (DAC). A stable source (such as a crystal reference) clocks a phase accumulator which provides the

‘index’ to the sine look-up table. The sine look-up table is stored in a ROM. The output of the look-up table goes to a DAC and is converted to a stepped sine wave.

This type of architecture offers low levels of spurious tones and low phase jitter. In addition, it can quickly switch output frequencies and provide an output that is phase continuous. However, because it is very complex, it can only be used for slow frequencies with a reasonably low power dissipation.

1.3.4 UCLA Local Oscillator Architecture

The architecture chosen by UCLA must meet all of the requirements for a Frequency Synthesizer in the wireless environment. It must be completely integrated, have low levels of phase noise, a fast switching speed, and a fine frequency step size. While a PLL meets many of these requirements, it falls short in terms of providing both fine frequency step size and fast switching speeds. These features can be achieved only in expensive implementations [3].

By combining the fine frequency step size and fast switching speeds of the DDS with the low noise, high frequency output of the PLL, all of the system requirements can be met. An example of such an architecture is shown in Figure 1-3.

Unfortunately, the sum and the difference of the input frequencies appear at the output of the mixer. A sharp, narrow-band filter could be used to select the desired output or quadrature mixers can be used as in Figure 1-4. Due to the good matching that is available on an integrated circuit, it is expected that the undesired

sideband will be suppressed by 40 dB.

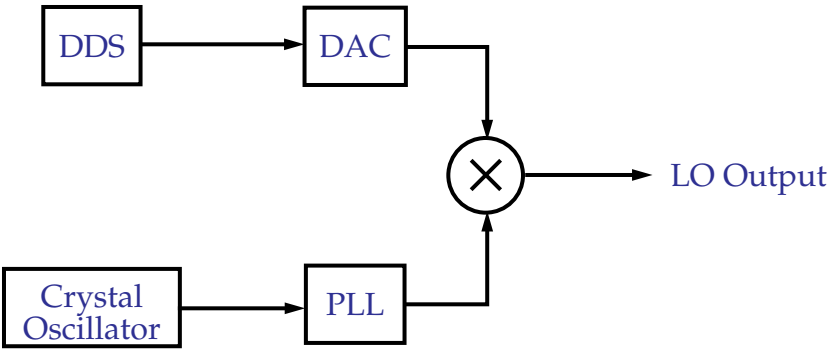


Figure 1-3 Local Oscillator Block Diagram

It is possible to choose either the upper or the lower sideband, depending upon whether the outputs of the mixers are added or subtracted. The subtraction operation can be moved back to the DDS where it is easily implemented by toggling a sign bit. Since selection of the upper or lower sideband is possible, the PLL output can be centered in the desired spectrum and the output range of the DDS can be cut to half of the bandwidth of the channel bandwidth, reducing power dissipation and complexity. The entire channel is covered by either selecting the upper or the lower sideband. In the actual implementation, the DDS/DAC combination provides a frequency-agile output from 0-13 MHz and the PLL provides quadrature outputs at 915 MHz. The LO output is capable of hopping from 902-928 MHz.

This implementation is ideal for a Frequency Hopped Spread Spectrum (FHSS) system with a Frequency Shift Keyed (FSK) modulation. The DDS/DAC combination generates an output that contains the data and the hopping pattern, while the PLL provides the carrier frequency for transmission. The Radio

Frequency (RF) output frequency is given by:

$$f_{RF} = f_{data} + f_{hoppingpattern} + f_{915MHz} \tag{1.7}$$

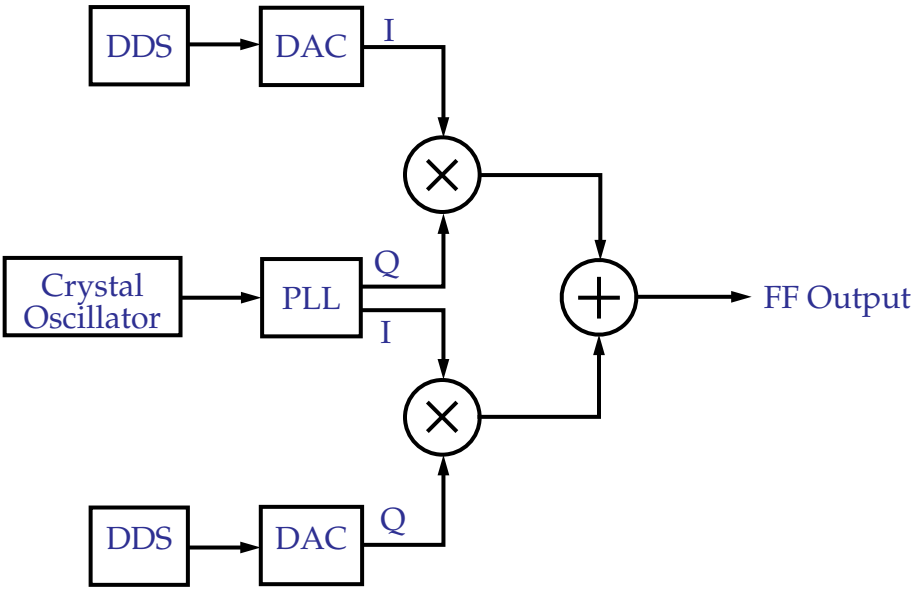


Figure 1-4 Complete RF Block Diagram

If a relaxation oscillator is chosen as the VCO in the PLL, then the LO generator can be completely integrated. The DDS/DAC combination has already been implemented while the PLL is the subject of this work. The complete RF section is presently being readied for fabrication.

Chapter 2

System Noise Specifications

2.1 Introduction

Phase Locked Loops (PLLs) are well understood and so a detailed analysis of their operation will not be covered here. A number of good books are available on this topic [5,14]. Instead, this chapter will discuss the noise in the VCO, the effect of the control loop, and the system requirements for proper implementation.

A PLL is typically composed of a Phase Detector (PD), a loop filter, a Voltage Control Oscillator (VCO), and a Prescaler. The PLL is used to synthesize a higher frequency by comparing the phase of a reference source, typically a crystal oscillator, to the phase of a prescaled version of the VCO. A block diagram of a basic PLL is shown in Figure 2-1. The output of the phase detector is filtered and used to adjust the frequency of the VCO until the two phases are equal or “locked”.

By adjusting the VCO until f_{ref} and f_2 are equal, the VCO output f_{out}, is forced to equal $N \bullet f_{ref}$.

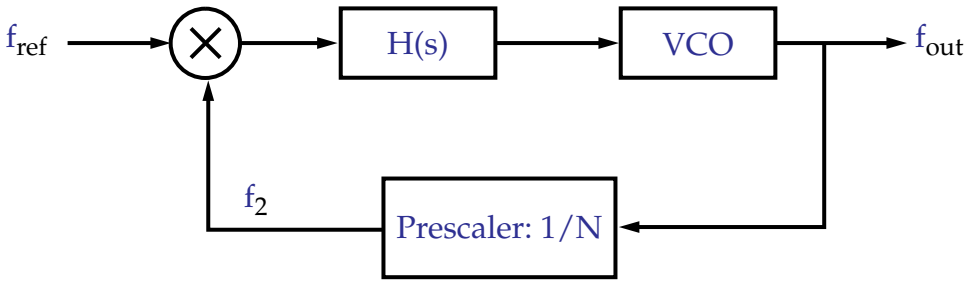


Figure 2-1 PLL Block Diagram

The loop acts to correct any phase and frequency deviation of the VCO due to noise and changes in operating conditions. However, these corrections can only be made up to the bandwidth of the loop and any high frequency noise remains unattenuated. For this reason, the control loop acts as a high pass filter for noise internal to the VCO and as a lowpass filter to noise at the input of the PLL. If there is any noise or changes in the operating conditions that are faster than the bandwidth of the loop, they will appear at the output. Further, purity and stability of the output signal relies on the purity and stability of the crystal reference. Any low frequency noise on the input signal will feed through to the output and up to the bandwidth of the loop.

The sources of noise work out rather well for a PLL. It will be shown that the major source of noise in a VCO is low frequency noise. Further changes in the operating conditions of the circuit, such as the discharging of the supply battery, are also slowly varying. These low frequency noise sources are easily corrected by the

loop. Additionally, because the bandwidth of the loop does not beyond the reference frequency, high frequency noise at the input is attenuated.

To minimize the total (integrated) phase noise, the loop bandwidth should be set to the Fourier (offset from the carrier) frequency where the sum of the unfiltered phase noise spectral density from the reference and the loop electronics equals the free running VCO phase noise spectral density [6].

2.2 System Specifications

The noise specifications for the Local Oscillator (LO) in communication applications are always very strict. An ideal LO has a spectrum of a pure carrier with no noise sidebands. However, every oscillator has noise that degrades the performance of the transceiver. The “close-in” noise degrades the Signal-to-Noise Ratio (SNR) at the output of the demodulator. The higher frequency noise sidebands degrade the adjacent channel selectivity by mixing that occurs due to nonlinearities in the mixer. These occur regardless of the quality of the IF Filter. Noise at even higher frequencies will limit the dynamic range (a measure of the ability to receive weak signals in the presence of strong signals at different frequencies) of the system.

When RF architectures are initially designed, the LO is assumed to be infinitely pure and precise with very good agility. As the design progresses, the LO architecture gains a structure to implement the precision and the agility, but it is still

assumed to be infinitely precise. As the design advances further, the purity of the LO becomes an important issue because it can limit the SNR of the transmitted and received signals, and be the limiting factor in determining how closely spaced (in the frequency domain) two communication channels can be [8]. This section will describe and analyze the effect of finite purity in the LO.

2.2.1 LO Noise in the Receiver

A well-designed Local Oscillator (LO) used in a receiver should not limit the performance of the transceiver. The UCLA architecture requires that the received signal should have an SNR of at least 30 dB. This requirement limits the amount of noise that can be tolerated in the LO. The problem with noise in the LO can be demonstrated by looking at a down-conversion example. A sample channel spectrum is depicted in Figure 2-2. Suppose it is desired to down-convert the signal transmitted by User 3. If User 3 is downconverted by an ideal sinewave, only User 3 will appear at base-band. However, if the LO is not an ideal sinewave, any noise around the LO will down-convert other users to base-band as well. These other users will appear as noise to the detector and degrade the SNR of the received signal.

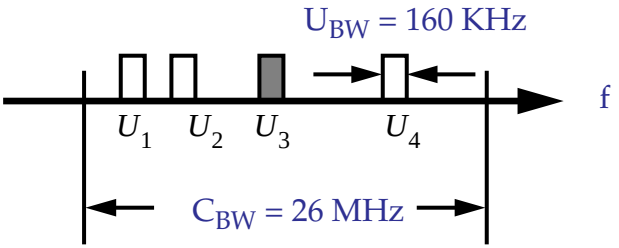


Figure 2-2 Channel Spectrum

All oscillators will have “sideband” noise and so it is important to determine the amount of sideband noise that is acceptable. An idealized power spectrum of an LO is given in Figure 2-3. It consists of an impulse at the desired frequency of operation and flat noise sidebands with a noise density given in dB/Hz below the carrier. The noise sidebands beyond ±26 MHz will not contribute noise because the received signal is base-band filtered and the noise sidebands will be very low this far from the carrier. In an actual LO power spectrum, the noise sidebands will rise up from the noise floor close to the impulse (as indicated by the light gray region in Figure 2-3). These sloping sidebands or “near-in noise” will initially be ignored in this analysis. However, they are very important because they determine the minimum channel spacing by degrading the received signal exactly like the flat noise sidebands.

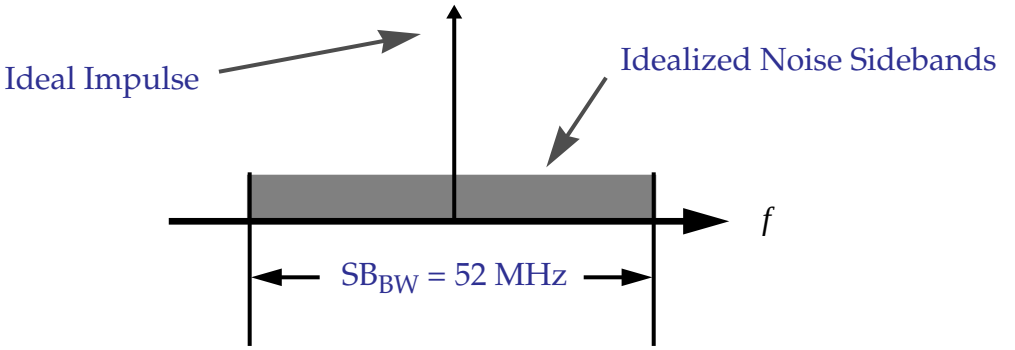


Figure 2-3 Idealized Local Oscillator Power Spectrum

The sideband noise degrades the SNR of the received signal by folding other users onto the desired signal. The other users carry unwanted information and hence act as a noise source that degrades the desired signal. Since the transceiver architecture depends on diversity and not extra power to improve SNR, the average power of all users will be a constant. This assumption becomes more accurate as the number of users increases and is a valid assumption for 50 users. Additionally, the relative level of the desired user to the other users is highly variable and can differ by as much as 36 dB. This variability was accounted for by adding a 15 dB margin to the 15 dB SNR required for reliable transmission. These assumptions calculate the mean noise level requirements. The actual requirements would be a probability distribution about this value.

The total noise folded onto the received signal is given by equation (2.1). The total noise power is the product of the sideband power spectral density (PSD), the user bandwidth, and the number of users.

$$P_{TN} = P_{SB} \cdot U_{BW} \cdot N_{users} \quad (2.1)$$

If the sideband noise PSD is given relative to the signal, then total noise is also given relative to the signal. This is simply the inverse of SNR. The PSD of the noise sidebands can now be defined in equation (2.2). By inserting 30 dB for the SNR, a user bandwidth of 500 KHz, and 50 users, the PSD of the noise sidebands must be 104 dB/Hz below the carrier.

$$P_{SB} = \frac{1}{SNR \cdot U_{BW} \cdot N_{users}} \quad (2.2)$$

2.2.2 Effect of Near in Noise

In the previous section, the Local Oscillator was assumed to have an impulse response at the desired frequency and a flat noise floor limited to a bandwidth about the impulse. In reality, the noise floor is amplified by the oscillator and causes the flat-band noise to rise towards the carrier as in Figure 2-4.

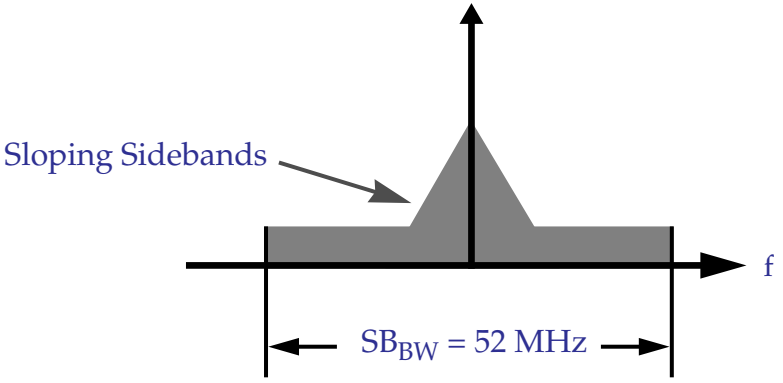


Figure 2-4 More Realistic Local Oscillator Power Spectrum

Since this system is wide-band, the sloping sidebands will fall within the user bandwidth. The sideband noise in the VCOs studied was typically at a

reasonably low level past the channel bandwidth of 500 KHz. As a result, the sloping sideband noise within the user bandwidth will dominate the noise performance of the VCO. If this noise level is very high, the VCO will essentially add so much noise to the received signal that an unacceptable SNR level will result regardless if there are any other users present. To prevent this from happening, the integrated SNR within the channel bandwidth must be at least 40 dB. This completes the specifications of the Local Oscillator. These results are summarized in Table 1.

Table 2.1 Frequency Synthesizer Specifications

Specification	Value
Flat-band Noise Floor	-104 dB/Hz
In Band SNR (500 kHz)	40 dB

2.2.3 Noise Induced Phase

Often, the Local Oscillator specifications are given in the time-domain. Most often this is given as RMS Jitter. This specification defines the instability of the generated signal relative to the reference signal. RMS Jitter is measured by recording the time delay from the zero crossing of the reference to the zero crossing of the generated signal and calculating the RMS value. Jitter is sometimes given in seconds but is usually normalized to the period of the generated frequency and given as a percentage of the period or converted degrees. The following sections describe the relation between a Power Spectral Density (PDS) spectrum and RMS

Jitter.

2.2.3.1 Analytical Method

The ideal LO signal is modeled as an ideal sinusoid without any noise or modulation and is expressed as [5]:

$$v_i = V_i \sin(\omega_i t) \tag{2.3}$$

When noise is added to the signal, both the phase and the amplitude of the LO signal are modulated. The LO with additive noise is given in equation (2.4).

$$v_i + n = (V_i + x) \sin(\omega_i t + \theta_i) \tag{2.4}$$

Since communication circuits require low noise design, the amplitude variations will be small. Further, amplitude variations are not as important as frequency variations in this application because the LO will drive a four FET switch type mixer. These types of mixers are not sensitive to amplitude variations, except at the point where they turn on and off. Additionally, these amplitude variations will be much smaller than amplitude noise contributions elsewhere in the system.

The additive noise affecting the LO is assumed to have passed through a base-band filter, with a bandwidth B_i centered on $\omega_i/2\pi$. If the additive noise was white with a spectral density of N_o, then the filtered noise is given by Φ_n as shown in Figure 2-5.

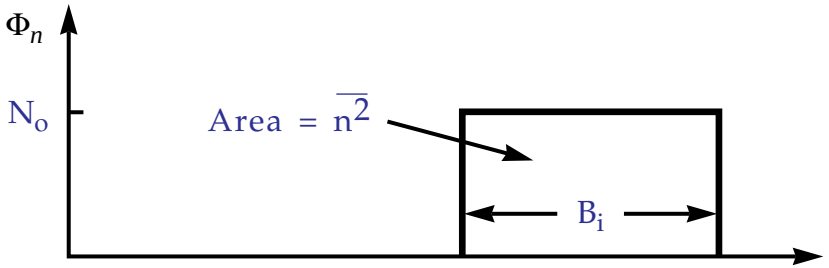


Figure 2-5 Power spectral density of noise components

The total noise power is given by the integral of the noise density in this example is simply the product of the noise density and the bandwidth of the filter. This is given by equation (2.5).

$$\overline{n^2} = N_o B_i \tag{2.5}$$

The additive noise can be broken up into quadrature components as follows:

$$n = n_x + n_y \tag{2.6}$$

and defined in (2.7) where x and y are random variables that change as a function of time.

$$n_x = x \sin \omega_i t \qquad n_y = y \cos \omega_i t \tag{2.7}$$

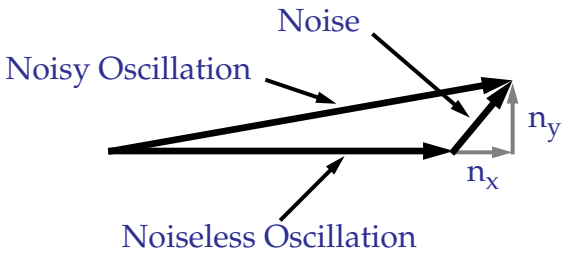


Figure 2-6 Quadrature Noise added to a Noiseless Oscillation

The quadrature noise sources are shown in Figure 2-6 and added in a mean-square sense such that the total noise is given by equation (2.8).

$$\begin{aligned} \overline{n^2} &= \overline{n_x^2} + 2\overline{n_x^2}\overline{n_y^2} + \overline{n_y^2} \\ &= \overline{n_x^2} + \overline{n_y^2} \end{aligned} \tag{2.8}$$

When the sin and cos functions were established in equation (2.7), the phase reference was arbitrary and so $\overline{n_x^2} = \overline{n_y^2}$. Using this equality in (2.5) and (2.8), the total power for each component is given as:

$$\overline{n_x^2} = \overline{n_y^2} = \frac{\overline{n^2}}{2} = \frac{N_o B_i}{2} \tag{2.9}$$

Since each quadrature component occupies the same bandwidth as the original filtered spectrum, the density of each is simply $N_o/2$. The noise expressed as n_x results in amplitude modulation of the LO while n_y results in angle modulation of the LO. The power of the random time functions x and y can be evaluated by equating the power of the quadrature component with the mean-square value of the time function:

$$\overline{n_x^2} = \overline{(x \sin \omega_i t)^2} = \overline{x^2 (\sin \omega_i t)^2} = \frac{\overline{x^2}}{2} \tag{2.10}$$

Since (2.9) gives the noise power of a single quadrature component to be $N_o B_i/2$, the power of the random time functions is given by equation (2.11).

$$\overline{x^2} = \overline{n^2} = N_o B_i \tag{2.11}$$

Returning to the original expression of the ideal LO with additive noise, the random time functions are substituted for n.

$$\begin{aligned} v_i + n &= V_i \sin\omega_i t + x \sin\omega_i t + y \cos\omega_i t \\ &= (V_i + x)\, \sin\omega_i t + y \cos\omega_i t \end{aligned} \tag{2.12}$$

For small angle variations due to *y*, (2.12) can be expressed as:

$$v_i + n \approx (V_i + x)\, \sin(\omega_i t + \theta_i) \tag{2.13}$$

Where θ_i is given by:

$$\theta_i = \operatorname{atan}\left(\frac{y}{(V_i + x)}\right) \approx \operatorname{atan}\left(\frac{y}{V_i}\right) \approx \frac{y}{V_i} \tag{2.14}$$

A relation with the original noise density can be found by calculating the mean-square value of the angle modulation. The power of y as expressed by (2.11) is substituted into the squared and averaged value of equation (2.14).

$$\overline{\theta_i^2} = \frac{\bar{y}^2}{V_i^2} = \frac{N_o B_i}{V_i^2} \tag{2.15}$$

By examining equation (2.15), it is clear that the jitter of the LO given in radians is just the inverse of the Signal-to-Noise Ratio (SNR) which is equal to the integral of the noise spectrum normalized to the amplitude of the output signal. This relation is very convenient when comparing different oscillations when a PSD is not available.

2.2.3.2 Slope Method

An alternative method to determining the RMS jitter of a signal from the

PSD is given in the work by Abidi [9]. Here it is assumed that any amplitude noise around the zero crossing of a sinewave is attenuated by the slew rate of the sinewave.

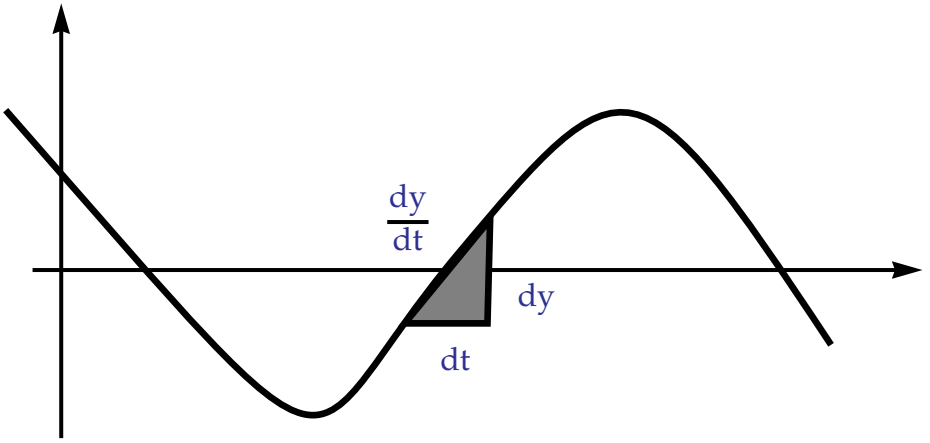


Figure 2-7 Sinewave Modulated by Noise

The LO is given by equation (2.16), a sine function with an amplitude of V_i and a frequency of oscillation f_i.

$$v_i = V_i \sin(2\pi f_i t) \tag{2.16}$$

By differentiating this function, the slope of the function can be calculated when the function crosses zero.

$$\frac{dy}{dt} = V_i \, 2\pi f_i \cos(2\pi f_i t) \tag{2.17}$$

The cosine function is equal to unity when the function crosses zero.

$$\frac{\Delta y}{\Delta t} = V_i \, 2\pi f_o \tag{2.18}$$

Solving this relation for radians:

$$2\pi f_o \Delta t = \frac{\Delta y}{V_i} \tag{2.19}$$

By squaring and averaging, the jitter is once again given by the inverse of the SNR and is expressed in equation (2.20).

$$\overline{\theta_i^2} = \frac{\Delta y^2}{V_i^2} = \frac{1}{SNR} \tag{2.20}$$

For example, take SNR = 30 dB = 31.6 and f_o = 915 MHz. The normalized RMS jitter is 2.83%.

2.2.3.3 Leeson's Model

Leeson has developed a simple model to describe the noise of oscillators with high Q resonators [15]. The oscillator is modeled as an amplifier with a resonant circuit as a feedback element as shown in Figure 2-8. The peak of the resonant circuit is normalized, requiring the amplifier to have a gain of 1 for oscillation to occur. The noise of the amplifier is described as a spectral density and is referred to the input. As the noise passes through the resonator, energy near the resonant frequency will be amplified due to transfer function of the resonator circuit. This model predicts a phase noise spectrum that is flat at high frequencies with the PSD of the amplifier. At low frequencies, the resonator begins to amplify the noise and the sidebands begins to rise at 20 dB/decade. Finally when the frequency is lowered to the point where the noise of the amplifier is dominated by *1/f* noise, the sidebands rise at 30 dB/decade. The frequency where the noise rises

above the flat noise floor decreases when a larger Q is chosen to improve the noise performance.

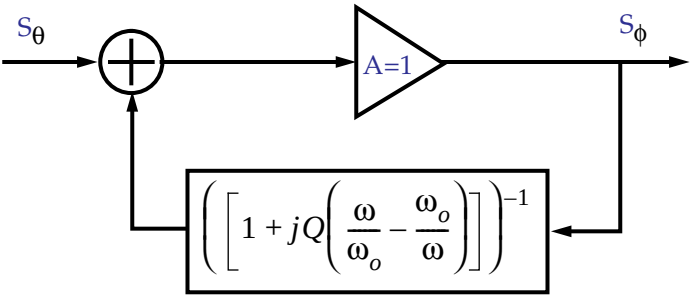


Figure 2-8 Leeson Oscillator Noise Model

2.3 PLL Noise Reduction

If a VCO is not placed in a PLL, its output frequency will tend to wander due to both noise in the internal circuits and environmental changes. The PLL makes adjustments to suppress the noise sources and the environmental variations. This noise suppression is shown in Figure 2-9.

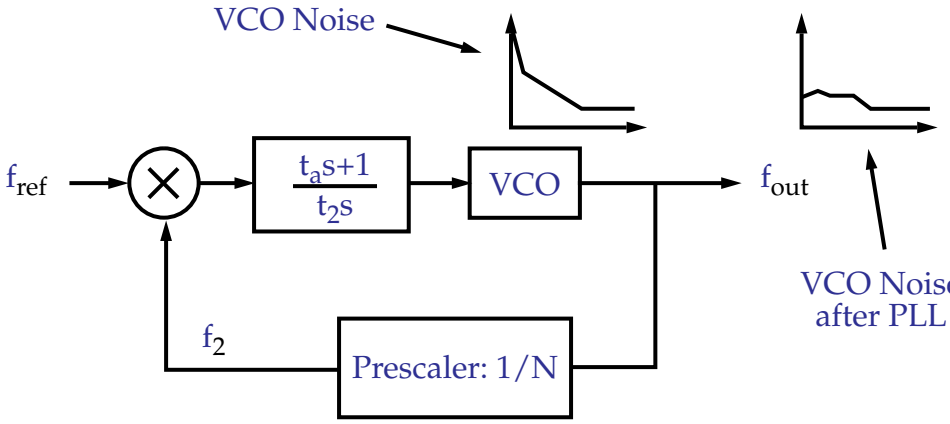


Figure 2-9 Phase Noise Suppression by a PLL

The output of the PLL is calculated by subtracting the noise attenuation of the PLL from the VCO noise spectrum. A typical VCO phase noise plot based on

Leeson's model is given in Figure 2-10 [15]. This plot shows the amount of energy as a function of frequency away from the carrier. For frequencies far from the carrier, the noise is flat and defined as the noise floor of the VCO. As the distance to the carrier decreases, the noise rises from the noise floor at 20 dB/decade. The frequency where the noise begins to rise depends on the effective "Q" of the oscillator and is shown as f_d. At even lower frequencies, the 1/f noise of transistors causes the VCO to wander even more and the noise spectrum begins to follow a 30 dB/decade slope at f_b.

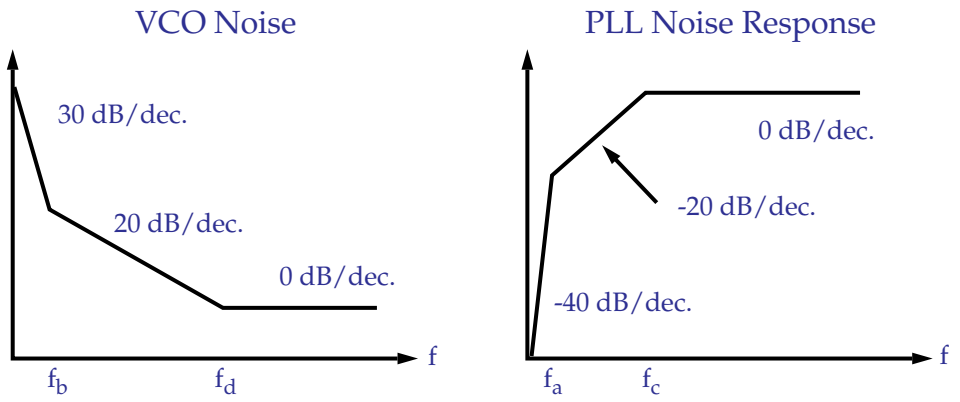


Figure 2-10 VCO Noise Spectrum and PLL Noise Response

The PLL suppresses the VCO noise by adjusting the control voltage to cancel the variations. The PLL noise response is also given in Figure 2-10. At very small offsets from the carrier, the PLL suppress the noise at -40 dB/decade. This is due to the two poles in the PLL system (the pole in the integrator and the pole in the VCO). The response changes when the PLL encounters the zero placed in the loop for stability. This occurs at f_a. From this point until the edge of the PLL bandwidth, the noise response follows a -20 dB/decade response. Beyond the bandwidth of the

loop, the noise passes unattenuated. A composite between the VCO noise spectrum and the PLL noise response is given in Figure 2-11.

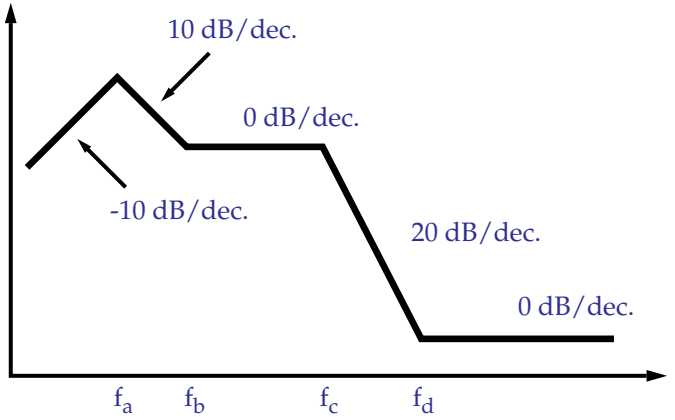


Figure 2-11 VCO Noise after PLL Noise Suppression

Chapter 3

PLL Circuit Elements

3.1 Voltage Controlled Oscillators

Although many types of Voltage Controlled Oscillators (VCO) are available for use in wireless transceivers, many of them are not suitable for this application. The characteristics of the following three types of oscillators are summarized in Table 3.1: crystal resonator oscillators, LC tank oscillators, and multivibrator oscillators.

While crystal oscillators provide the purest signal, they are limited to low frequency operation and have a narrow tuning range as was described in Section 1.3.1.1. The crystal oscillator's inability to be modulated by noise is reflected in the limited tuning range.

The LC tank oscillator provides very good noise performance but typically

Table 3.1 Characteristics of Oscillators

Type	Noise Performance	Output Frequency	Tuning Range
Crystal	Very Good	Low Frequency	Very Narrow
LC Tank	Good	Limited by Active Devices	Narrow
Multivibrator	Poor	Limited by Active Devices	Very Wide

requires either external components or an exotic manufacturing process. Oscillators with integrated LC tank resonators take advantage of varactor diodes to tune the frequency of oscillation by adjusting the capacitance of the resonator. There has been some work to integrate a tunable LC VCO by interpolating between two different tank resonators [16]. A limit on the tuning range is required to prevent simultaneous oscillation from occurring at the resonate frequency of each individual tank circuit.

Finally, a multivibrator oscillator provides the widest tuning range of the other oscillators. The ring oscillator type of multivibrator oscillator has the highest frequency of operation. With proper design and a technology with well-controlled process variations, the ring oscillator will be able to overcome process and environmental variations by adjusting the control voltage of the VCO. In addition, this oscillator does not require any external components. The disadvantage to this oscillator is the poor spectral quality of the output signal.

Since a Single Side Band (SSB) modulator is used in the transceiver,

quadrature outputs are required from the VCO and are readily available from a four stage ring oscillator. If quadrature outputs are not provided naturally by the oscillator, they can be generated by using a standard RC-CR circuit. The amplitudes of the quadrature channels are frequency dependent and do not match each other very well. However, in this application, amplitude matching is not too important because FET mixers will be used. If amplitude matching is important, a polyphase RC-CR filter can be used [24]. In this filter, the amplitudes match very well for almost a decade in frequency.

3.2 Dividers and Prescalers

The term “prescaler” is used to describe a non-programmable divider with a high operating frequency. The prescaler is used to minimize the power consumption of the programmable divider, allowing the use of higher VCO frequencies. Unfortunately, high speed prescalers are typically constructed in a fast logic family like Bipolar ECL.

The prescaler is the feedback element that forces the VCO output to be a multiple of the reference frequency. Just as in any negative feedback system with enough forward path gain, the transfer function reduces to the inverse of the feedback element. In the case of the PLL, this forces the input frequency to be scaled by the prescaler divide ratio.

A problematic situation can occur if the maximum operating frequency of

the VCO is faster than that of the prescaler. For example, if the VCO begins oscillating at a frequency beyond the range of the prescaler, the output of the prescaler will either be a constant or possibly a divided version of its own natural frequency, both of which would be slower than the reference frequency. The loop would respond by forcing the VCO to oscillate faster until the integrator output becomes saturated and the VCO is trapped, operating at its highest output frequency. Because the prescaler must operate at a higher frequency than the VCO, this circuit is not trivial, especially if the technology requires a large effort to get the VCO to operate at these speeds. The speed of the prescaler is the ultimate limit in the design of integrated frequency synthesizers.

3.2.1 Ripple Counter

There are three types of digital counters used as frequency dividers: asynchronous (or “ripple”) counters, synchronous counters, and dual modulus counters. Ripple counters are relatively simple, low-power circuits which are generally used as fixed frequency dividers. However, because the signal ripples through each of the stages sequentially, these counters can have relatively high levels of phase instabilities. In certain applications, these instabilities can be cleaned up by following the prescaler with a flip-flop clocked by both the counter output and the input source [6].

The most basic prescaler is a simple D-latch flip-flop (DFF). By connecting the inverting output of the DFF to the input, the clock is forced to sample the inverse

of the latch's present state, resulting in an oscillation that is allowed to occur only at the rising edge of the input clock. This simple divide-by-two cell is typically cascadable and requires the least amount of circuitry, resulting in the highest operating speeds and the lowest power dissipation.

The DFF has implementations in many different logic families and even a few specialized circuits. The CMOS logic family provides the most popular latch with the advantage of having no static power dissipation and being readily available in any digital cell library. Unfortunately, it requires a large swing at its input which can be difficult to provide at high frequencies (915 MHz). Further, the CMOS latch has a very slow maximum operating frequency, making it unsuitable for this application.

Dynamic logic families have been developed for areas where the speed of CMOS logic is inadequate. In an attempt to simplify dynamic logic families and provide high operating speeds, True Single Phase Logic (TSPL) was developed [17]. It has been a popular choice for high speed dividers with input speeds as high as 1.16 GHz being reported [18]. The speed of the standard TSP latch has been increased by switching the position of the clocking transistor and the inverter transistor. This improvement was made in the third section by Rogenmoser [18] and in the middle section by Fang Lu at UCLA [27]. In addition to being very robust, programs have been written to optimize this rather complicated circuit.

The disadvantages of this divider are exacerbated by the requirements of a

mobile environment. The input requires a moderately large input signal and a rather quick rise time. Both of these requirements are difficult to achieve at 900 MHz. Finally, the TSPL tends to consume a lot of power when operating at high frequencies. A 1.2 μm version operating from a 5 volt power supply consumed 45 mW at 1.16 GHz [18], 1/4 of the total RF power budget.

Bipolar Emitter Coupled Logic (ECL) was successfully adapted to CMOS and GaAs technologies and is considered the fastest logic circuit among GaAs logic circuits [21]. Since FET transistors have a source rather than an emitter, this type of logic is called Source Coupled FET Logic (SCFL). This circuit is biased by a constant current source, so noise currents injected onto the supply line are minimal and the circuit is relatively insensitive to power supply variations. This circuit also has the advantage of having a differential input and output. One major disadvantage of this type of phase detector, however, is that it has the highest levels of phase noise relative to other divider circuits [22].

Other forms of asynchronous dividers include regenerative dividers and injection locked oscillators. These circuits can operate at very high speeds but only over a relatively narrow band of frequencies. Further, these dividers are susceptible to cycle skipping [6]. Because of such limitations, these types of prescalers are not suitable for use in applications that require the oscillator to have a wide tuning range.

3.2.2 Synchronous Counters

The second type of frequency divider is the synchronous counters. These counters tend to have lower levels of phase instabilities, but higher levels of power consumption than ripple counters [6].

3.2.3 Dual-Modulus

The third type of counter is called a dual-modulus or “swallow” counter. This counter uses a high speed divide by N/N+1 counter which is controlled by a lower speed resetable synchronous counter. It is used to produce variable division ratios with relatively low power consumption. Because this circuit typically divides by N and occasionally divides by N+1, it has the effect of dividing by a number somewhere between N and N+1. This is convenient in situations where the PLL is required to synthesize many different frequencies with a fine resolution. The dual modulus counter has the disadvantage of having a minimum division ratio as well as a maximum one, but this is not a problem in many applications [6]. Additional disadvantages with the dual-modulus divider include greater complexity over the DFF and a slower operating frequency. However, its major disadvantages include high levels of spurs and phase jitter [6].

Foroudi has overcome the speed problem by developing a high-speed dual-modulus divider based on a high-speed memory latch [20]. This divider has a high operating frequency but Hspice simulations showed that it was not as fast as the ECL divider and does not take advantage of the differential output of the VCO. The

divider developed by Foroudi is a creative and interesting structure and with some modification may lead to a very fast design. In addition, the thesis by Foroudi is an excellent summary and tutorial in high speed prescaler design.

One method to reduce the high spurious frequencies of the dual-modulus divider is the Digiphase synthesizer [28]. The Digiphase synthesizer keeps track of the long term phase of the reference frequency and of the VCO output. The long term phase information is used to provide a frequency resolution equivalent to a dual-modulus synthesizer while maintaining very low spurious tones and low random phase noise.

The operation of the Digiphase synthesizer is explained by referring to Figure 3-1. The output of a dual-modulus divider is a series of pulses with the average pulse rate equal to the reference frequency. However, instantaneously, these pulses have a different frequency than the reference frequency so an error signal is produced at the output of the PD. The average of this error signal (i.e. the amount of “long term voltage” that remains to tune the VCO) is zero and only serves to create spurious outputs. The Digiphase synthesizer calculates the output pulses of a locked PLL and subtracts it from the actual error signal, attenuating any spurious frequencies due to the dual-modulus division.

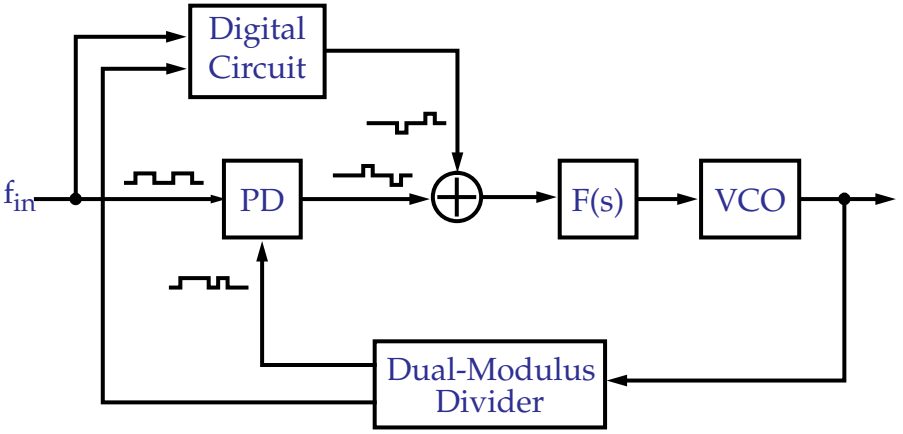


Figure 3-1 Digiphase Synthesizer

Another method to reduce the high spurious tones of the dual-modulus divider takes advantage of oversampling techniques to move the spurious noise away from the low frequency phase information [19]. This method can effectively eliminate spurious frequencies without requiring a Digital to Analog Converter (DAC) or by introducing broad-band noise into the divided signal.

3.2.4 Prescaler Conclusions

Since crystal oscillators are available at almost any frequency, the divide ratio can be a simple power of 2. A divide ratio of 32 was chosen because it is easily implemented by cascading five simple divide by 2 cells together and it results in the highest crystal frequency without selecting a crystal oscillator that operates at a higher mode of oscillation.

3.3 Phase Detectors

Phase Detectors (PD) are often referred to in the literature as Phase Comparators and multipliers. The term Phase Comparator most accurately describes the function of this component. It is not a device that “senses phase”, but rather it compares the phases of two signals and ideally provides a signal that is linearly related to the phase difference. However because the term Phase Detector is the most popular, it will be used in this text. There are many types of PDs to choose from in the design of a frequency synthesizer. A summary of some typical choices are given below.

3.3.1 Multipliers

This type of PD provides a signal that is proportional to the phase difference between two signals by multiplying the two input signals together. This type of PD is sometimes referred to as a linear phase detector. The PD properties of a multiplier can be seen through the following trigonometric identity.

$$V_i \sin(A)\, V_o \cos(B) = 0.5 V_i V_o [\sin(A-B) + \sin(A+B)] \qquad (3.1)$$

For small differences in phase, the sine function can be approximated as (A-B), a signal that is proportional to phase with the gain defined to be $0.5V_iV_o$. The other sine function results in a signal at twice the input signal frequency and is typically removed with a simple filter. The output of this PD is a sine-wave with multiple zero phase values, half with a positive slope and the other half with a negative slope. This

is shown in Figure 3-2. This property allows the user to neglect the relative polarity of the input signals in a multiplier PD because positive feedback will always force the loop past the unstable operating point and towards the stable one.

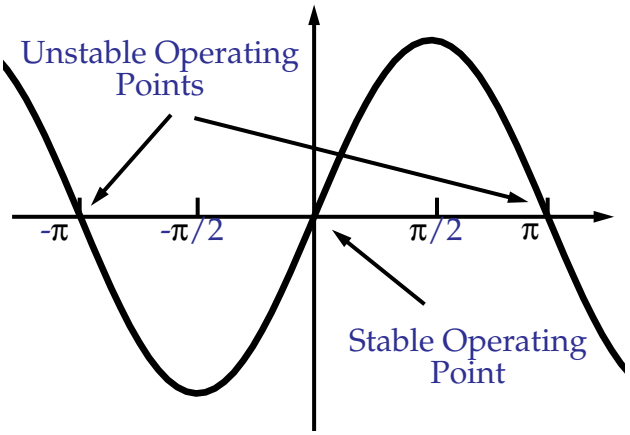


Figure 3-2 Multiplying PD Transfer Function

Except for special applications like low-noise tracking filters, the linear phase comparator is not the best choice for a PD [11, 12] because the gain of PD changes with the amplitude of the input signal. Equation (3.1) shows that the output signal amplitude is directly proportional to the input signal levels due to the multiplying function. If the amplitude of either signal varies due to changes in temperature or power supply voltage, the PD gain will vary as well. These changes will alter the loop characteristics and may cause the loop to become unstable. Additionally, if one of the input signals increases in frequency, the loop will begin to skip cycles and the PD gain will decrease.

It might seem that this PD has an advantage by providing a continuous phase-error signal through a complete cycle, however, if the VCO signal passes

through any type of digital circuit such as a prescaler, the signal will be “squared up” and there will only be phase information at the zero crossings. Further, if the divider does not provide a 50% duty cycle, then the phase information will be valid only on the leading edge.

3.3.2 Exclusive Or Gate

An Exclusive Or (XOR) gate can also be used as a PD. This PD can be thought of as an over driven, multiplying PD with the advantage of having a gain that is independent of the input signal levels. However, many of the disadvantages of the multiplying PD hold for this PD as well.

This type of detector was not chosen because it acts strictly as a phase comparator. This type of detector is not desirable because of its narrow capture range and long settling time. These disadvantages stem from the fact that the detector does not provide much frequency information to the loop. These problems can be overcome by designing a complicated PD that contains two sections. The first section would perform the frequency lock and then turn itself off. The PD would then be switched in to perform the phase lock.

An additional disadvantage of this PD is the large amount of energy the output contains at twice the reference frequency. In fact, in the locked condition, the output of the XOR PD is a square wave with a 50% duty cycle at twice the reference frequency. Unless this energy is sufficiently attenuated, it can modulate the control signal of the VCO, resulting in FM tones about the carrier at this frequency.

3.3.3 Type-Four Phase/Frequency Detector

A type Four Phase/Frequency Detector is a very robust circuit. Not only does it provide a linear input range of 4π radians, it also provides frequency information to the loop. A typical implementation is shown in Figure 3-3.

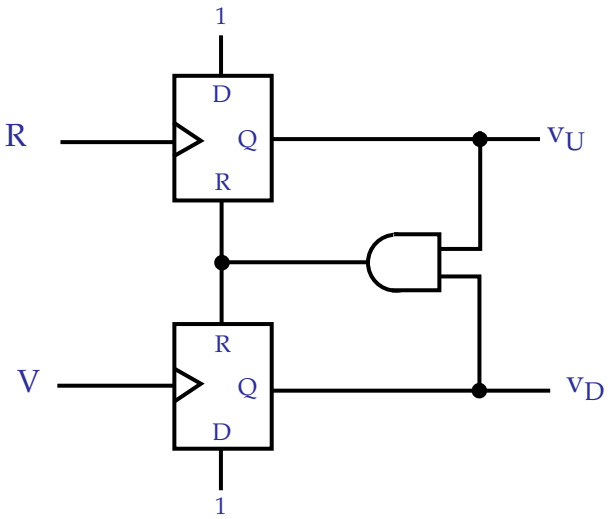


Figure 3-3 Type 4 PD Block Diagram

The operation of this circuit can be describe with a three state machine as shown in Figure 3-4. The rising edges of the input signals cause the circuit to move from one state to the next. If, for example, the state machine was initially in State 2, the output of the PD would be 0 volts and not change the frequency of the VCO. If the VCO increased in frequency, then two rising edges from the VCO might arrive before a single rising edge from the reference. At this point, the state machine would move to State 1, where the output voltage is V_L-V_H< 0. This would decrease

the control voltage to the VCO and slow it down.

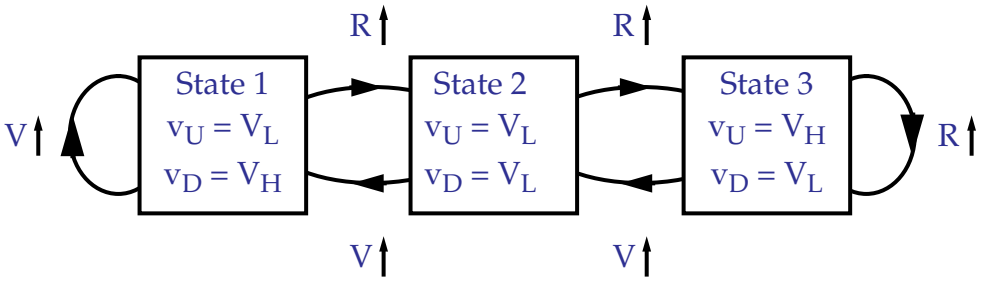


Figure 3-4 Three State Machine

The gain curve of the PD is shown in Figure 3-5. The gain is linear from -2π to +2π and repeats every 4π. The gain is easily calculated to be:

$$K_d = \frac{V_H - V_L}{2\pi} \tag{3.2}$$

At high frequencies, the range of this PD is reduced from ±2π, but the gain remains constant [5,23].

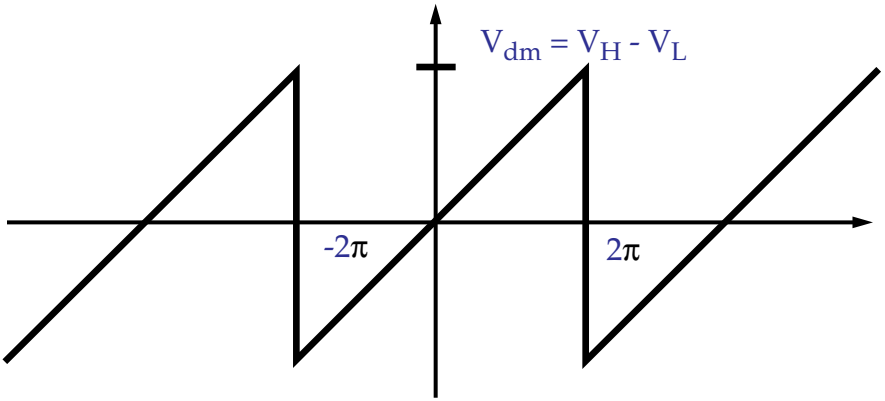


Figure 3-5 Type Four PD Gain Curve

This circuit is not without its disadvantages. One disadvantage is that the phase to voltage transfer function of this phase detector may contain a nonlinearity referred to as a “dead zone”, near the zero phase point. The PD gain at the dead zone

can decrease and even become negative. Since a PLL forces the oscillator to operate in this zero phase region, the loop gain is also reduced (possibly to zero or even crossing over and changing the negative feedback to positive feedback). The result is that the VCO output can wander around this dead zone without sending any error signal to the loop, increasing phase noise [13].

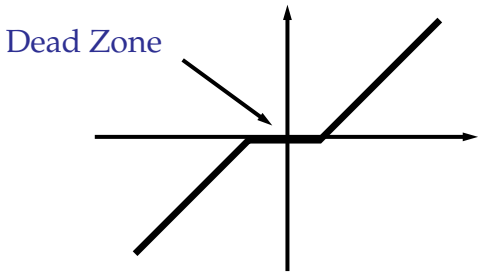


Figure 3-6 Example of Dead Zone in Type Four Gain Curve

A detailed analysis of this effect is given in an application note from GigaBit Logic [13] and is summarized below. In standard operation, one of the outputs will rise on the leading input signal edge and fall when the reset signal propagates through the circuit. When the input signals are near lock, the leading output does not have a chance to reach the full logic level before it is reset. Due to the finite rise time of the internal circuitry, the amplitude of the output signal is dependent on the phase difference between the two signals. Since the width of the output signal is also dependent on the phase difference between the two signals, the area of the output signal is a second order function. A plot of the transfer function is given in Figure 3-7 with the rise time defined as T_r , the fall time as T_f , and the width of the reset pulse as t_d . The running variable being, t_d , the normalized delay of the reset

signal of the PD.

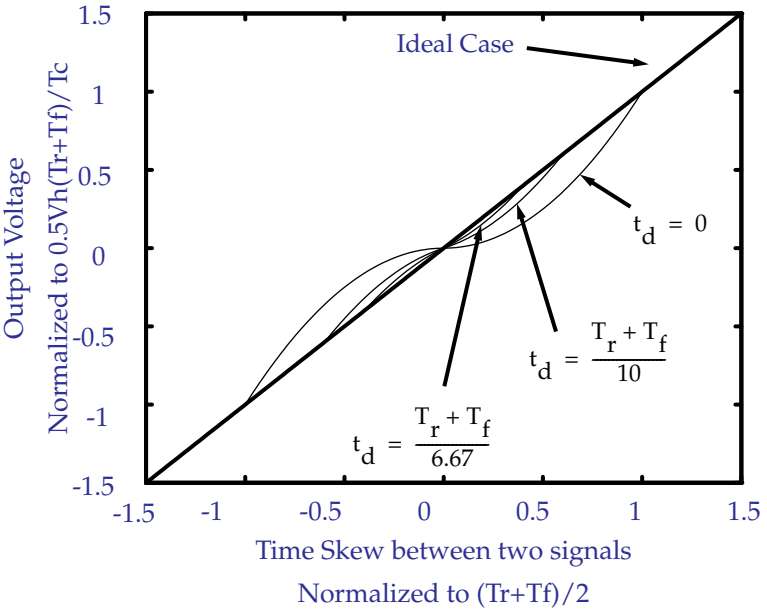


Figure 3-7 Calculated Type 4 Transfer Function

Mijuskovic has reduced the dead zone problem by increasing the width of the reset pulse [29]. From Figure 3-5, it is clear that as the width of the dead zone is inversely proportional to the ratio of the delay time to the rise and fall times the internal circuits. By the increasing this ratio, the nonlinearity is minimized. Mijuskovic accomplishes this by increasing the width of the reset pulse by inserting a string of delay stages between the 4-input NAND and the reset input to the FFs.

While this is a very simple solution to the dead zone problem, there is a major disadvantage with this architecture (and the XOR PD). The problem occurs during the lock condition because the output signal contains energy at twice the reference frequency. This energy will lead to FM spurs about the carrier unless the bandwidth of the loop is reduced to filter these tones, which might not be acceptable

in some applications. Further spurs might cause mixing products that could degrade the SNR of the system.

Analog Devices has extended this idea by coming up with a very simple structure that implements the two loop idea presented in 3.3.2 [25]. This architecture is implements with four D-flip-flops and an XOR gate. The first two flip-flops provide the same frequency information as in the standard Type Four PD. However, as the phase error approaches π, the frequency acquire aid is turned off and a standard XOR gate is switched in with a NAND gate to provide the phase information.

This is a very robust design that is easily integrated on any CMOS process and only consumes slightly more power and area than the Type Four architecture, but it once again trades the non-linearity for increased energy at twice the reference frequency.

3.4 Loop Filter

Digital modulation schemes have very demanding noise specifications and require a very clean LO signal. To appropriately suppress the noise of the VCO, a second-order loop is required. A digital phase-frequency detector was chosen because an integrator is easily implemented into the charge pump circuit that typically follows the PD. Implementing the integrator in the charge pump instead of with an op amp reduces power dissipation and complexity.

Chapter 4

Circuit Design

4.1 MOSFET Model

Below is a brief review of the MOSFET model used in this design. This model is reviewed to avoid confusion due to variable names. The drain current in the MOSFET has a square law dependency on its gate voltage as given by equation (4.1). This model does not hold for short channel devices but provides a starting point for a design that will always end in SPICE.

$$I_D = \begin{cases} K\frac{W}{L}(V_{gs}-V_t)^2 \\ K\frac{W}{L}V_{gt}^2 \end{cases} \qquad K = \frac{\mu C_{ox}}{2} \tag{4.1}$$

Where $V_{gt} = V_{gs} - V_t$. The threshold voltage V_t varies as the source substrate bias

voltage V_{SB} varies. This variation is described by:

$$\lambda = \frac{\partial V_T}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_F}} \tag{4.2}$$

The transconductance of the transistor is given in equation (4.3).

$$g_m = \begin{array}{c} 2\sqrt{K\frac{W}{L} I_D} \\ \frac{2I_D}{V_{gs} - V_T} \\ 2K\frac{W}{L}(V_{gs} - V_T) \end{array} \tag{4.3}$$

Noise in the transistor is composed of thermal noise and flicker noise. The thermal noise is flat with frequency while the flicker noise has a 1/f shape in the frequency domain. The noise currents in the transistor are given below.

$$\begin{aligned} i_{therml} &= \sqrt{\frac{8kT \cdot g_m}{3}} \\ i_{flicker} &= \sqrt{\frac{K_F \cdot g_m^2}{C_{ox} W_{eff} L_{eff} f^{A_f}}} \end{aligned} \tag{4.4}$$

4.2 FS Block Diagram

Since many different circuits need to be tested, the FS chip must be designed to evaluate different sections independently. The FS chip block diagram is shown in Figure 4-1. It consists of a digital PD followed by a charge pump. The load applied to the charge pump can be selected between an on chip load or an off chip

load through the analog multiplexor. The filtered control signal passes from the CP to a differential-to-single ended converter. Another analog multiplexor is present at the VCO control voltage input. This multiplexor allows the VCO to be controlled either from the on chip PLL or from an external PLL. The external PLL allows the evaluation of different filter characteristics.

One pair of the VCO's outputs drives an on chip prescaler. The other outputs drive a cascaded chain of differential buffers that increase in size until they are capable of driving a large open drain device. The output of the prescaler is feedback to the PD.

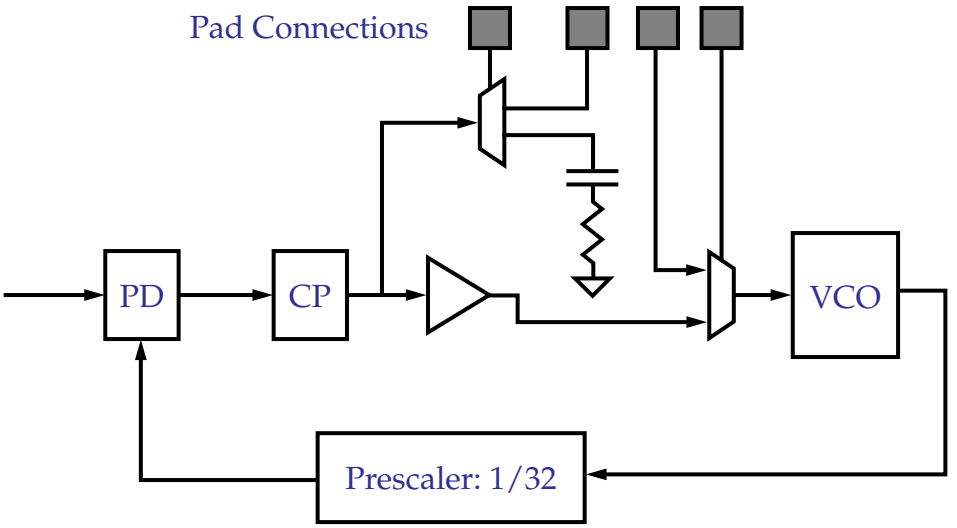


Figure 4-1 FS Chip Block Diagram

4.3 Voltage Controlled Oscillator

One goal of the transceiver design is to eliminate all external components. To achieve that goal, a four stage ring oscillator was chosen. In addition to providing quadrature signals without extra circuitry, it has the highest operating

frequency of any regenerative VCO. Finally, this circuit also provides a wide tuning range and differential output cells.

The ring oscillator is constructed by connecting four differential delay cells in ring as shown in Figure 4-2. Each delay cell provides a delay of 45° for a total delay of 180°. The additional 180° comes from the cross connection between the second and third delay cells. Two pairs of quadrature signals are available at opposite sides of the ring oscillator.

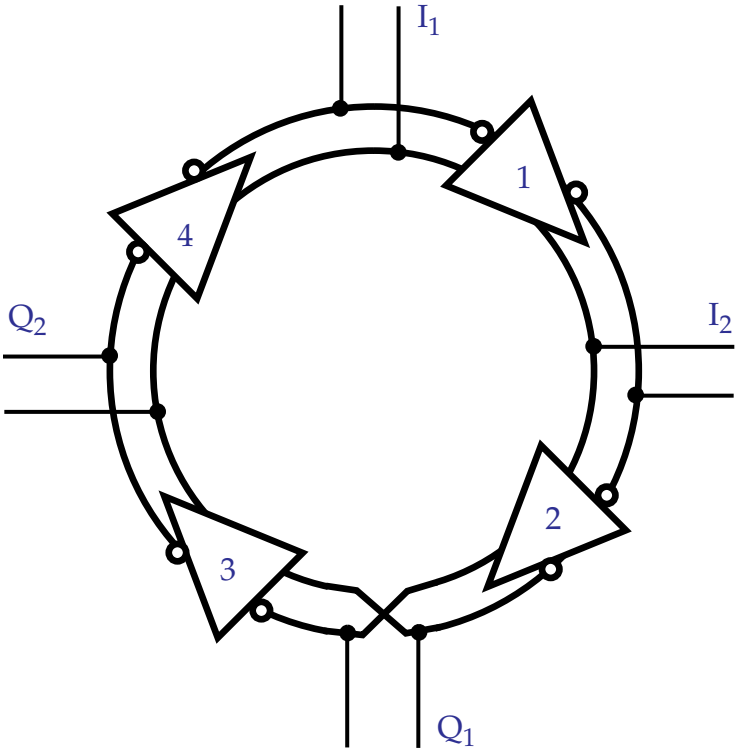


Figure 4-2 Four Stage Ring Oscillator

4.3.1 Delay Cell

The delay cell used in the design is a differential pair with an NMOS load and is shown in Figure 4-4. In normal operation, a constant-gain bias circuit will set

the voltage of the current source and the PLL will control the voltage at the gate of the PMOS transistor to adjust the frequency of oscillation.

The initial analysis will ignore the effect of the PMOS transistor. A complete expression for the oscillation frequency is difficult to solve due to the many non-linear elements that are involved. However a simple expression can by obtained by examining the phase delay per stage of the ring oscillator. Each delay stage must provide 45° of phase shift, which occurs exactly at the dominant pole of the amplifier. The position of the pole location is approximated by time constant of the load capacitance at the output node and the effective bias resistance of the load device. This is given in equation (4.5).

$$f_o = \frac{g_{m3}}{2\pi C_L} \tag{4.5}$$

This approximation does not predict the amplitude of the oscillation or the asymmetry of the output signal. A complete model would predict the delay as a combination of the time it takes for the load device to pull up the output node, including the effect of the changing transconductance, and the time required to discharge the output node by the bias current source. A similar analysis was performed by Bayruns for a simplified case [30]. This analysis is accurate when the output swings to the full logic levels. In the case of the ring oscillator, as the load device is pulling up the output node, the input device is being switched, pulling the output node down again.

Since the delay is composed of an RC time constant, and a slew rate type behavior, it is important to calculate which effect dominates the delay of the cell. If the delay is dominated by the RC time constant, then the delay of a resistive load device would be independent of the bias current. Figure 4-3 shows the results of a simulation comparing output frequency versus the bias current for an NMOS load VCO and a resistive load VCO. While the delay of the resistive load is not independent of the bias current, it is 2.4 times less sensitive than the NMOS load and confirms the RC delay model. This model was used in design various VCOs and it was found to predict the frequency of oscillation very well.

The delay variation of the resistive load delay cell is due to the output signal not increasing linearly with the bias current. If the amplitude of the output node increased linearly, the slew rate period of the transition would be independent of the bias current.

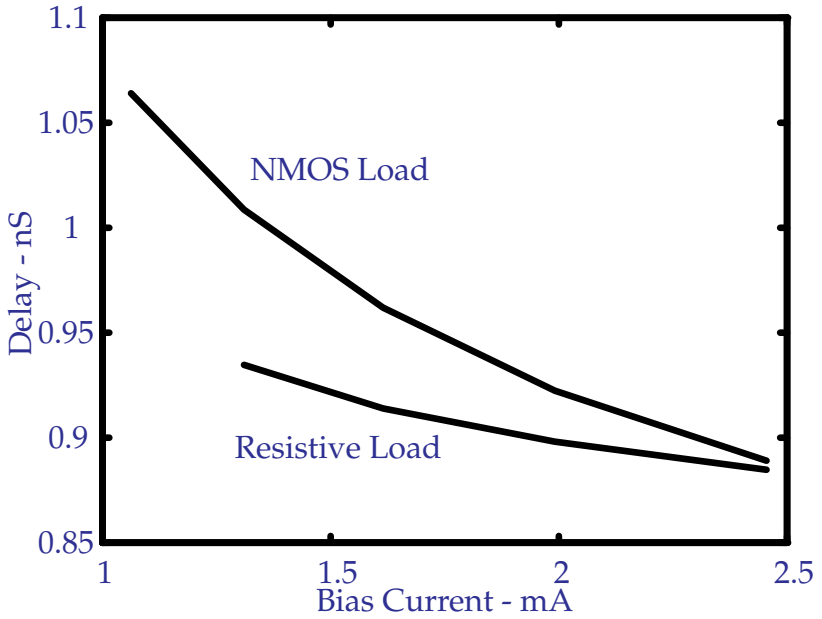


Figure 4-3 NMOS and Resistive Load VCO Delay Characteristics

If it is assumed that the RC models the delay fairly accurately, then an expression similar to the common expression given for regenerative oscillators ($f_o=I/[8\Delta VC_L]$) can be formed.

$$f_o = \frac{2I}{2\pi V_{gt} C_L} \tag{4.6}$$

By substituting V_{gt} from equation (4.1) into (4.6), it is found that there is actually a square root relation between the frequency of oscillation and the bias current. This has been confirmed by simulation.

$$f_o = \frac{\sqrt{K\frac{W}{L}I}}{\pi C_L} \tag{4.7}$$

At high oscillation frequencies (i.e. at high bias currents) it is very difficult

to get a ring oscillator to generate an even higher output frequency.

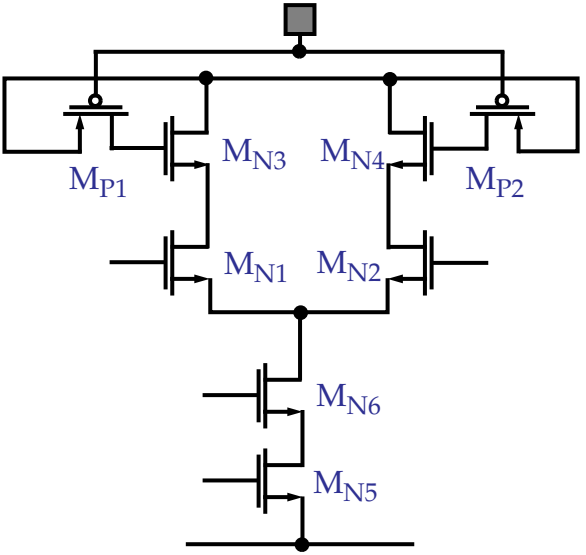


Figure 4-4 Delay Cell

The first step in designing the ring oscillator is to guarantee the delay cell has a gain greater than 1 when the phase is equal to 45°. This small-signal analysis guarantees that there will be enough gain for oscillation to begin during start-up. Since the voltage gain is equal to 0.707 of the DC gain when the phase is equal to 45°, the DC gain should be greater than 1.41. This is accomplished by making the ratio of $W_1/W_3 > 2$.

The single ended output swing is easily calculated. The high voltage of the output swing occurs when all of the current is switched to the opposite side of the differential pair. When this occurs, the output node is at V_{DD}-V_t. The low voltage of the output swing occurs when all of the voltage is switched back. At this point, the output node is at a voltage of V_{DD}-V_{gs}. The output swing is defined as the difference between the high and the low voltages and is equal to V_{gt}.

$$\Delta V = \frac{(V_{DD} - V_t) - (V_{DD} - V_{gs})}{V_{gt}} \tag{4.8}$$

Many of properties of the delay cell depend on the effective voltages, V_{gt}, of each transistor. For example, for low noise operation, the V_{gt} of the current source should be as large as possible. However, with a large V_{gt}, the bias transistor can easily move into the triode region at high current levels, resulting in common-mode oscillation. The oscillation is described as a common-mode oscillation because the differential outputs of the delay cell move together. The common-mode (CM) oscillation occurs when the CM gain becomes greater than unity and common-mode noise is amplified as it propagates through the loop. Since the CM gain is equal to the load resistance divided by the resistance of the current source, CM oscillation can be prevented by insuring the bias transistor is in saturation. Further, the effective voltages of the transistors in the differential pair must also be maximized due to noise considerations. In summary, the effective voltages for all of the transistors in the delay cell pair must be maximized for a given current without allowing any transistor to enter triode.

The cascode transistor M_{N6} only decreases the effective voltage of the current source and was removed in all future designs. If it is ignored, and the assumption that all the current is steered to the left hand side following voltage equation is easily derived:

$$V_{dd} = V_{gs3} + V_{gt1} + V_{gt5} \tag{4.9}$$

Which leads to:

$$V_{dd} - V_t = V_{gt3} + V_{gt1} + V_{gt5} \tag{4.10}$$

The effective voltage of the M_{N3} is α times larger than the effective voltage of M_{N1}, where α is the DC gain of the differential pair. To allow higher current (and higher output frequencies), the effective voltage of M_{N5} is chosen to be equal to that of M_{N1}. An expression for the maximum effective voltage is given in (4.11).

$$V_{g1} = \frac{V_{DD} - V_t}{\alpha + 2} \tag{4.11}$$

Stepping back, equation (4.5) can be simplified. Since the same current flows through M_{N1} and M_{N3}, the g_m of M_{N3} is α types larger, where α is the DC gain of the delay cell. By substituting $g_{m3} = g_{m1}/\alpha$, into equation (4.5), we get:

$$f_o = \frac{g_{m1}}{\alpha 2\pi C_L} \tag{4.12}$$

The load capacitance is dominated by the load of the next delay cell, which is equal to $W_1 L C_{ox}$. By substituting this value for C_L, the third expression for g_m given in equation (4.3), and the value of K given in (4.1), an expression for the maximum oscillation frequency for any technology is given.

$$f_o = \frac{\mu (V_{DD} - V_t)}{2\pi L^2 \left(2\alpha + \alpha^2 \right)} \tag{4.13}$$

In this equation, α must be held constant (α=1.414) to guarantee the VCO has enough gain to oscillate. As the width of the channel decreases, a square

increase in speed is expected. For example, a 1 μm oscillator operating at 700 MHz would operate at 1.094 GHz in a 0.8 μm technology. Speed also increases as the threshold voltage, V_t, decreases.

The actual expression for the frequency of oscillation becomes slightly more complicated once the effect of the PMOS resistor is added. The PMOS acts as a variable resistor connected to the gate of the load NMOS. The effect on the delay cell is exactly the same as looking up the emitter of a bipolar transistor with a resistor connected to the base. The low frequency resistance is given by $1/g_m$ while the high frequency resistance is given by the resistance at the gate. This affects the dynamic gain of the delay cell. By decreasing the gate to source voltage of the PMOS, the effective resistance of the load device is increased, and the delay cell slows down, decreasing the oscillating frequency.

4.3.2 Application of FM Theory to VCO Noise Analysis

The noise sidebands around the VCO are the result of low frequency noise sources that are upconverted to the oscillation frequency. These sidebands are very detrimental to the SNR of the received signal, see Section 2.2.2. To reduce these noise sources, the circuit must be analyzed to determine how to improve the VCO's noise performance.

First, the sensitivity of the oscillation frequency to noise currents at different nodes is determined. This sensitivity is referred to as the modulation coefficient. Next, the level of these noise currents is determined. The product of the modulation

coefficient and the noise currents can be used as a figure of merit with the goal to reduce this value as much a possible.

Unfortunately, this noise model was formed after the design of the FS chip was completed. Much insight has been gained, however, regarding the phase noise of these oscillators. First of all, the major sources of sideband noise have been identified. The largest contributor to phase noise is the bias transistors, with the second major source of being from the PMOS transistor used to simulate a variable resistor at the gate of the load transistor.

Second, the phase noise rises from the noise floor toward the carrier with a slope proportional to $1/f^2$ until about 250 KHz. At this point, the flicker noise in the transistors begins to dominate and the PSD begins to follow a slope equal to $1/f^3$.

4.3.3 Quadrature Quality

To guarantee 40 dB of attenuation of the image channel, the I and Q channels must not differ by more than 1°. To determine the effect of mismatch on the I and Q channels, many Hspice simulations were performed. The simulations were performed by allowing the ring oscillator to oscillate, measuring the frequency of oscillation, and then converting the measured time difference between the two channels to degrees. A perfectly matched ring oscillator was simulated to verify the measurement method. Figure 4-5 shows the circuit topology used in the simulations

along with the node names used.

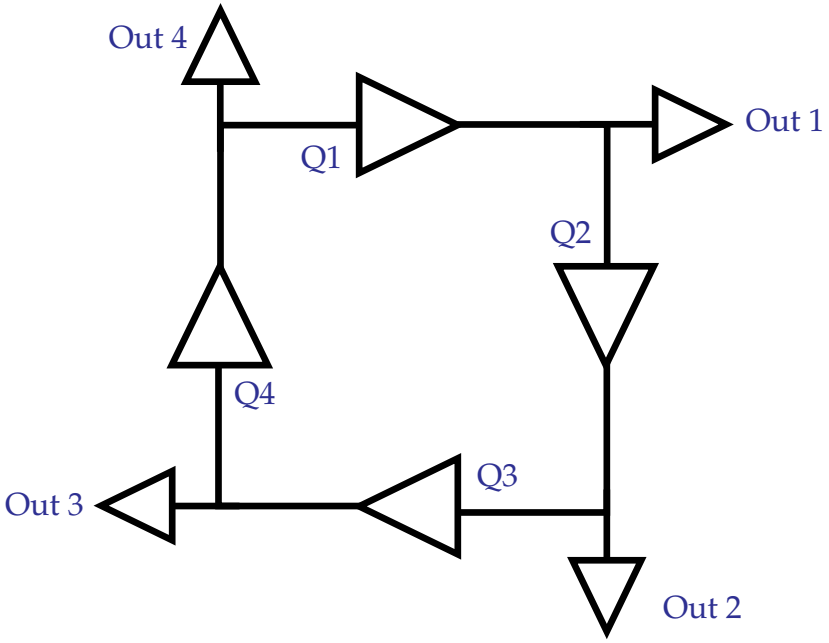


Figure 4-5 Circuit Topology to test Quadrature Quality

The effect of capacitance mismatch can be simulated by adding parasitic capacitances to different nodes. Table 4.1 shows that by adding as little as 10 ff of capacitance to a single node of the ring oscillator, the phase error between the I and Q channels is increased to more than 1°. For this reason the quality of the layout of the VCO is extremely important.

To model the mismatch in the threshold voltage, V_t, DC voltage sources can be added to the input devices of the delay cells. Table 4.1 shows the results of adding a typical offset to one stage of the ring oscillator. The simulations show that the quadrature of the ring oscillator is much more sensitive to typical capacitor mismatch than to typical variations in V_t. This follows intuition since the ring

oscillator uses DC feedback to bias each delay cell at exactly its “trip point”, effectively nulling out the offset voltage of the delay cell.

Table 4.1 Effect of Mismatch in the Ring Oscillator

Description	Frequency of Oscillation	Phase Delay	Phase Error
Nominal	932 MHz	90.0024°	0.0024°
10ff@Q1	917.31	88.7878	-1.212
10ff@Q2	917.33	91.49	1.490
10ff@Q3	917.34	91.218	1.218
10ff@Q4	917.318	88.5180	-1.482
10mV Offset Input of Q3	931.7	89.97	-0.02882
±10mV Offset Input of Q1	931.986	89.9163	-0.08366

Since the oscillator is so sensitive to capacitive mismatch, the ring oscillator is laid out as symmetrically as possible as shown in Figure 4-6. The VCO uses a delay cell with the first buffer already connected. By using this cell, the capacitive loading of the oscillator is guaranteed to match. This delay cell and buffer combination is flipped horizontally and vertically to complete the four stage ring oscillator. By laying out the VCO in this manner, the only source of capacitive mismatch is in the wiring capacitance between each delay cell.

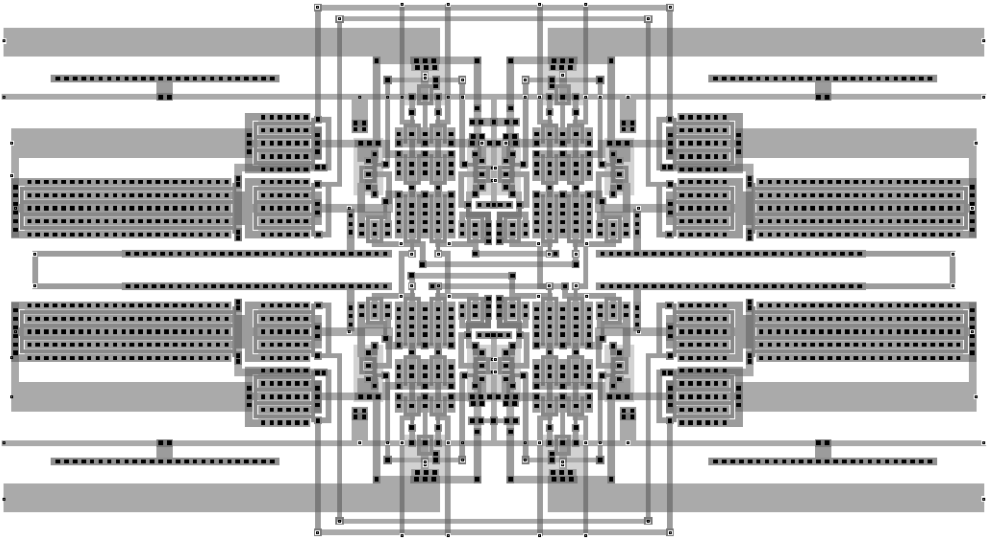


Figure 4-6 VCO Layout

The parasitic capacitances of the VCO were extracted and are given in Table 4.2. The VCO was simulated with these parasitic capacitances and the phase error between I and Q channels was found to be 0.22°.

Table 4.2 VCO Extracted Capacitances

Channel	Node	Capacitance
Q1	36	10.075 ff
	39	10.061 ff
Q2	33	11.39 ff
	34	15.06 ff
Q3	vco_outn	10.06 ff
	vco_outp	10.06 ff
Q4	32	13.069 ff
	35	13.059 ff

Two other process variations that might affect the quality of the quadrature are differences in device mobility and *W/L* mismatch. Both effects will be minimal due to the proximity of the devices and the delay mechanism in the oscillator. Since the delay is dominated by the g_m of the load NMOS, any variation in mobility or *W/L* will be reduced by the square root function in (4.3a). For 1% matching, the channel mismatch should be less than 2°.

The final sources of mismatch between two quadrature channels is the random delay variations that would develope in the buffer chains used to amplify the signals. However, Monte Carlo simulations have shown this skew to be small.

4.4 High Speed Prescalers

A D-latch type prescaler is used due to its high operating frequency. Further, the D-latch is implemented using a SCL configuration. This latch is found to be the fastest and the most power-efficient of all the latches simulated. Since it is biased by a constant current source, it does not inject noise into the power supply lines or onto the ground lines. Further, this circuit does not require the large amplitude input signals required by the TSP latch. The schematic of the latch is given in Figure 4-7.

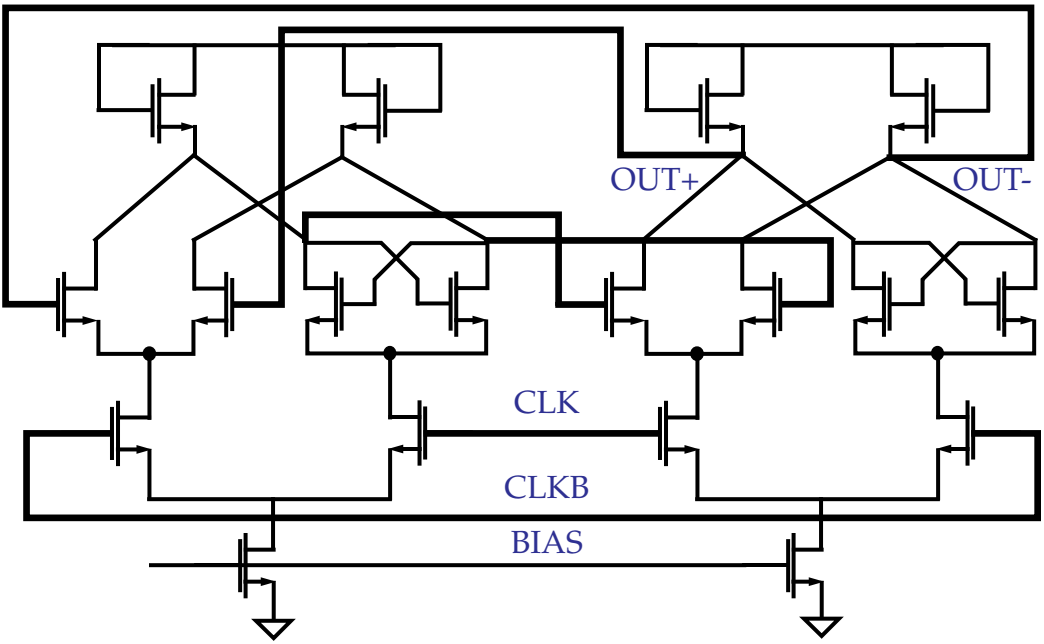


Figure 4-7 SCL D-Latch

The circuit topology of the SCL D-latch is very similar to the delay cell of the VCO. In fact, if the input signal is very small, the D-latch will oscillate on its own! Because of the similarity between the VCO delay cell and the SCL D-latch, much of this insight can be applied to the design of the prescaler.

The D-latch consists of two sections that are alternately selected with the input clock. When the clock signal is high, the first section acts as a comparator and senses the output of the latch. At the same time, the second section acts as a regenerative latch, holding the last value of the latch. When the clock goes low, the roles of the two sections are reversed.

This circuit can be optimized by making the sizes of the transistors in the first section smaller than the transistors in the second. This reduction is possible

because the first section only drives the second section, while the second section drives the first section and the large input transistors of the following latch.

4.5 Phase Detectors

The reference frequency was chosen to minimize the divide ratio of the prescaler. A large divide ratio is attenuates the loop gain of the PLL and reduces the amount of VCO noise attenuation. However, the ration cannot be made very small because then the reference frequency increases and the power dissipation. The power dissipation for a crystal oscillator increase rapidly at overtones above the fundamental mode of oscillation. In addition, the digital phase/frequency detector does not provide very much frequency information at higher frequencies.

A digital phase/frequency detector was chosen because of the ease of implementation and the built-in frequency detection feature for low frequencies. If the PD did not provide frequency difference information, a separate circuit would have to be added to aid the loop in acquiring lock.

The standard digital phase/frequency detector developed by Motorola was used. The circuit was implemented using SCL type gates to reduce noise injection into the substrate and onto the power supply lines. These gates have the advantage of drawing a constant current from the supply lines as opposed to the current spikes that are generated at logic transitions in CMOS cells. Further, this type of gate interfaces easily to the prescaler and to the charge pump. The reference frequency will come from a differential crystal oscillator circuit to reject common-mode noise,

thus interfacing easily with the PD as well. The block diagram is given below.

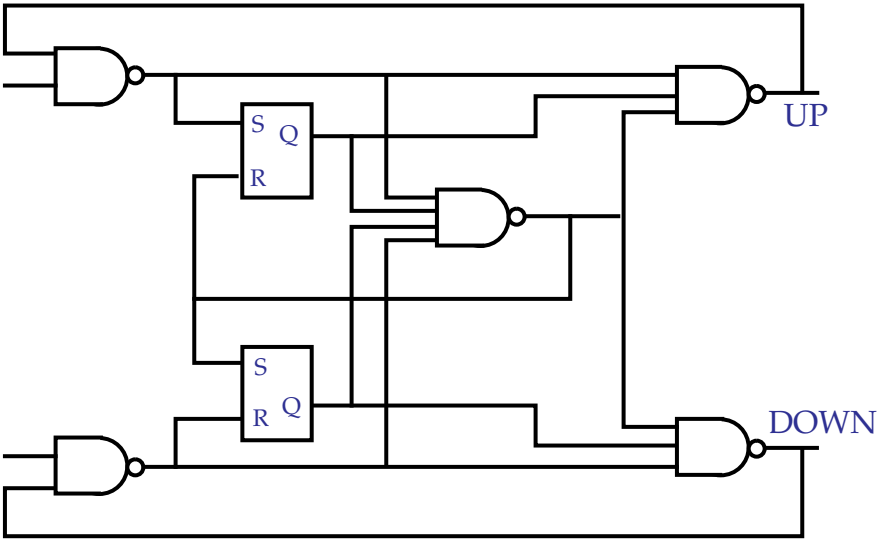


Figure 4-8 Digital Phase/Frequency Detector Block Diagram

A single SCL NAND gate cell was designed and used to implement the RS Latch, the 3-Input NAND, and the 4-Input NAND. The SCL NAND gate is shown in Figure 4-9. The output swing is independent of supply voltage and is equal to V_{gt} of M_{N3}. The RS Latch was formed by cross coupling a pair of NAND gates in the standard configuration. The 3-Input NAND was formed by cascading two NAND gates. The 4-Input NAND was formed by taking the NAND of pairs of signals and then taking the NAND of that pair.

The dead zone of the PD was analyzed using the method described in Section 3.3.3. The rise-time of the internal circuitry was found to be much smaller than the width of the reset pulse minimizing the dead-zone effect.

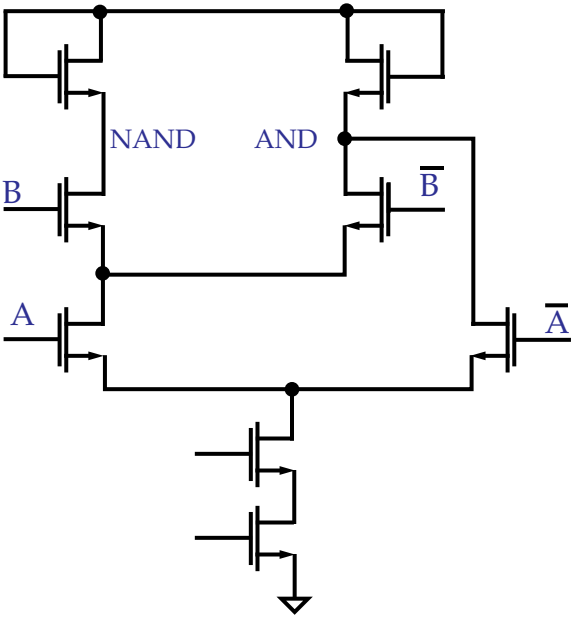


Figure 4-9 SCL NAND Schematic

Care was taken in the layout to guarantee that the upper and lower halves of the PD matched each other. The layout for the PD is shown below. The signals from the PD contain a reset pulse with energy at the reference frequency. This energy will show up as spurious tones around the carrier at the reference frequency. By maintaining symmetry throughout the control circuits, the reset pulse coming from the PD can be exactly cancelled.

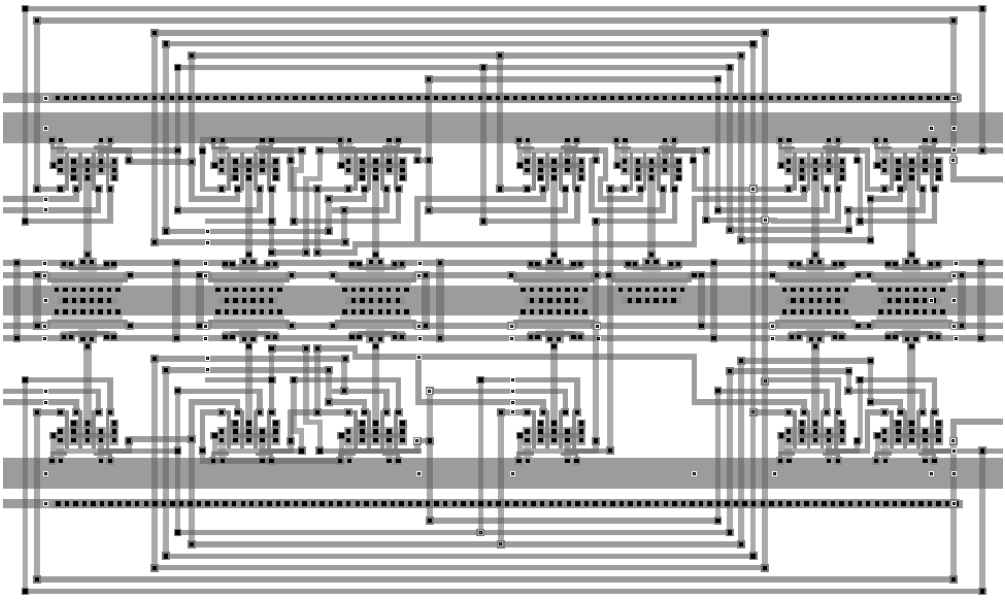


Figure 4-10 Layout of PD

4.6 Charge Pump and Loop Filter

By including an integrator in the PLL, the phase error between the VCO output and the reference is forced to be zero. In addition, the low frequency noise of the VCO is suppressed to a higher degree than a passive loop. A charge pump loop filter has been chosen because of its ability to implement an integration without an op amp. A block diagram of the charge pump and the loop filter is shown in Figure 4-11. The load Z_L, consists of a capacitor in series with a resistor. The capacitor implements an integrator while the resistor provides a compensation zero for PLL. The differential to single-ended converter provides some gain and level-shifts the control signal.

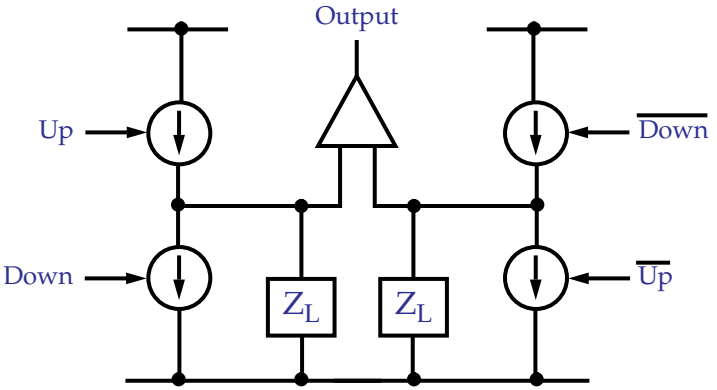


Figure 4-11 Charge Pump and Loop Filter Block Diagram

The charge pump is designed so that similar signals drive input devices that are at the same voltage level. By ensuring that all the input transistors are at the same voltage level, almost all of the energy at the reference frequency is cancelled. The charge pump circuit is shown in Figure 4-12.

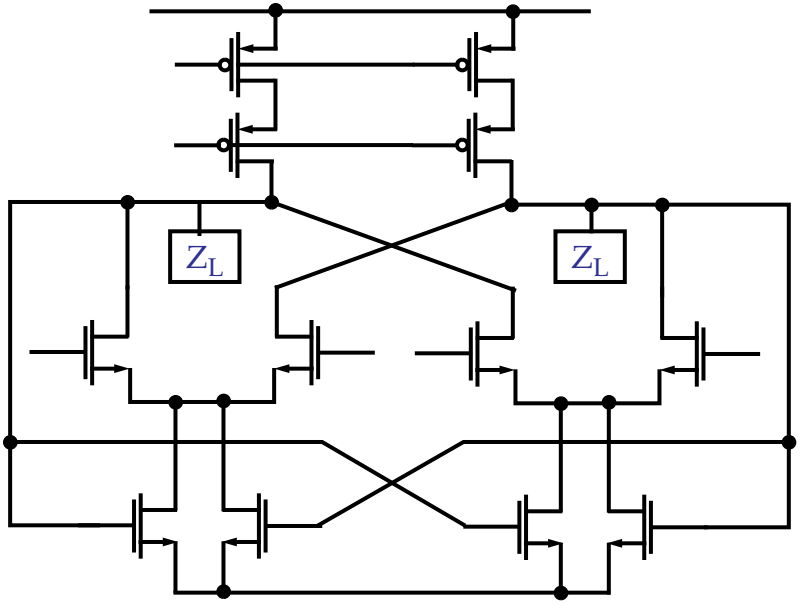


Figure 4-12 Charge Pump Schematic

4.6.1 System Simulation of PLL Performance

The entire PLL was simulated using Hspice as well as Matlab. Matlab provides a system simulation environment, called Simulink, that allows linear blocks of the PLL to be simulated very quickly. A full simulation performed in Hspice would take about a full day. In Simulink, the simulation only takes a few minutes. Further, additional system elements such as a DDS and mixers can be easily added to simulate the entire transceiver.

The Simulink block diagram is given in Figure 4-13. The function of each block is readily apparent except for the VCO and frequency divider. Because the phase of a signal is the integral of the frequency, the VCO is modeled as a gain stage, an integrating function, and a sine function. The frequency divider is modeled as a gain block that scales the phase of the output signal by 1/N. The PD is modeled exactly like an ideal PD by using ideal switches to implement AND blocks and resetable flip-flops.

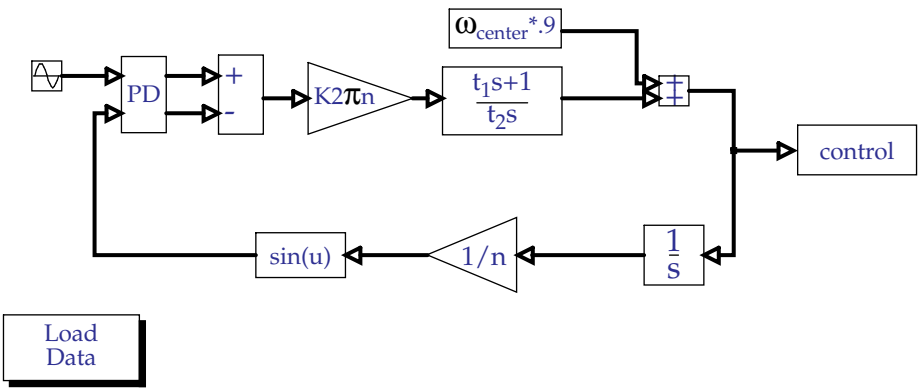


Figure 4-13 Simulink Block Diagram

By double clicking the “Load Data” button, new filter coefficients can be

simulated. The plot in Figure 4-13 shows the typical system simulation. The PLL bandwidth was set to 500 kHz and the damping coefficient was set to 1.2. During the locking period, the control signal resembles an exponential curve even though the system contains some discrete time elements. As the VCO frequency gets close to the reference frequency, the PLL sends out pulses to nudge the phase of the VCO. Finally, when the VCO is locked, the control signal is flat.

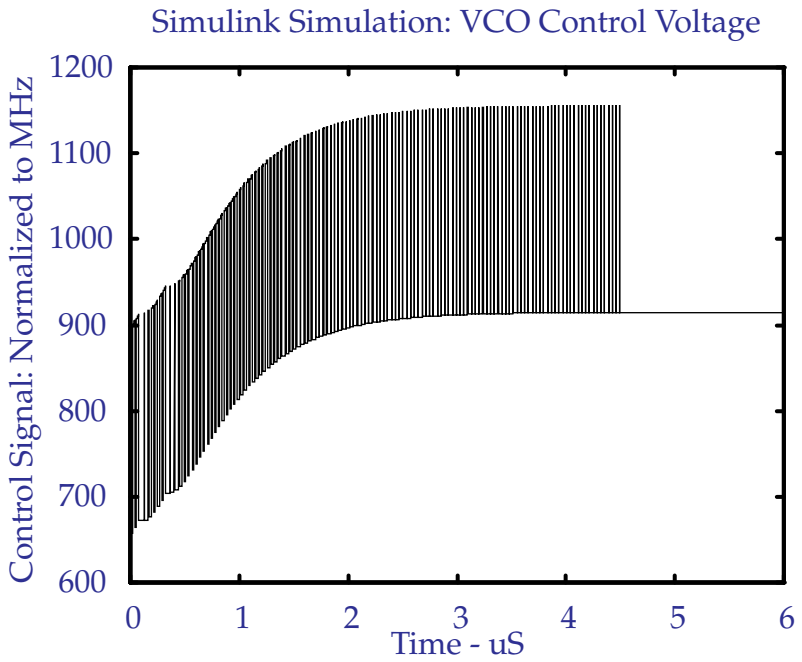


Figure 4-14 Simulink System Simulation

4.7 Amplifier and Level-Shift Circuits

All the active circuits in the charge pump must be carefully designed not to add any additional noise to the loop. A differential to single ended amplifier and a level shifting circuit directly follow the charge pump in Figure 4-1. These circuits

are shown in Figure 4-15. This circuit is used as a level shift to ensure the control voltage of the VCO is biased in the middle of the tuning range.

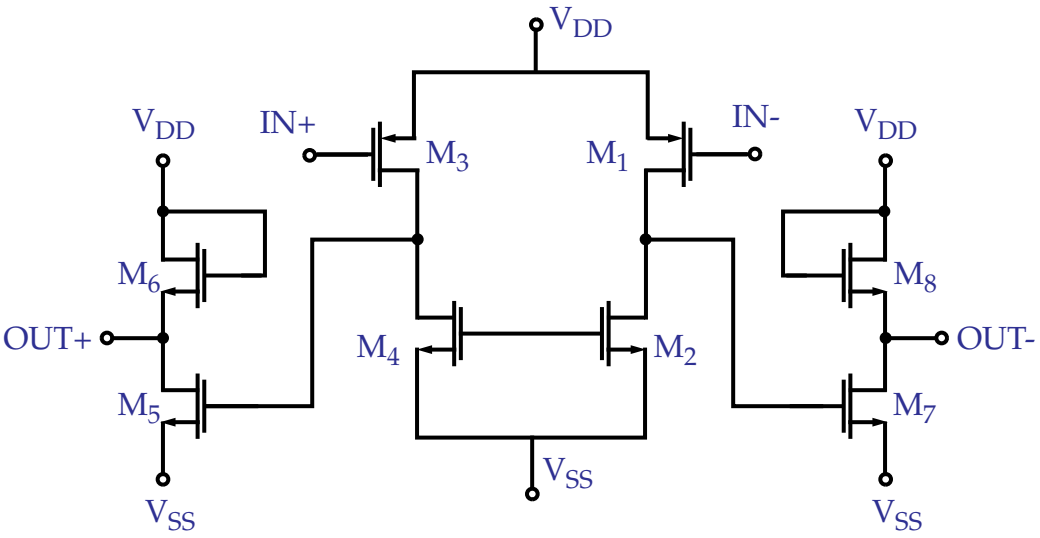


Figure 4-15 CMOS Differential Amplifier

Chapter 5

Testing

5.1 Test Set Up

A high frequency test set-up was built to test the chip. The test set-up was designed to allow different external loop filters, phase detectors, and divide ratios to be tested. Additionally, if other circuits such as a Low Noise Amplifier (LNA) or mixers were added to the frequency synthesizer chip, they could be tested without having to build a new test set-up. The set-up is shown in Figure 5-1.The set-up consists of four individual circuit boards that are mounted to a 1/4” aluminum plate. The plate allows the set-up to be more portable and prevents the circuit boards from moving around. By limiting the mobility of the circuit boards, any fatigue in the solder joints can be prevented.

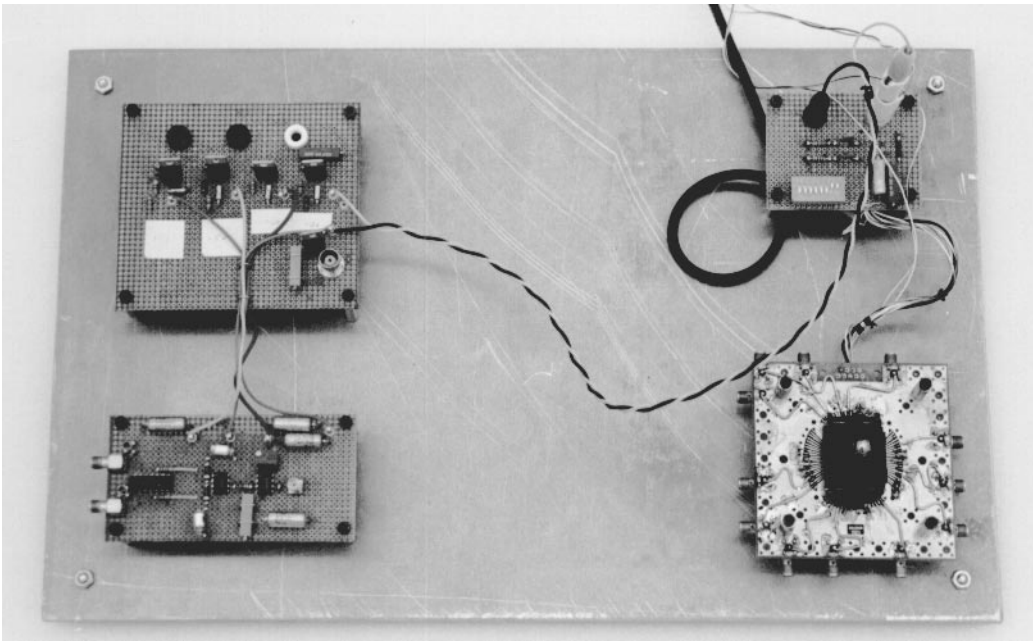


Figure 5-1 High Frequency Test Board

The first circuit board provides all the supply voltages for testing. By generating all the required supply voltages, fewer external supplies or adjustments are required, and additional filtering can be applied to the supply lines. The circuit diagram for the bias section is given in the Appendix.

The second board contains a commercial Phase Detector and a loop filter. Level shifting and gain is also provided by an additional op-amp. The PD used is the Motorola 12040, an ECL version of the Motorola 4044.

The third board is a high frequency test board with a 40 pin leadless chip carrier test socket. All bias and supply lines are decoupled at the socket pin with a 0.1 μF chip capacitor. All high frequency supply lines were connected to SMA connectors with 50 Ω semi-rigid coax-cable.

The last circuit board provides control signals to the FS chip via switches to choose between different operating modes. The external loop filter is also located on this board.

The external instruments that were used include a high speed divide by 16 board, a HP 8643A high speed frequency synthesizer, a HP 3585A low speed frequency synthesizer, a HP 8643A high speed spectrum analyzer, a HP 3335A low speed spectrum analyzer, and various oscilloscopes.

5.2 VCO Characterization

First the VCO was tested. The bias current was fixed and the supply was varied for different control voltages. A plot of the VCO's gain curve is shown in Figure 5-2. The gain curve shows how sensitive the VCO is to supply variations.

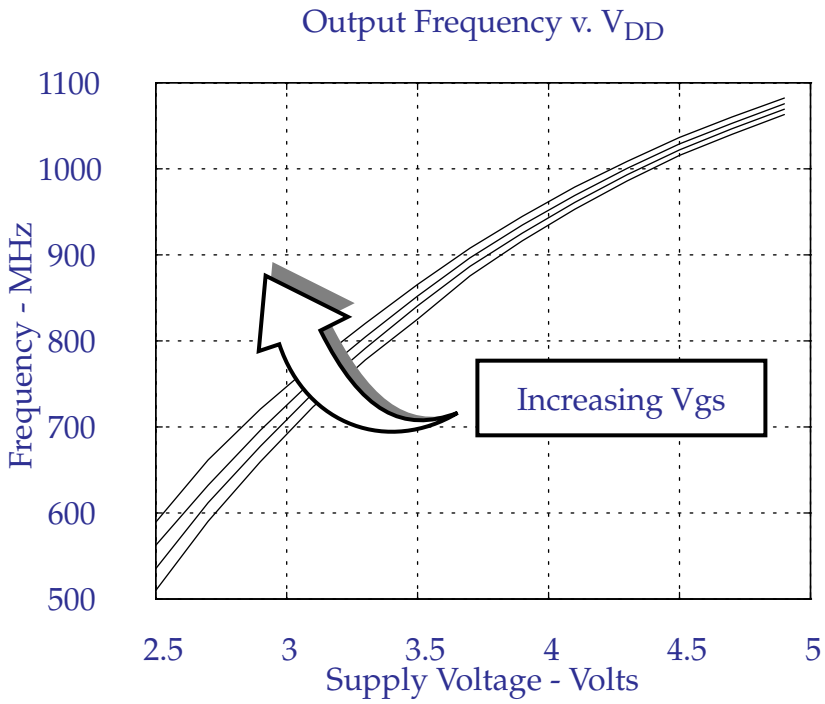


Figure 5-2 VCO Gain Curve

The plot shows that the VCO does not operate at 915 MHz until the supply voltage is increased to 3.7 volts. Increasing the bias current will also increase the operating frequency. This is shown in Figure 5-3. However, the bias current cannot be increased without limit. As the current is increased, the sources of the differential pair drop in voltage until the bias transistor is forced into triode. Once in triode, the common-mode gain of the differential pair increases and even results in a low frequency, common-mode oscillation. The effective voltage, V_{gt}, of the bias transistor could be decreased, but this would result in very bad noise performance.

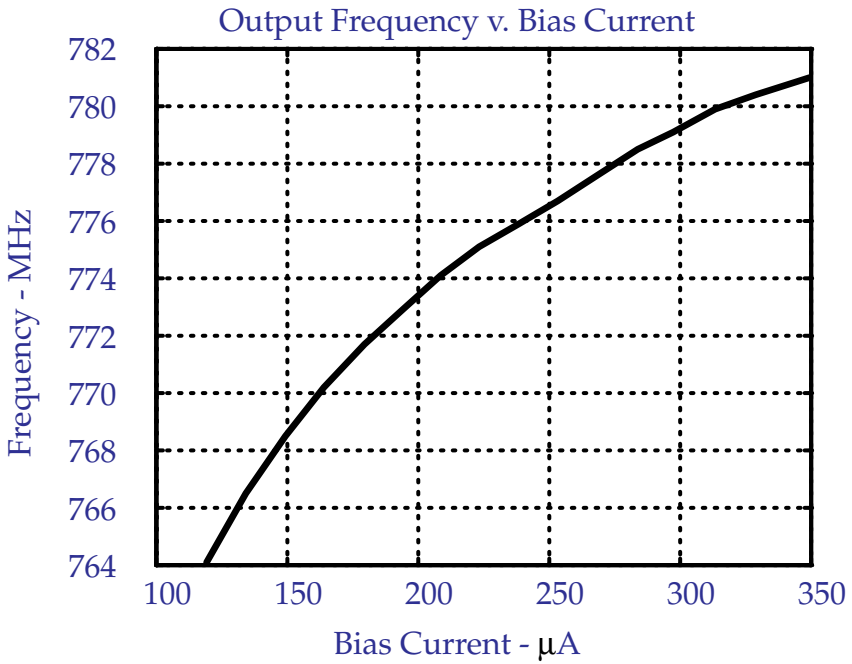
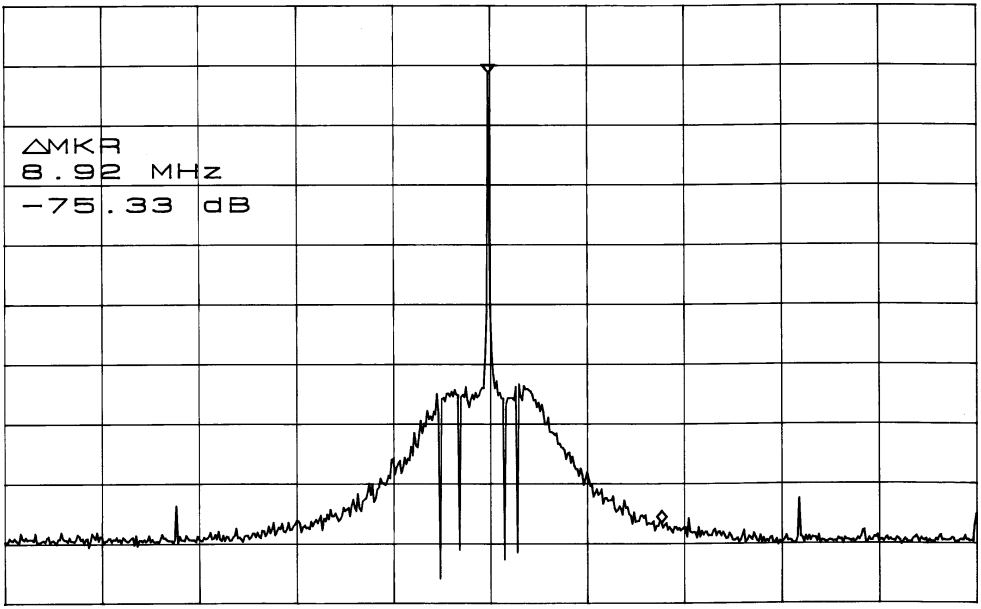


Figure 5-3 Output Frequency v. Bias Current

5.3 Closed Loop Spectrum

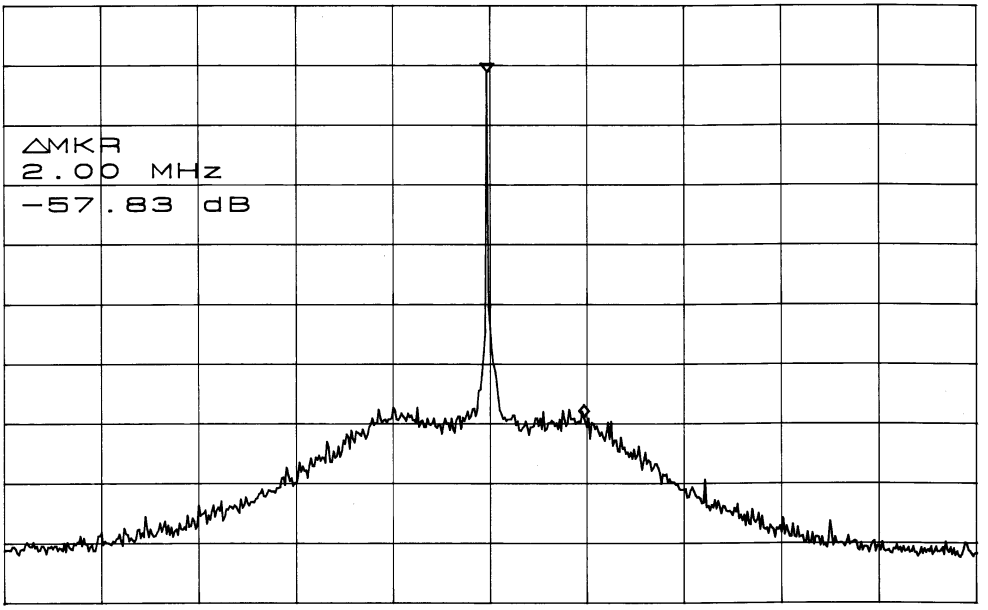
By using the measured data, the coefficients of the external loop can be chosen so the loop is stable. A typical wide-band spectrum is shown in Figure 5-4.



RBW 3.0 kHz	Span50.00 MHz
VBW3.0 kHz	Sweep20 sec.

Figure 5-4 Output Signal PSD - 50 MHz Span

From this PSD, the noise floor is clearly visible. The side-band noise begins to rise above the noise floor and has a 3 dB corner at about 8.92 MHz. This corner corresponds to f_d in Figure 2-10. This corner corresponds to an effective Q of the oscillator. It is expected that as the VCO becomes less sensitive to noise variations, this corner frequency will decrease.

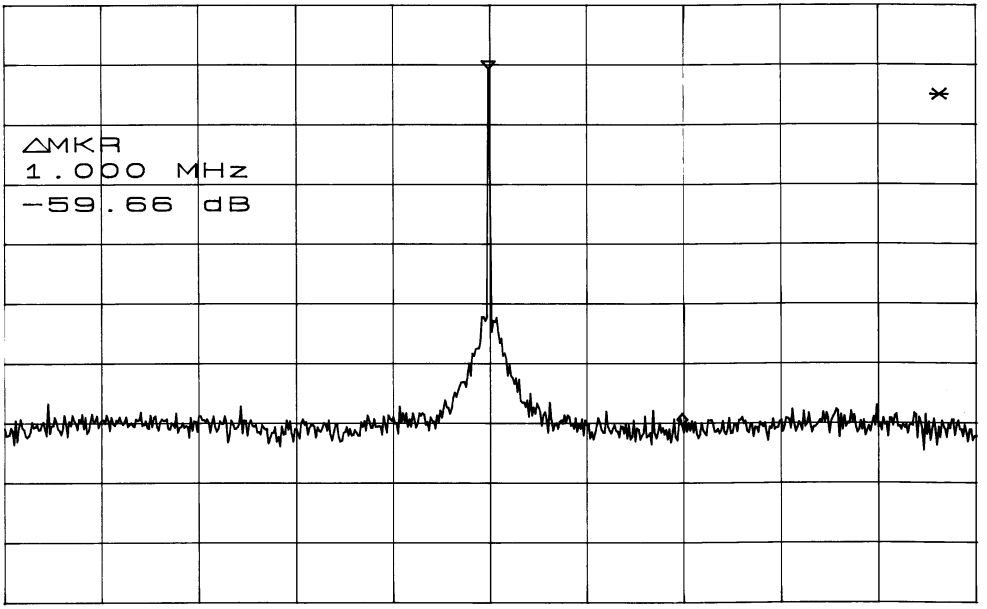


RBW	1.0 kHz	Span	20.00 MHz
VBW	1.0 kHz	Sweep	50 sec.

Figure 5-5 Output Signal PSD - 20 MHz

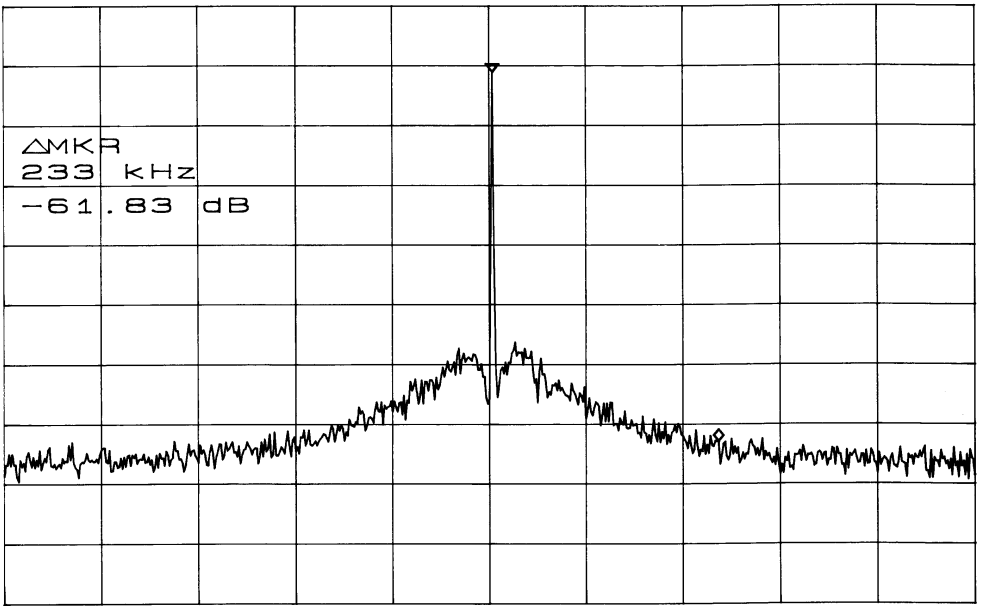
The PSD in Figure 5-5 shows that the noise continues to rise until it reaches the bandwidth of the loop. This point, corresponds to f_c in Figure 2-10 and is at about 2 MHz. The flat region predicted by Figure 2-11 is clearly visible.

As the span of the spectrum analyses is narrowed even further, the 1/f corner corresponding to f_b appears. Figure 5-6 and Figure 5-7 contain the flat region expected between f_b and f_c. The noise level begins to rise once again and indicates that the sideband noise is rising faster than the 20 dB/decade of attenuation provided by the PLL. The 1/f corner is at about 233 kHz.



RBW	1.0 kHz	Span	5.00 MHz
VBW	1.0 kHz	Sweep	20 sec.

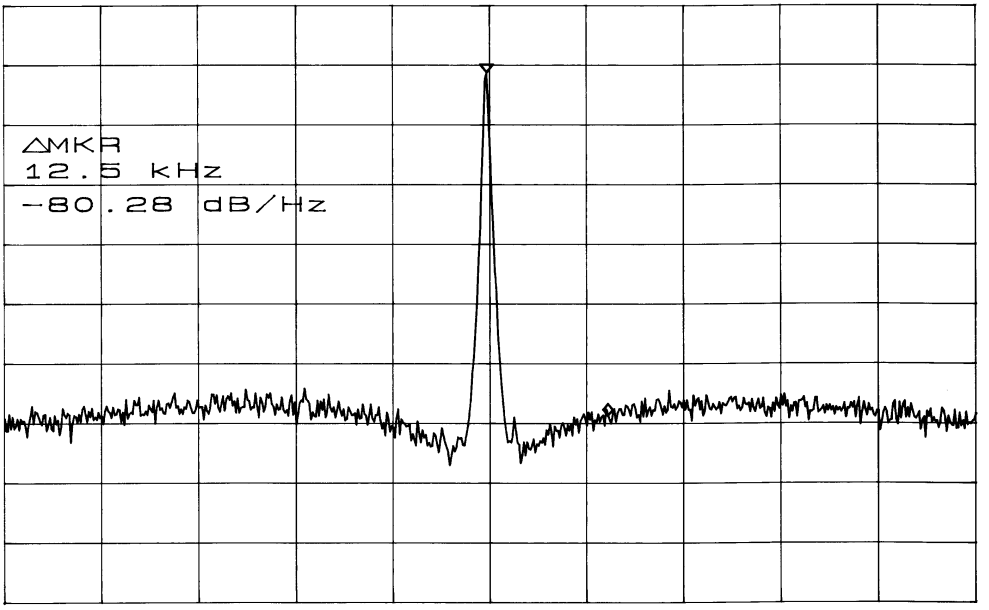
Figure 5-6 Output Signal PSD - 5 MHz



RBW	300 Hz	Span	1.00 MHz
VBW	300 Hz	Sweep	30 sec.

Figure 5-7 Output Signal PSD - 1 MHz

Finally, as the bandwidth of the spectrum analyzer is narrowed to 100 kHz, the stabilizing zero in the PLL is passed and the noise attenuation is 40 dB/decade. The dip predicted by Figure 2-11 begins at about 12.5 kHz, which corresponds exactly to the time constant of the resistor and capacitor implementing the zero in the PLL.



RBW	300 Hz	Span	100.00 kHz
VBW	10 Hz	Sweep	90 sec.

Figure 5-8 Output Signal PSD - 100 kHz

5.4 Phase Noise

The noise performance of a frequency synthesizer is commonly given as a plot of RMS power versus the offset frequency from the carrier. This plot is generated by taking the single-sideband power of the phase noise and normalized it to a 1 Hz bandwidth and converting it to dBc and is defined as £(fm) [26].

The test setup was modified to allow the phase noise of the FS to be measured. This setup is shown in Figure 5-9. An amplifier follows the FS chip to amplitude-limit the VCO signal, eliminating any AM modulation of the signal.

When the two inputs to the mixer are in quadrature, the mixing products are

equal to sine functions of the sum and the difference of the input signals. For low levels of phase noise, the function sin(x) can be approximated as x. For this approximation, the mixer acts as a phase detector, converting the phase noise of the FS to a voltage.

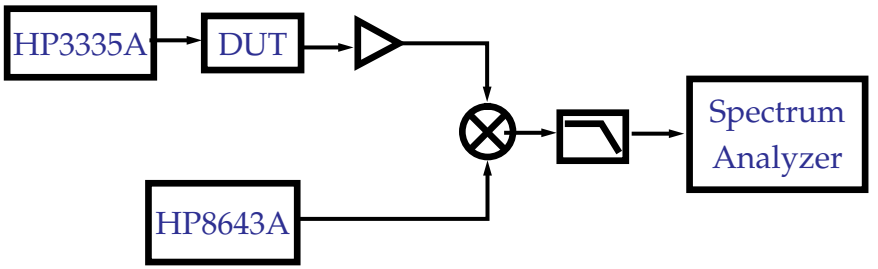


Figure 5-9 Heterodyne Setup to Measure Phase Noise

Quadrature is easily maintained by using the reference clock of the HP 8643A as the reference to the HP 3335A. The phase of the HP 8643A can be adjusted until the DC voltage at the output of the mixer is zero, indicating perfect quadrature.

5.5 Quadrature Quality

The quality of the quadrature between the I and Q channels is very difficult to measure on an actual chip due to the skew that arises from parasitic elements and there are no instruments with the necessary resolution. The only clean way to measure the quadrature quality is build a Single Side-Band (SSB) modulator and measure the rejection of the image tone. A SSB chip is currently in fabrication.

Chapter 6

Conclusions

6.1 Low Noise Design

A number of improvements can be made to the frequency synthesizer chip to reduce the sideband noise. During noise analysis, it was found that the PMOS in the delay cell contributed the second most amount of noise to the VCO. By removing this device and controlling the frequency with the bias current, the noise sidebands should decrease by a few dB.

Since the major source of noise is the bias transistor, it should be made as low-noise as possible. For a given current, the noise current is inversely proportional to V_{gt}. By removing the cascode in the current source, the V_{gt} of the bias transistor can be increased. Only a small increase, if any, in common-mode power supply sensitivity is expected since the differential pair was pushing the

cascode current source into triode, reducing its effective resistance. Finally, the total area of the bias transistor should be increased as well since 1/f noise is inversely proportional to the device area.

Finally, any noise currents in parallel with the control node of the VCO directly modulate the output signal and must be reduced. The charge pump and the differential to single-ended converter circuits should be scaled to minimize any noise contributions that they might add. The analog multiplexors have a non-zero on resistance and add noise directly to the control voltage of the VCO. In the final design, these multiplexors should be removed.

The prescaler should also be redesigned to be a synchronous divider instead of a ripple counter. This would cut down on phase instabilities in the divider, but would require the final divider section to operate at 915 MHz along with the first cell. It has been show [22] that ECL dividers are the most noisy of all dividers so care must be taken in this design.

6.2 Higher Operating Frequency

In the present design, the VCO could only operate at 915 MHz when the supply voltage was increased past 3.7 volts. Future designs should be able to operate from a 3 volt power supply. The easiest solution would be to move to a faster technology such as 0.8 μm CMOS process. If such a move was made, not only would it be possible to operate from a 3 volt power supply, but lower noise

would also be achieved. A simple argument shows this. If, for example, the same bias current is used for the 0.8 μm oscillator as the 1.0 μm oscillator, the 0.8 μm oscillator would operate 40% faster than the 1.0 μm oscillator. The 0.8 μm oscillator could be “slowed down” by increasing the size of the output swing, reducing the noise as explained in section 2.2.3.2.

6.3 Future Work

Future work includes expanding the noise analysis begun during this project to accurately predict the sideband noise of any type of regenerative oscillator. It is also hoped that enough insight is gained from this analysis to develop new regenerative oscillator structures that not only have a wide frequency range but low noise performance as well. This knowledge can be applied to the design of high speed, low jitter prescalers as well.

A low noise VCO could be realized with the on-chip inductors developed in our group by James Chang. An on-chip inductor could provide the high purity signals required for the increasingly strenuous demands of contemporary wireless communication applications.

Appendix A

Additional Schematics

A.1 Test Board Schematics

The circuits in Figure A-1 were used to provide all the supply voltages for the chip and the external PLL. Two variable supplies were used to vary the supply voltage of the chip and the control voltage of the VCO.

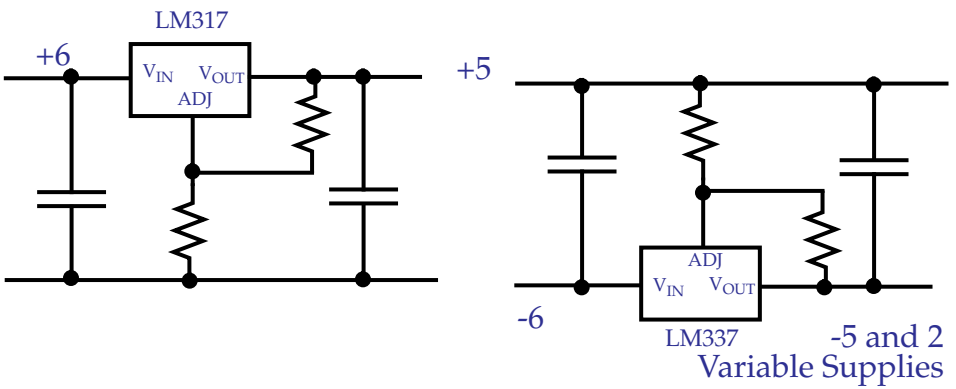


Figure A-1 Bias Board

The external loop filter was used to test different loop bandwidths. A commercial PD and an op amp were used to implement the loop filter. The second op amp was used to level shift the control signal and provide gain adjustment to the loop.

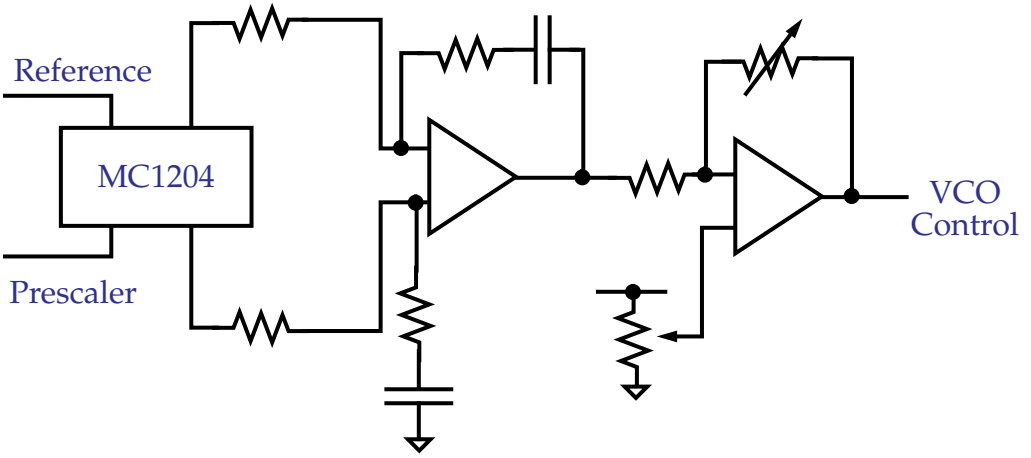


Figure A-2 External PLL

The final schematic shows some simple current bias resistors, and external loop filter, and the switches used to select between the external and internal loop filter and control voltage.

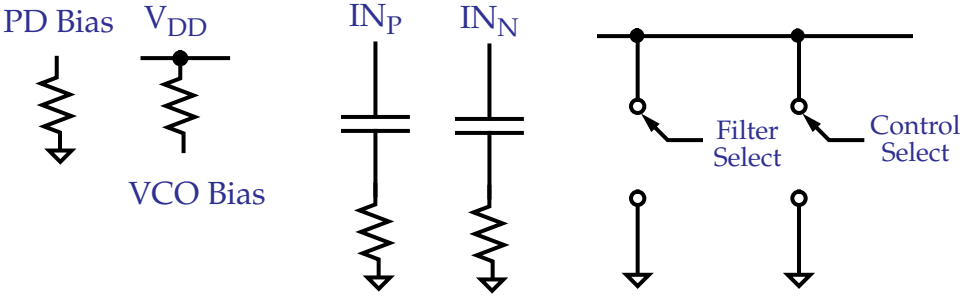


Figure A-3 External Loop Filter, Current Bias, and Mux. Switches

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