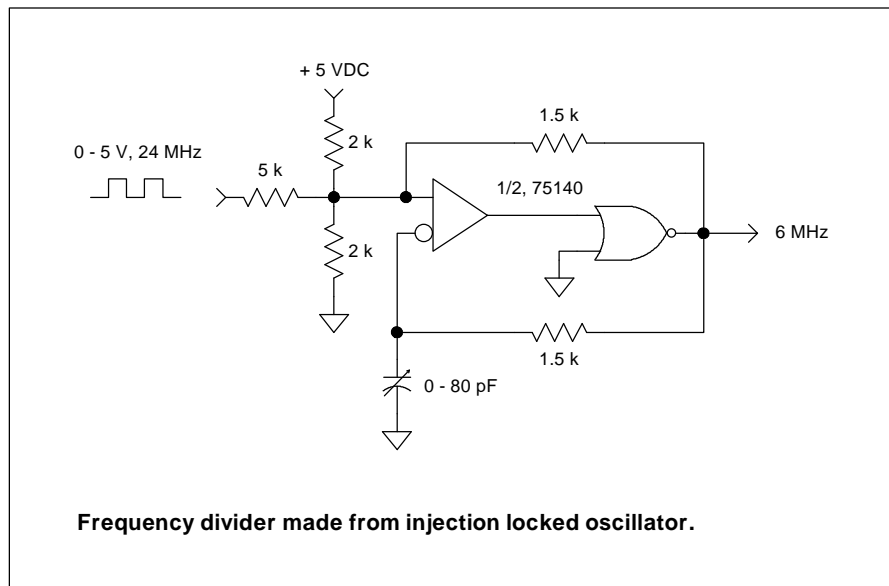# Unusual Frequency Dividers

Charles Wenzel

This paper is a collection of unusual frequency divider techniques which offer features not achieved with ordinary divider ICs or prescalers.
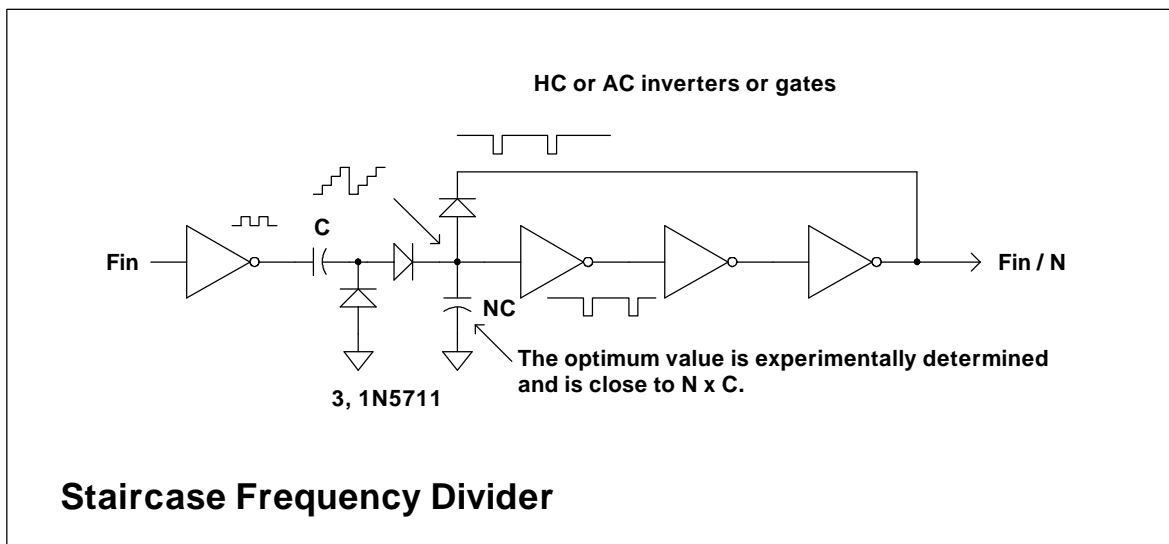
Injection Locked Frequency Divider

The following circuit uses a 75140 line receiver to form an injection locked oscillator. The circuit is similar to the common op-amp square-wave oscillator with values selected to keep the voltages within the recommended operating ranges. The frequency to be divided is coupled through a 5k resistor to the positive feedback input of the comparator superimposing a 0.5 volt squarewave. The small squarewave toggles the comparator when the sawtooth voltage on the capacitor comes close to the DC level on the positive feedback input. The result is that the comparator output frequency is an integer sub-multiple of the input frequency. Since the comparators exhibit good temperature stability and precision, the division ratio can be quite high. A division factor over 20 is practical and since the 75140 is a dual line receiver, two dividers may be cascaded for division ratios over 400. For ratios higher than 4, increase the 5k series resistor to 10k.

Frequency divider made from injection locked oscillator.

This type of divider usually exhibits poor phase noise performance but with proper modifications good phase noise performance may be achieved. The fundamental technique is to use the output of the oscillator to gate the input pulses such that the input pulse controls the output edges. For example, the output of the circuit shown could drive the input of a D-type flip-flop with the input frequency driving the flip-flop's clock input. Jitter on the D input has no effect on the output jitter.
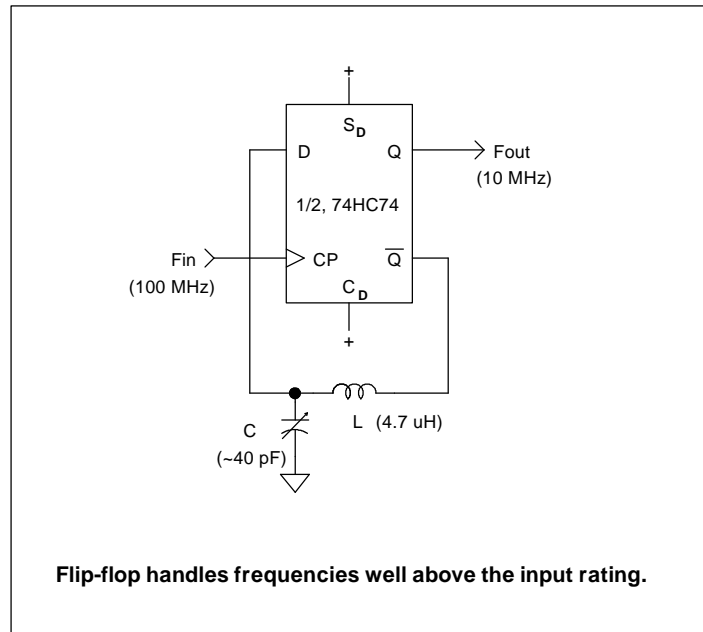
Staircase Frequency Divider

A pulse counter may be implemented by dumping the charge from a small capacitor into a larger capacitor at the input frequency. The voltage on the larger capacitor will increase in a staircase fashion. A comparator or other threshold device senses the voltage exceeding a certain level and a reset pulse discharges the capacitor. The following schematic shows one implementation using a CMOS inverter IC and three Schottky diodes. Each positive edge from the input inverter dumps charge from the small series capacitor, C, into the larger capacitor, NC, until the voltage reaches the gate threshold. When the threshold is passed, the following three gates change state and the capacitor is discharged through the feedback diode. The use of three gates produces a slight delay to give a reliable reset pulse. The ratio of the capacitor values determines the division factor but the optimum values will not necessarily be integer values. The input capacitor should be fairly small, perhaps 10 to 33 pf and the charge accumulating capacitor should be selected to give the desired division factor. A trimmer may be substituted for either capacitor to find the optimum operating point.

HC or AC inverters or gates

Fin

C

NC

The optimum value is experimentally determined and is close to N x C.

3, 1N5711

Fin / N

Staircase Frequency Divider
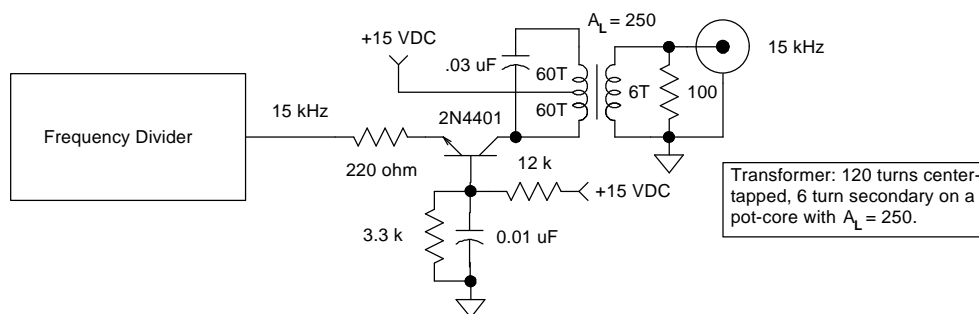
Getting More Speed from a Logic Family

Here is a simple trick for dividing a frequency well above the toggle frequency of a particular logic family. The clock inputs of a logic family respond to frequencies well above the frequency that the devices can successfully divide. The output becomes a chaotic jumble of unpredictable sub-harmonics below the expected frequency due to the internal circuitry's inability to keep up with the fast clock. By adding a delay line to the common D flip-flop divide-by-two circuit, the internal frequency of the device can be lowered to an acceptable range. After one of the high frequency pulses triggers the flip-flop all following input pulses are ignored until the effect of the trigger propagates through the flip-flop and the delay line back to the D input (see the schematic below). The flip-flop will trigger predictably if this delay is longer than the amount of time required for the flip-flop's internal circuitry to settle and the edge is not close to an input edge. Obviously, the circuit must divide by more than two but a flip-flop capable of only dividing 50 MHz (by two) may be able to divide frequencies well above 100 MHz (by four or more). The circuit is frequency specific due to the fixed delay but the technique can allow low power, slow devices to prescale surprisingly high fixed frequencies.

Flip-flop handles frequencies well above the input rating.

The schematic shows the values to convert a 74HC74 into a divide-by-ten 100 MHz prescaler handling frequencies about three times higher than the specified maximum input frequency (30 MHz). The current consumption is only about 10 mA. The circuit may be adjusted to work with frequencies approaching 150 MHz but the performance becomes unreliable and temperature sensitive. An experimental circuit was constructed with a 74F74 which has a toggle frequency near 100 MHz. Using a 0.47 uH inductor for L and a 20 pF trimmer, the circuit was able to divide 400 MHz by 8 to give a 50 MHz output. (The circuit was not particularly stable. A prescaler is probably best for handling frequencies above 300 MHz.) The circuit should work well with slower devices including 4000 series CMOS and the older 74L74s. Since the device is toggling at the output frequency, the power consumption will be lower than an ordinary divider from the same family.
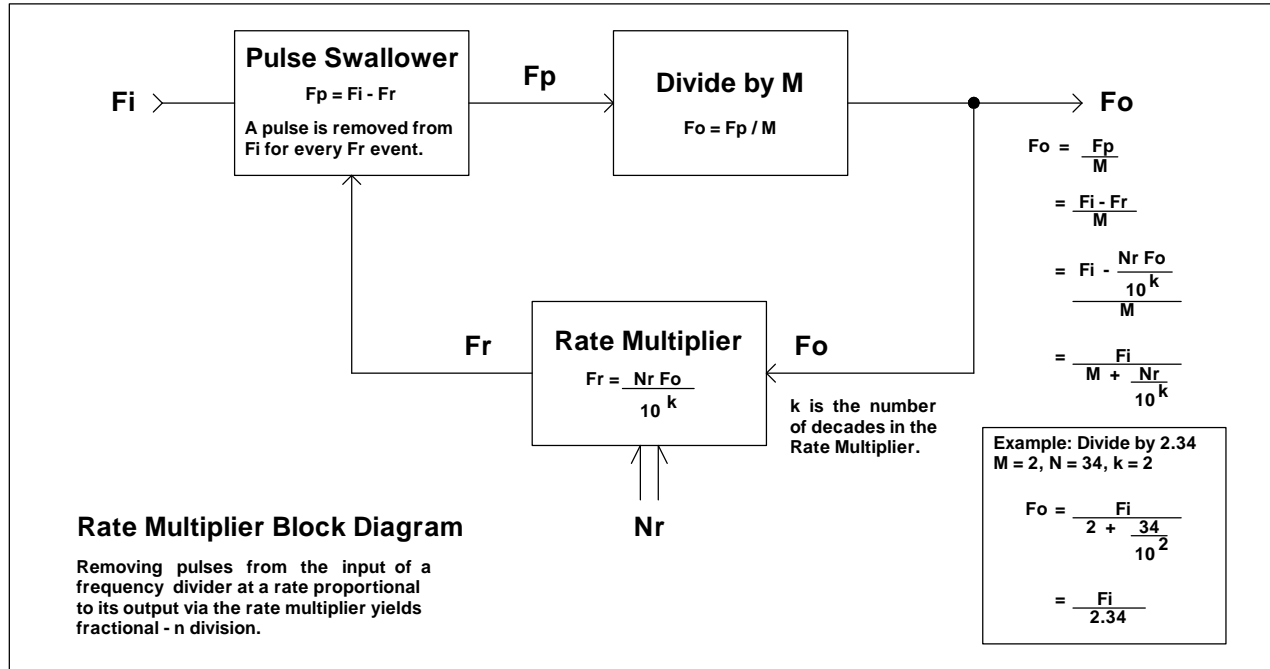
Sinewave Converter for Logic Devices

A grounded-base stage may be used to convert the output of a logic device to a sinewave. A typical implementation is shown in the following schematic. The resonant tank shown is for an unusually low frequency but higher frequency outputs are easily achieved by appropriate choice of resonant transformer.

Fractional-n Divider

Rate multipliers provide a programmed number of pulses per decade of clock pulses. For example, the CD4527 is a 4-bit BCD rate multiplier which will provide 3 pulses for every 10 clock pulses when the input is programmed with 3. The pulses are spread out as much as practical over the allotted time to reduce jitter. The rate multiplier may be combined with an ordinary divider and "pulse swallower" to form a fractional-n divider as shown in the following block diagram.

Pulse Swallower

$F_p = F_i - F_r$

A pulse is removed from Fi for every Fr event.

Fi $\rightarrow$

Fp $\rightarrow$

Divide by M

$F_o = F_p / M$

$\rightarrow$ **Fo**

$$F_o = \frac{F_p}{M}$$

$$= \frac{F_i - F_r}{M}$$

$$= \frac{F_i - \dfrac{N_r F_o}{10^k}}{M}$$

$$= \frac{F_i}{M + \dfrac{N_r}{10^k}}$$

Fr

Rate Multiplier

$$F_r = \frac{N_r F_o}{10^k}$$

Fo

k is the number of decades in the Rate Multiplier.

Nr

Rate Multiplier Block Diagram

Removing pulses from the input of a frequency divider at a rate proportional to its output via the rate multiplier yields fractional - n division.

Example: Divide by 2.34
M = 2, N = 34, k = 2

$$F_o = \frac{F_i}{2 + \dfrac{34}{10^2}}$$

$$= \frac{F_i}{2.34}$$

The circuit implementation shown below will divide by 1.000 to 9.999. The frequency input is connected to the pins labled "Fin" and an inverted version of the input is applied to "/Fin". "MR" and "/MR" are the master reset inputs.

Fin

Fin

Fout

CLK

4510

/CAR OUT

7

5

/CI

CLK

4510

/CAR OUT

7

SET

D Q

4013

DWN

DWN

/Fin

Q̄

P4 P1 PE /CI R

3 13 12 4 1 5 10 9

P4 P1 PE

3 13 12 4

R

10 9

CLR

BCD 1.0

BCD 10

4023

/MR

MR

MR

8

9

+

SET

D Q

4013

13

Fin

11

CLR

10

9

6

12

9

6

12

9

CLK

OUT

CAS

CLK

OUT

CAS

CLK

4527

INH O

7

11

INH

4527

INH O

7

11

INH

4527

OUT

6

INH CLR

10

ST

10

ST

S

CAS ST S

3 2 15 14

12 11 10 13 4

ST CLR

13 4

3 2 15 14

CLR

13 4

3 2 15 14

S

BCD 0.1

BCD 0.01

BCD 0.001