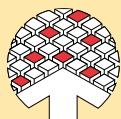




product features

- All digital implementation — less than 0.25 dB of implementation loss
- Fully DVB compliant — accepted worldwide standard
- Continuous variable baud rate from 3 to 45 Msps — common hardware for different applications
- Patented internal variable rate root raised cosine filtering
- Fixed rate sample clock — lower system cost ; external tunable oscillators not required
- All digital carrier tracking algorithm — permits frequency multiplexing
- Post filtering AGC — stable performance, near optimum implementation loss
- Programmable frequency sweep circuits — minimal processor overhead required
- Noise measurement function — facilitates antenna steering with high SNR
- I²C or simple 8-bit microcontroller interface — compatible with many processors
- Glueless interface to OTI-8211 MPEG-2 decoder
- Provides 3- or 5-volt interface — compatible with wide variety of interface components
- Access to tracking loop registers — accurate frequency error monitoring



OAK TECHNOLOGY

OTI-8511

DVB-Compliant QPSK Demodulator

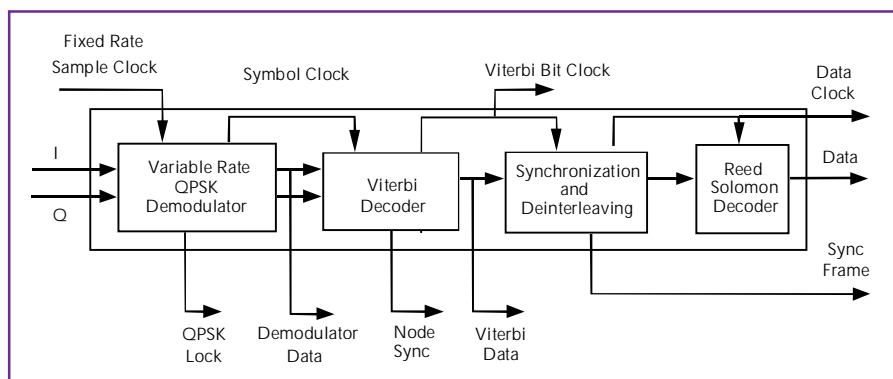
The OTI-8511 is a highly integrated, single-chip variable, data-rate digital QPSK demodulator with embedded deinterleaver and error correction circuitry.

The OTI-8511 is fully compliant with the Digital Video Broadcast (DVB) specification for digital satellite broadcasts. It is designed for specific applications within the consumer and communication markets including direct-to-home video set-top box, VSAT, and other communication applications requiring QPSK demodulation and error correction.

Functional Overview

The OTI-8511 is a single chip DVB-S compatible QPSK receiver that demodulates, deinterleaves, and error corrects DVB-S signal formats. This chip integrates a variable-rate QPSK demodulator with a deinterleaver, Viterbi, and Reed Solomon decoder. Both the symbol timing and carrier tracking loops are implemented digitally, which eliminate the need for external connections to analog tuning components. An I²C interface or 8-bit parallel interface is provided to set appropriate register parameters and periodically read specific status registers.

Baseband in-phase (I) and Quadrature (Q) inputs are generated by external A/D converters and applied to the OTI-8511 at a fixed sampling rate. Carrier frequency error associated with these samples is removed digitally during tracking operations by a complex multiplier and numerically controlled oscillator (NCO). A patented polyphase filter performs the root raised cosine filtering and drives the symbol timing circuitry performing symbol timing of the frequency corrected baseband samples. The digital tracking-loop error may be read by the host processor, which can compute frequency corrections to the L-band tuner to compensate for tuner drift. The demodulator provides a 3-bit soft decision output to the Viterbi decoder portion of the chip. The Viterbi decoder can decode rates of 1/2, 2/3, 3/4, 5/6, and 7/8. Next, the deinterleaver and Reed Solomon circuits perform the synchronization, deinterleaving, and final error correction. The Reed Solomon is N=204, K=188, and T=8. A noise estimation circuit is provided to facilitate antenna installation and provide an estimate of signal strength over the range of SNR between 4dB and 20dB.



OTI-8511 Functional Block Diagram

OTI-8511 Product Brief

DBS Receiver



Typical DBS Receiver Using OTI-8511 and OTI-8211

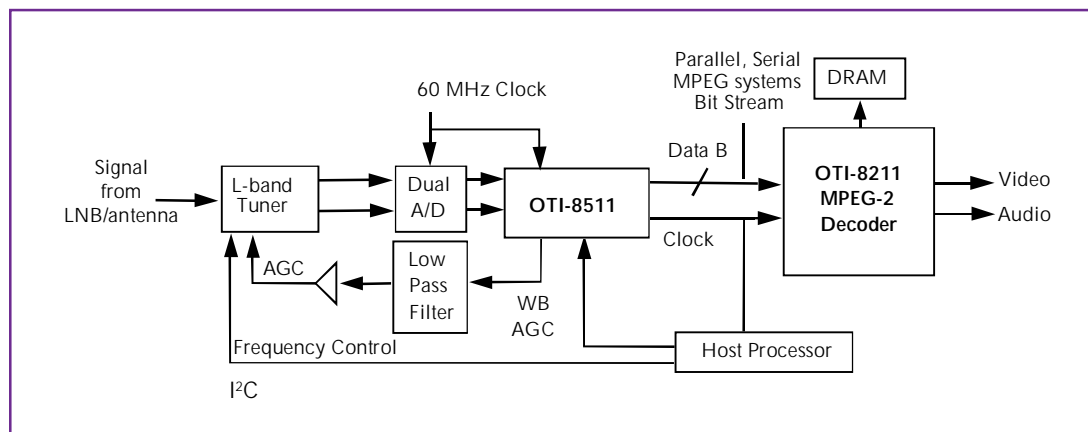
The Oak Technology OTI-8211 MPEG-2 decoder provides the core digital processing technology for a DBS receiver conforming with the DVB standard for satellite reception. A tuner accepts an L-band RF input from the antenna/LNB assembly located outside the building. A host processor controls the tuner to the nominal center frequency of the target signal. Baseband I and Q outputs are applied to an A/D converter pair that is sampled at a fixed rate (60 MHz) as illustrated in the example below. The tuner is required to filter the received passband signal to a bandwidth less than the sampling rate, but is not required to perform matched filtering or adjacent channel rejection.

Once the OTI-8511 has locked to the target signal, the host processor may read the internal registers through the OTI-8511 I²C, 8-bit parallel bus, or internal registers to determine the steady state frequency error. This error could be used to make periodic corrections to the programmed frequency of the tuner PLL or calibrate system parameters.

The OTI-8511 provides a 1-bit sigma delta output that can be used to control the analog AGC in the tuner. This digital signal must be filtered and amplified before applying it to the AGC control element. When the loop is closed, the signal applied to the A/D converters is optimally scaled.

The output of the OTI-8511 is designed to be compatible with the OTI-8211 MPEG-2 decoder, with no required glue logic. The output of the OTI-8511 is an 8-bit parallel data bus and clock. If the maximum symbol rate is less than 35 Mbaud, the OTI-8511 can share the 50 MHz clock that drives the OTI-8211. For Baud rates as high as 45 Mbaud, the OTI-8511 must be driven with a 60 MHz sampling clock.

The OTI-8511 supports both a serial I²C interface and 8-bit parallel interface. It has been designed to minimize the interaction with the host processor. A complete satellite network interface module (NIM) reference design is available along with supporting software.



DBS Receiver Block Diagram

OTI-8511 Product Brief

Technical Specifications



Physical Description

- OTI-8511 DVB-compliant QPSK demodulator

Package/Process

- 100-pin PQFP
- 0.5 μ triple-layer metal process

System Interfaces

Inputs

- Baseband in-phase (I)
- Quadrature (Q)

Outputs

- 8-bit parallel data bus for MPEG system and transport bit streams
- Serial output for MPEG system and transport bit streams clock

Microcontroller Interfaces

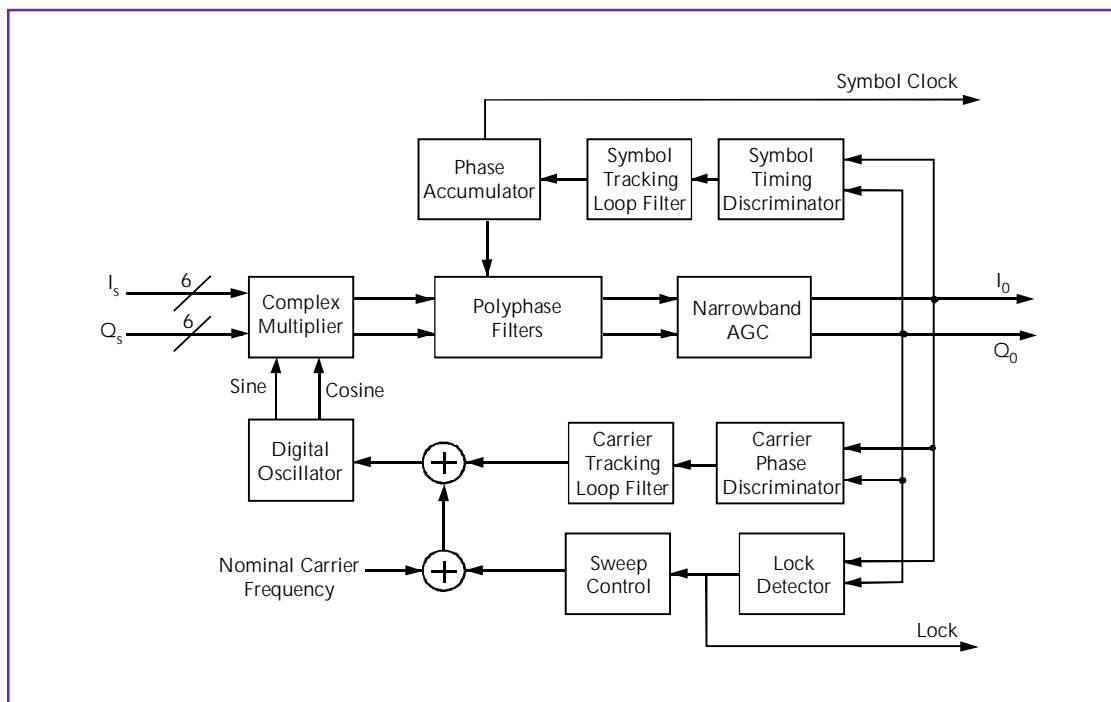
- 8-bit parallel host interface, compatible with Intel 80xx and Motorola architectures
- I²C Interface — slave device, transmitter or receiver

Demodulator Specifications

- Symbol rate — 3 mbaud — 45 mbaud
- Symbol rate resolution — clock/ 2^{20}
- Viterbi data rate — clock Mbps
- Reed Solomon data rate — <0.92 clock Mbps
- Implementation loss — 0.25dB

Power Requirements

- 3- or 5-volt interface
- Power dissipation — 1.6 watts



Internal Configuration Diagram



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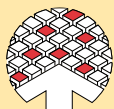
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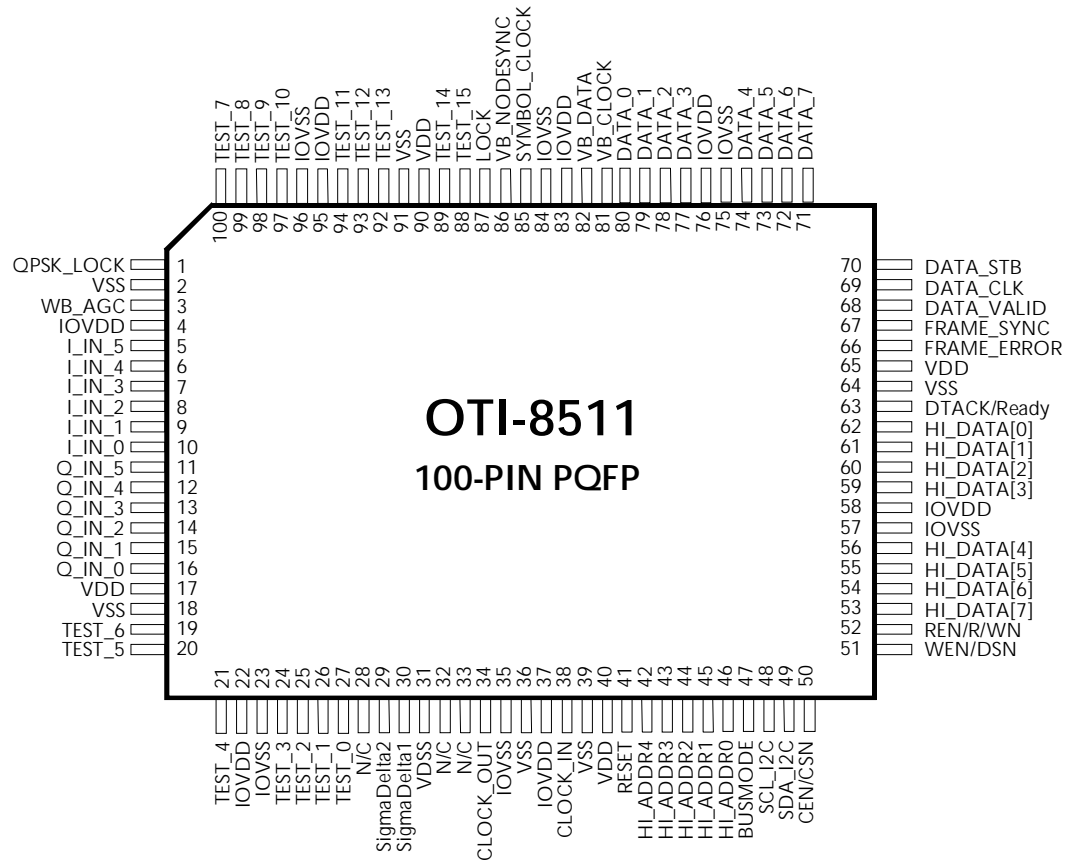
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OAK TECHNOLOGY



OTI-8511 Pinouts

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