ULC Design Checklist

TEMIC Semiconductors

(Please complete and include with ULC design data package)
To complete feasibility or start conversion, all questions must be answered

1. Customer	Technical Contact
Company:	Name/Position: .....
Address:.....	Tel: .....
	Fax:.....
City/State/Zip Code.....	Email Address.....

2. Design Files on 3 1/2 or 5 1/4 floppy (see Table 1).....❒ Incl.

3. Simulation Vectors .....❒ None ..❒ Incl.
   Vector files of simulations from I/O pins.. .....❒ No .....❒ Yes
   Vector files of simulations that include internal nodes as "I/Os" .....❒ No .....❒ Yes
   Vectors from I/Os provide 85% Fault Coverage .....❒ No .....❒ Yes
   Vectors toggle all I/O pins.....❒ No .....❒ Yes

4. Technical Input Data (Specification)
   FPGA part type:_____
   Block Diagram that identifies the major circuit blocks in the design and shows data flow, and/or a full schematic.....❒ Incl.
   Short description of functional blocks including any special features.....❒ Incl.
   Pinout table of the device with all pins labeled with signal name, function, pull-ups/downs, etc.,.....❒ Incl.
   Layout software used, and version number: _____

5. Input and Output Levels
   Inputs: ❒ Some Schmidt triggers (list)....❒ Some CMOS required (list).....❒ All CMOS.....❒ All TTL
   Outputs: V_{OH} value for testing I_{OH}:.....❒ TEMIC Std, 2.4V (TTL) or ❒ 3.84V (CMOS)
   Full 0-V_{DD} swing required on any output pin.....❒ No....❒ Yes

6. Critical Timing Information
   List of Setup/Hold times on input pin(s) and output pin(s) .....❒Incl.
   List of Min/Max propagation or clock delays from input pin to output pin.....❒Incl.
   AND/OR: Timing diagram specification for each pin.....❒Incl.
   Asynchronous input/output timing requirements.....❒ None..❒ Incl.

7. Clocking Scheme Information
   Number of clocks:_____
   Internally generated clock(s) .....❒ No .....❒ Yes
   Description of synchronization circuitry and clocking scheme.....❒ Incl.
   Circuitry (counters, state machines, etc.) requires > 1,000 external clocks to toggle .....❒ No .....❒ Yes
   Combinational feedback.....❒ Unkn... ❒ Some ..❒ None

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8. Initialization Information

Global Reset Pin (Master Clear)..... ❒ No ❒ Yes
or: Initialization/Reset Sequence (partial reset and sequence)..... ❒ No ❒ Yes
SRAM-programmed FPGAs only: Power-up programming protocol..... ❒ N/A ❒ Incl.

9. Environmental..... ❒ Commercial (0°C-70°C) ..... ❒ Industrial (-40°C-85°C) ..... ❒ Military Temp (-55°C-125°C)
Processing: ..... ❒ Standard..... ❒ Mil-Std-883B ..... ❒ Other .....

10. Boundary Scan Support (JTAG)..... ❒ FPGA . ❒ TEMIC ❒ ....None

11. Noise Standard? If so, please list:_____..... ❒ None

12. PCI Compliance Required..... ❒ No . ❒ Yes

13. Part Masters in the Required IC Package
OTP (One Time Programmed), 2 programmed devices plus one blank device..... ❒ N/A ❒ Incl.
E-Squared (Electronically Erasable), 2 programmed devices..... ❒ N/A ❒ Incl.
SRAM (Static RAM Programmed), one device ..... ❒ N/A ❒ Incl.

14. Marking Instructions ..... ❒ Incl.

15. Purchase Order ..... ❒ Will Follow ..... ❒ Incl.

Table 1 Design and Simulation file formats

PAL, GAL, FPLD & AMD MACH Files
- ☐ .PDS Source File
- ☐ .JED fuse (with vectors if available)

ACTEL FPGA Files
- ☐ .ADL files
- ☐ .PIN file
- ☐ Viewsim output files

ALTERA "Classic" Design Software Files
- ☐ .ADF file
- ☐ .LEF file
- ☐ .SCH schematic file
- ☐ .JED fuse (with vectors if available)

ALTERA MAX Plus 2 Files
- ☐ All design files: .GDF, .POF, .TDF, .FIT, .RPT,...
- ☐ .SCF sim file

QUICKLOGIC Files
- ☐ .QDF File
- ☐ Viewsim output files

LATTICE pLSI EPLD Files
- ☐ Verilog or EDIF netlist file
- ☐ . LDF file
- ☐ . JED fuse (with vectors if available)

XILINX FPGA Files
- ☐ .XNF netlist file (XNF created by “LCA2XNF -V”)
- ☐ .LCA post layout file
- ☐ .BIT downloadable file
- ☐ .MCS downloadable file (created from .BIT)
- ☐ Viewsim output files

AT&T ORCA FPGA Files
- ☐ EDIF netlist file
- ☐ .BIT programming file
- ☐ Viewsim output files

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Note: See ULC Product book for Viewsim output file format

ULC Design Checklist

TEMIC
Semiconductors

A ULC Design Checklist must be submitted with each design package (each code) for TEMIC to complete a feasibility and accept the design for conversion. Although the part master and purchase order are not required to complete the feasibility study, they are required to start the conversion. The numbering in the ULC Design Checklist Instructions corresponds to the numbering on the Design Checklist.

1. Technical Contact

Provide the name, phone number, fax number, and email address for the designer to contact with questions about the design. While frequent contact is not generally necessary for a ULC conversion, it is occasionally necessary to ask a question.

2. Design Files

The required design file formats and the optional simulation vector file formats are listed in Table 1. These may be transmitted on a DOS floppy, or electronically via Internet or BBS.

3. Simulation Vectors

Simulation vectors are optional for most ULC conversions; however, if they are not provided, there will be a significant impact on the conversion time, as they will have to be developed by TEMIC. Simulation vectors from I/O pins are directly usable. Others, where internal nodes are used as inputs and outputs to the simulation, are wanted as well but are not directly useful. The test vector files required are listed in Table 1, along with the required design files. See the ULC Databook for more information about vector formats. A vector set should have 85% fault coverage, and all signal pins must toggle.

4. Technical Input Data (Specification)

Block diagram, schematic, description and pinout
Since TEMIC is performing the verification of a ULC conversion, it is generally necessary to develop some understanding of what is happening inside. The documentation requested here is the minimum necessary to meet this requirement: 1) A block diagram that identifies the major circuit blocks in the design and shows the flow of the signals from inputs to outputs is required. A full schematic should be provided if available, and may be in lieu of a block diagram. 2) A pinout description is required. A schematic representation of the device with all pins labeled with signal names as produced by many design packages is helpful. At a minimum, all pins should be defined: input, output, I/O, V_{DD}, GROUND, clock, etc. Any special requirements on any pins should also be identified here, such as pull-ups, pull-downs, CMOS vs. TTL levels, special drive, etc. 3) A functional description of the circuit and how it works in your application is required. Please identify and give a short description of the function of all major blocks and identify any special features such as a counter that resets itself after n counts. This description can typically be handled in 1/2 page for moderate-sized designs.

Miscellaneous
Any other information that you feel would be useful to know in converting your design. TEMIC is committed to give you the best product possible. In particular, if there were problem areas during the original FPGA or PLD design, this information is frequently useful to know for the conversion.

5. Input and Output Levels

Some FPGAs allow use of CMOS levels on inputs or outputs. Select the appropriate threshold levels for inputs. Some FPGAs, such as Xilinx and Actel define V_{OH}=3.84V min. @ rated I_{OH}. These devices also typically have outputs which will swing "rail-to-rail", even though this is not specified. The default specification for ULC outputs is a standard TTL compatible specification: V_{OH}=2.4V min. @ rated I_{OH}, and the standard outputs on smaller ULCs will not swing "rail-to-rail". These ULC drivers will not have any trouble driving TTL compatible inputs but may cause problems driving any linear circuitry such as resistor networks, caps, LEDs, integrators, etc. If you require V_{OH}=3.84V min. and/or "rail-to-rail" output swing, please indicate; this will preclude the use of the UD technology and may require a re-quote.

6. Critical Timing Information

The system timing requirements should be identified along with any special requirements for pin to pin propagation, setup, or hold times. For PAL-architecture devices, the timing is adequately described by the PLD device datasheet, but for FPGAs timing is more a function of the design and specific layout than the datasheet parameters. Any special problems encountered with the speed or routing of the PLD or FPGA should be noted. Timing diagrams for each pin would be ideal. Describe any asynchronous input and output timing requirements.

7. Clocking Scheme Information

Identify all clock pins and the overall clocking scheme used in the design. This includes internally derived clocks and an explanation of how the clocks interact with each other (multiple clock sequence). Clocks and clock pins should be identified both in the description and on the block diagram. Latch enable description should also be included.

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8. Initialization Information

Initialization/reset sequence
In order to verify and test the ULC all flip flops must be able to be set to a known state. It is best to use a Global Reset (Master Clear) pin to reset all flip flops to a known state. If not in the FPGA already, this usually can be easily added when converting to the ULC. If a Global Reset pin cannot be used, and you, the customer, are providing test vectors, the first part of your functional input vector set should be the input pattern required to bring the entire design to a known state. This includes resetting or loading all memory devices or registers/latches and all counters, resetting all combinational feedback loops, and initializing all state machines. If you are not providing vectors for your design, the ULC designer will create these initial vectors. For this, you must provide a very detailed description of the logic, identifying the initial states and sequences on all pins, even "don't cares". The most effective format to provide this is a truth table format (see the ULC Product Description book, Test Vectors, for an example).

Resetability
The Actel architecture does not have a built-in master reset or power-on reset function, which is provided for all other PLD and FPGA architectures. It is therefore necessary to explicitly design-in reset capability into an Actel design, either with a specific reset pin or a specific set of input vectors which will perform the required initialization as described above. Any Actel design without this capability cannot be converted. For other FPGA and PLD types, it is not recommend to rely on the built-in power-on reset for proper operation of your circuit, however, as this function is typically not reliable.

Power-up programming protocol
This only applies to SRAM based FPGAs such as Xilinx LCA's and Altera 8000 and 10K series. These are volatile devices which must be programmed on power-up each time. Identify the power-up programming scheme used and if the system is monitoring any of the programming pins. By default these pins are not supported. In most cases emulation can be provided if required, but this is done on a case by case basis as required.

9. Environmental

Check required temperature range and any special processing requirements.

10. JTAG Support

For devices that support the JTAG standard, such as Xilinx XC4000 series, Altera Flex 8000 series and the Lattice pLSI3000 series, TEMIC can provide support for this feature. Please indicate whether you require this support.

11. Noise Standard

If you have any noise standard that must be met, state the standard name, number, and general requirements. TEMIC ULCs have programmable clock skew capability, so your noise needs can be met.

12. PCI Compliance

TEMIC can support the PCI (Peripheral Component Interconnect) standard. The UG series technology will be required.

13. Part Masters

These are required for TEMIC' "Verify-before-silicon" process.. Please double-check that the masters provided match the files provided (source files, programming files, and simulation files). Miss-matched parts and files are a frequent source of delays in the conversion process.

14. Marking Instructions

ULCs are marked with the ULC part number, TEMIC' custom program number, and have a line available for your custom program number. The desired part number must be provided. Alternatively, a detailed marking specification may be submitted if you require, which could include your company's logo, for example. Non-standard markings may impact the cost.

15. Purchase Order

A purchase order, with deliveries contingent on prototype acceptance, which meets the minimums specified in our quotation, is required to begin the conversion.