

# DATA SHEET

## **TSA5515T** 1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

Product specification  
File under Integrated Circuits, IC02

November 1991

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

## TSA5515T

## GENERAL DESCRIPTION

The TSA5515T is a single chip PLL frequency synthesizer designed for TV tuning systems. Control data is entered via the I<sup>2</sup>C-bus; five serial bytes are required to address the device, select the oscillator frequency, programme the three output ports and set the charge-pump current. A flag is set when the loop is "in-lock". Another flag is set when a power dip occurs on the supply line. These flags are read out of the TSA5515T on SDA line (one status byte) during a READ operation. The device has 4 programmable addresses, programmed by applying a specific voltage on the AS pin. The phase comparator operates at 7.8125 kHz when a 4 MHz crystal is used.



- In-lock flag
- Varicap drive disable
- Low radiation
- Address selection for Picture-In-Picture (PIP), DBS tuner, etc.
- 3 bus-controlled output ports
- Power-down flag
- Available in SOT108A package

## FEATURES

- Complete 1.3 GHz single-chip system
- Low power 5 V, 35 mA
- I<sup>2</sup>C-bus programming

## APPLICATIONS

- TV tuners
- VCR tuners

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	–	5	–	V
I <sub>CC</sub>	supply current	–	35	–	mA
Δf	frequency range	64	–	1300	MHz
V <sub>I (RMS)</sub>	input voltage level (RMS value)				
	80 MHz to 150 MHz	12	–	300	mV
	150 MHz to 1 GHz	9	–	300	mV
	1 GHz to 1.3 GHz	40	–	300	mV
f <sub>XTAL</sub>	crystal oscillator	3.2	4	4.48	MHz
I <sub>O</sub>	open-collector output current				
	P7	–	–	5	mA
	P1, P2	–	–	20	mA
T <sub>amb</sub>	operating ambient temperature range	–10	–	80	°C
T <sub>stg</sub>	storage temperature range	–40	–	125	°C
R <sub>th j-a</sub>	thermal resistance	–	110	–	K/W

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TSA5515T	14	SO	plastic	SOT108A <sup>(1)</sup>

## Note

1. SOT108-1; 1996 December 3.

### 1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

### TSA5515T

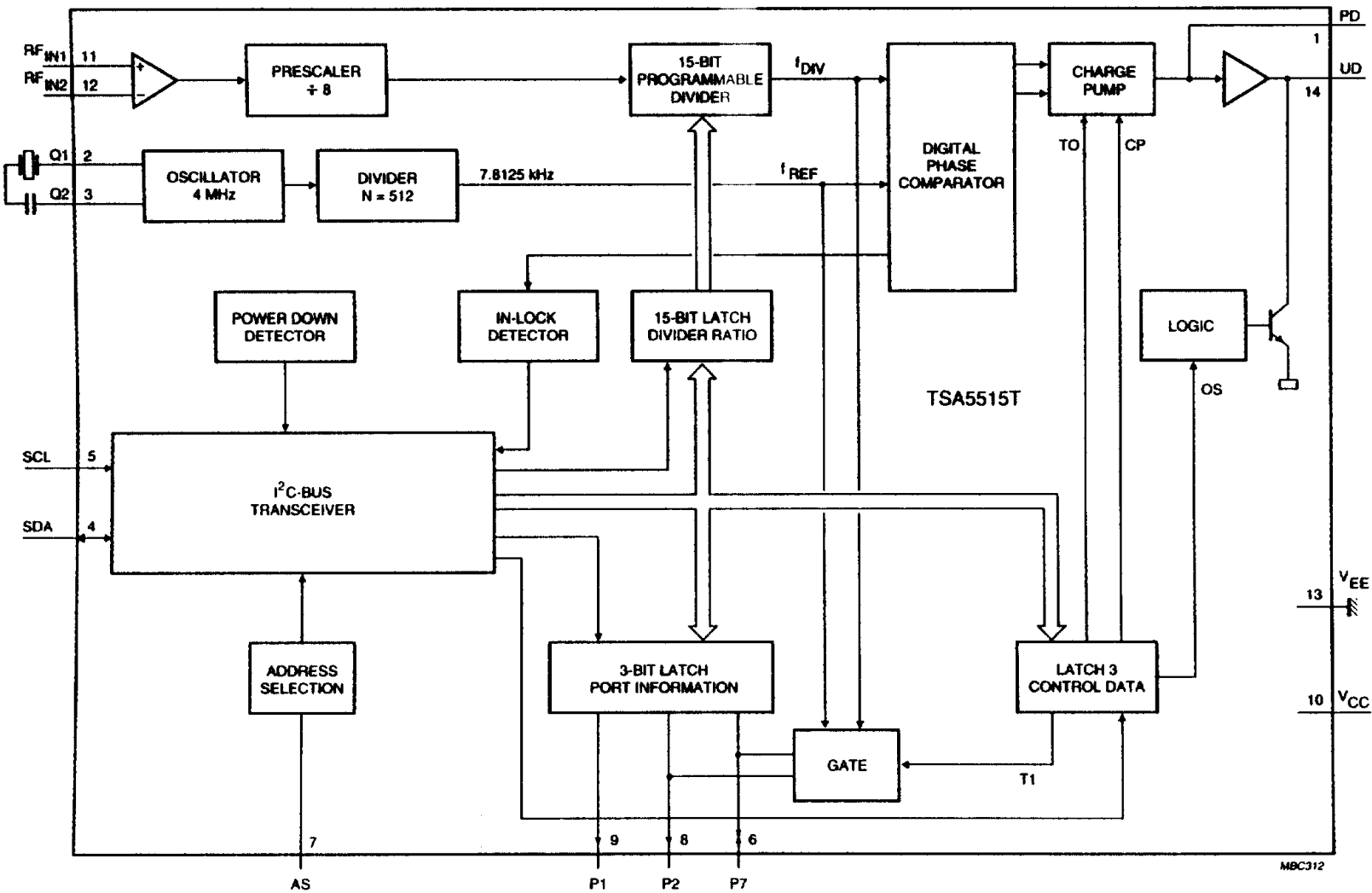


Fig.1 Block diagram

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**LIMITING VALUES**

In accordance with Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	-0.3	6	V
V <sub>P1</sub>	charge-pump output voltage	-0.3	V <sub>CC</sub>	V
V <sub>P2</sub>	crystal (Q1) input voltage	-0.3	V <sub>CC</sub>	V
V <sub>P4</sub>	serial data input/output	-0.3	6	V
V <sub>P5</sub>	serial clock input	-0.3	6	V
V <sub>P7</sub>	address selection	-0.3	6	V
V <sub>P6</sub>	output ports P7, P2, P1	-0.3	16	V
V <sub>P11</sub>	prescaler inputs	-0.3	2.5	V
V <sub>P14</sub>	drive output	-0.3	V <sub>CC</sub>	V
I <sub>6L</sub>	output port P7 (open collector)	-1	10	mA
I <sub>8L</sub>	output port P2, P1 (open collector)	-1	25	mA
I <sub>4L</sub>	SDA output (open collector)	-1	5	mA
T <sub>stg</sub>	storage temperature range	-40	125	°C
T <sub>j</sub>	junction temperature	-	125	°C

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	THERMAL RESISTANCE
R <sub>th j-a</sub>	from junction to ambient in free air	110 K/W

**HANDLING**

Every pin withstands the ESD test in accordance with MIL-STD-883C, category A (&gt; 1500 V).

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**PINNING**

SYMBOL	PIN	DESCRIPTION
PD	1	charge-pump output
Q1	2	crystal oscillator input 1
Q2	3	crystal oscillator input 2
SDA	4	serial data input/output
SCL	5	serial clock input
P7	6	port output
AS	7	input for address selection
P2	8	port output
P1	9	port output
V <sub>CC</sub>	10	voltage supply
RF <sub>IN1</sub>	11	UHF/VHF signal input 1
RF <sub>IN2</sub>	12	UHF/VHF signal input 2 (decoupled)
GND	13	ground
UD	14	drive output

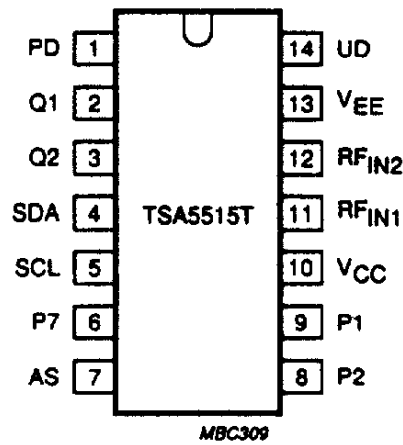


Fig.2 Pinning diagram.

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

## TSA5515T

**FUNCTIONAL DESCRIPTION**

The TSA5515T is controlled via the two-wire I<sup>2</sup>C-bus. For programming, there is one module address (7 bits) and the R/W bit for selecting READ or WRITE mode.

**WRITE mode:****R/W = 0 (see Table 1)**

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the TSA5515T. The bus transceiver has an auto-increment facility, which permits the programming of the TSA5515T within one single transmission (address + 4 data bytes).

The TSA5515T can also be partly programmed on the condition that the first data byte following the address is

byte 2 or byte 4. The meaning of the bits in the data bytes is given in Table 1. The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or charge pump and port information (first bit = 1) will follow. Until an I<sup>2</sup>C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning. At power-on, the ports are set to the high impedance state.

The 7.8125 kHz reference frequency is obtained by dividing the output of the 4 MHz crystal oscillator by 512. Because the input of the UHF/VHF signal is first divided by 8, the step size is 62.5 kHz. A 3.2 MHz crystal can offer a step size of 50 kHz.

**Table 1 Write data format**

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	byte 1
Programmable divider	0	N14	N13	N12	N11	N10	N9	N8	A	byte 2
Programmable divider	N7	N6	N5	N4	N3	N2	N1	N0	A	byte 3
Charge-pump and test bits	1	CP	T1	T0	X	X	X	OS	A	byte 4
Output ports control bits	P7	X	X	X	X	P2	P1	X	A	byte 5

MA1, MA0 programmable address bits (see Table 3)

A acknowledge bit

N14 to N0 programmable divider bits

$$N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2^1 + N0$$

CP charge-pump current

CP = 0 50  $\mu$ A

CP = 1 220  $\mu$ A

P7, P2, P1 = 1 open-collector outputs are active

P7, P2, P1 = 0 outputs are in high impedance state

T1, T0, OS = 0 0 0 normal operation

T1 = 1, P2 =  $f_{ref}$ , P7 =  $f_{DIV}$

T0 = 1 3-state charge-pump

OS = 1 operational amplifier output is switched off (varicap drive disable)

**Note**

1. X = don't care

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**READ mode:**  
**R/W = 1 (see Table 2)**

Data can be read out of the TSA5515T by setting the R/W bit to 1. After the slave address has been recognized, the TSA5515T generates an acknowledge pulse and the first data byte (status word) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a high position of the SCL clock signal.

A second data byte can be read out of the TSA5515T if the processor generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge from the

processor occurs. The TSA5515T will then release the data line to allow the processor to generate a STOP condition.

The POR flag (power-on-reset) is set to 1 when V<sub>CC</sub> goes below 3 V and at power-on. It is reset when an end of data is detected by the TSA5515T (end of a READ sequence). Control of the loop is made possible with the in-lock flag FL, which indicates (FL = 1) when the loop is phase-locked.

**Table 2** Read data format

	MSB						LSB			
Address	1	1	0	0	0	MA1	MA0	1	A	byte 1
Status byte	POR	FL	1	1	1	1	1	1	–	byte 2

**Notes**

1. POR power-on-reset flag. (POR = 1 on power-on)
2. FL in-lock flag (FL = 1 when the loop is phase-locked).

MSB is transmitted first.

**Address selection (see Table 3)**

The module address contains programmable address bits (MA1 and MA0), which offer the possibility of having several synthesizers (up to 4) in one system. The relationship between MA1 and MA0 and the input voltage on AS input is given in Table 3.

**Table 3** Address selection

MA1	MA0	Voltage applied on AS pin
0	0	0 to 0.1 V <sub>CC</sub>
0	1	open
1	0	0.4 to 0.6 V <sub>CC</sub>
1	1	0.9 V <sub>CC</sub> to V <sub>CC</sub>

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

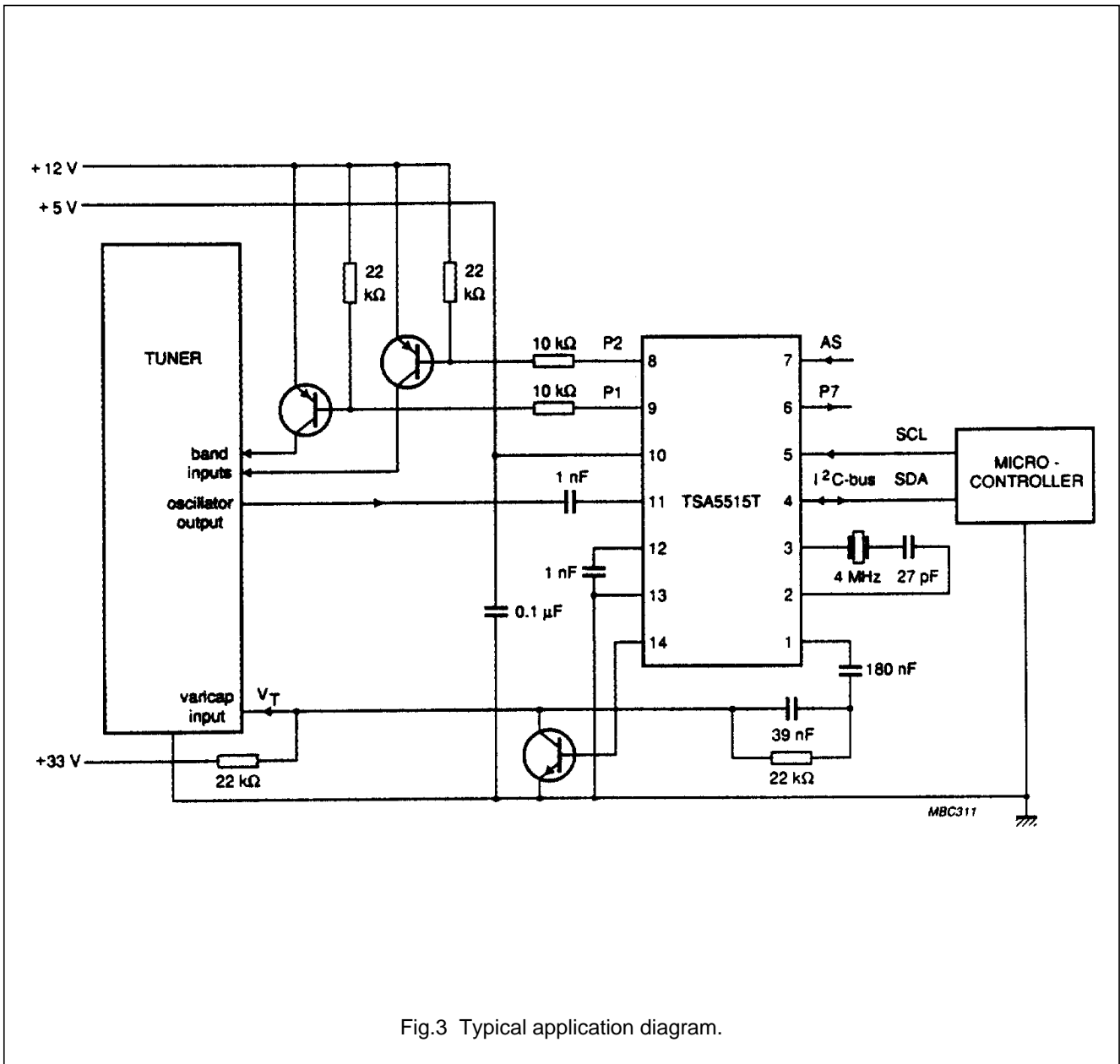


Fig.3 Typical application diagram.



1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**CHARACTERISTICS** $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage range		4.5	–	5.5	V
$T_{amb}$	operating ambient temperature range		–10	–	80	°C
$f_{CLK}$	clock input frequency range		64	–	1300	MHz
N	divider		256	–	32767	
$I_{CC}$	supply current		25	35	50	mA
$f_{XTAL}$	crystal oscillator frequency		3.2	4	4.48	MHz
$Z_I$	input impedance (pin 2)		–480	–400	–320	$\Omega$
$V_I$ (RMS)	input voltage level (RMS value) f = 80 to 150 MHz f = 150 to 1000 MHz f = 1000 to 1300 MHz	$V_{CC} = 4.5$ to $5.5\text{ V}$ ; $T_{amb} = -10$ to $80\text{ °C}$ see typical sensitivity curve in Fig.4	12 9 40	– – –	300/2.6 300/2.6 300/2.6	mV mV mV
$R_I$	prescaler input impedance	see Smith chart in Fig.5	–	50	–	$\Omega$
$C_I$	input capacitance		–	2	–	pF
<b>Output ports (open collector) (see note 1)</b>						
$I_{LO}$	leakage current	$V_{6H} = 13.5\text{ V}$	–	–	10	$\mu\text{A}$
$V_{OL}$	output voltage LOW (P7)	$I_{6L} = 5\text{ mA}$ note 2	–	–	0.5	V
	output voltage LOW (P2, P1)	$I_{8L} = 20\text{ mA}$ note 2	–	–	0.5	V
<b>Address selection input (AS)</b>						
$I_{IH}$	input current HIGH	$V_{7H} = 5\text{ V}$	–	–	20	$\mu\text{A}$
$I_{IL}$	input current LOW	$V_{7L} = 0$	–20	–	–	$\mu\text{A}$
<b>Bus inputs SCL, SDA</b>						
$V_{IH}$	input voltage HIGH		3	–	5.5	V
$V_{IL}$	input voltage LOW		–	–	1.5	V
$I_{IH}$	input current HIGH	$V_{5H} = 5\text{ V}$ ; $V_{CC} = 0$	–	–	10	$\mu\text{A}$
		$V_{5H} = 5\text{ V}$ ; $V_{CC} = 5\text{ V}$	–	–	10	$\mu\text{A}$
$I_{IL}$	input current LOW	$V_{5L} = 0$ ; $V_{CC} = 0$	–10	–	–	$\mu\text{A}$
		$V_{5L} = 0$ ; $V_{CC} = 5\text{ V}$	–10	–	–	$\mu\text{A}$
<b>Output SDA (open collector)</b>						
$I_{LO}$	leakage current	$V_{4H} = 5.5\text{ V}$	–	–	10	$\mu\text{A}$
$V_{4L}$	output voltage	$I_{4L} = 3\text{ mA}$	–	–	0.4	V
$V_{14}$	output voltage	$V_{1L} = 0$	–	–	100	mV

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

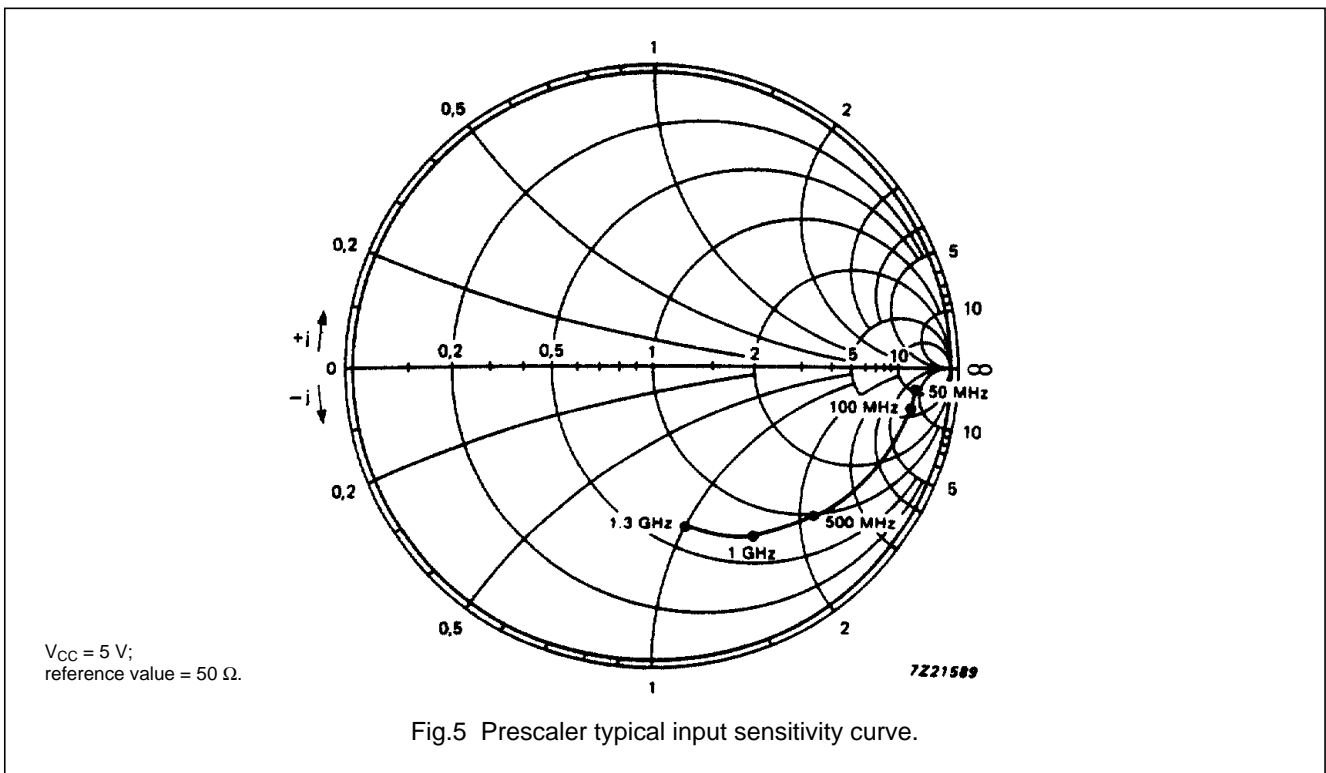
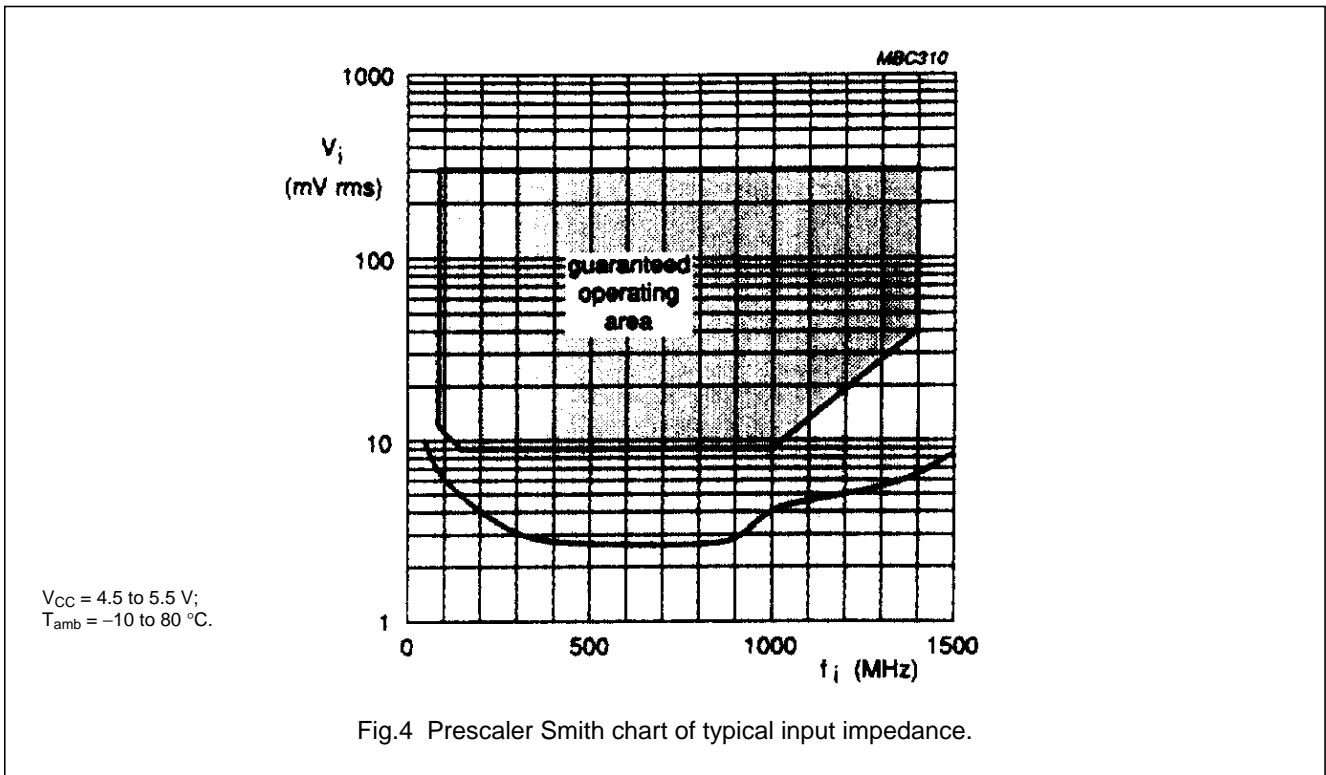
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Charge-pump output PD</b>						
I <sub>IH</sub>	input current HIGH (absolute value)	CP = 1	90	220	300	μA
I <sub>IL</sub>	input current LOW (absolute value)	CP = 0	22	50	75	μA
V <sub>O</sub>	output voltage	in-lock	1.5	–	2.5	V
I <sub>1leak</sub>	off-state leakage current	T0 = 1	–5	–	5	nA
<b>Operational amplifier output UD (test mode: T0 = 1)</b>						
V <sub>14</sub>	output voltage	V <sub>1L</sub> = 0	–	–	100	mV
	output voltage when switched off	T0 = 1; OS = 1; V <sub>1L</sub> = 2 V	–	–	200	mV
h <sub>FE</sub>	operational amplifier current gain $I_{14}/(I_1 - I_{1leak})$	T0 = 1; OS = 0; V <sub>1L</sub> = 2 V; I <sub>14</sub> = 10 μA	2000	–	–	

**Notes to the characteristics**

1. When a port is active, the collector voltage must not exceed 6 V.
2. A maximum of 1 port at the same time may sink 5 or 20 mA, to guarantee V<sub>O</sub> = 0.5 V.

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T



1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**FLOCK FLAG DEFINITION (FL)**

When the FL flag is 1, the maximum frequency deviation ( $\Delta f$ ) from stable frequency can be expressed as follows:

$$\Delta f = \pm(K_{VCO}/K_O) \times I_{CP} \times (C1 + C2) / (C1 \times C2)$$

where;

- $K_{VCO}$  = oscillator slope (Hz/V)
- $I_{CP}$  = charge-pump current (A)
- $K_O$  =  $4 \times 10^6$
- C1 and C2 = loop filter capacitors

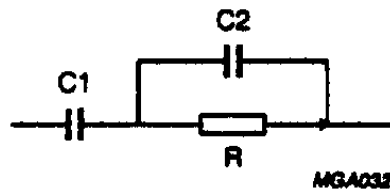


Fig.6 Loop filter

**FLOCK FLAG APPLICATION**

- $K_{VCO} = 16$  MHz/V (UHF band)
- $I_{CP} = 220$   $\mu$ A
- C1 = 180 nF
- C2 = 39 nF
- $\Delta f = \pm 27.5$  kHz.

**Table 4** Flock flag settings

	MIN.	MAX.	UNIT
Time span between actual phase lock and FL-flag setting	1024	1152	$\mu$ s
Time span between the loop losing lock and FL-flag resetting	0	128	$\mu$ s

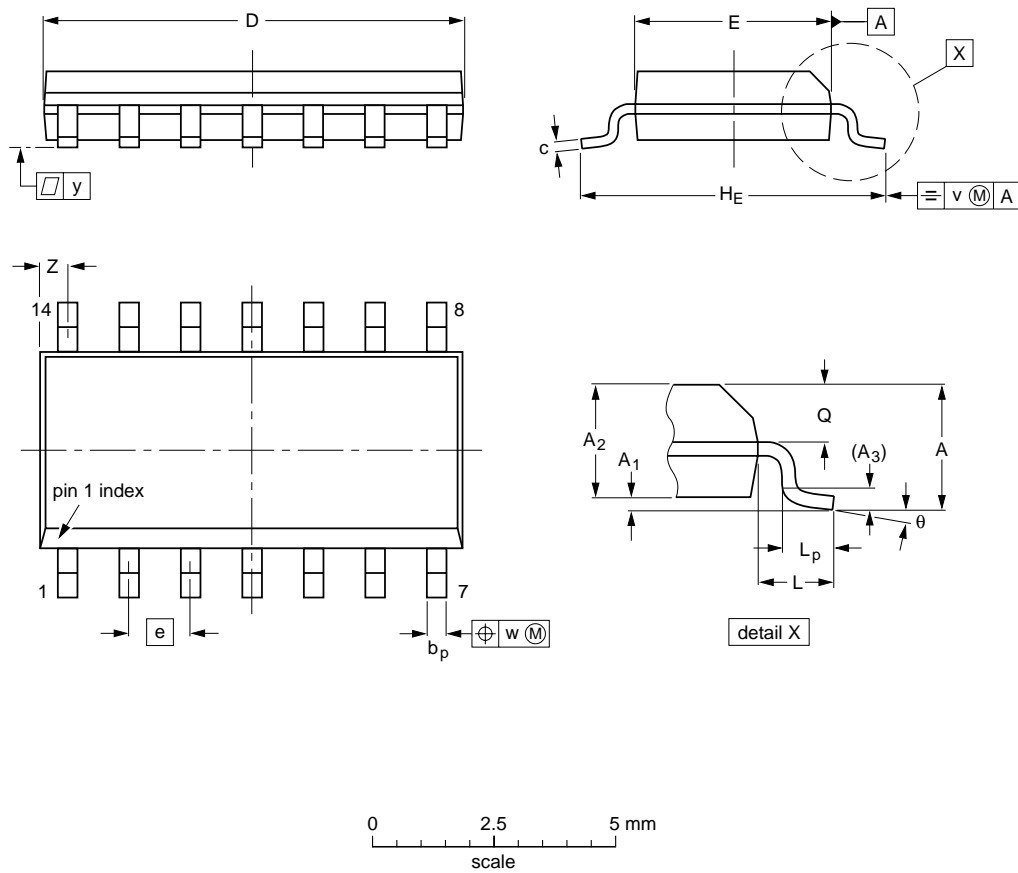
1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

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## 1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

1.3 GHz bi-directional I<sup>2</sup>C-bus controlled synthesizer

TSA5515T

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.