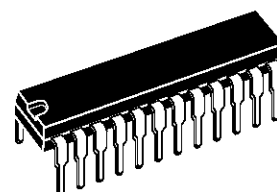


## BUS-CONTROLLED AUDIO MATRIX

- 6 STEREO INPUTS
- 3 STEREO OUPUTS
- GAIN CONTROL 0dB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE
- VERY LOW DISTORSION
- FULLY ESD PROTECTED

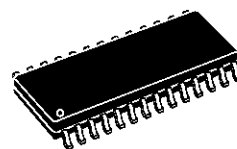
### DESCRIPTION

The TEA6422 switches 6 stereo audio inputs on 3 stereo outputs.  
All the switching possibilities are changed through the I<sup>2</sup>C BUS.



**SHRINK 24**  
(Plastic Package)

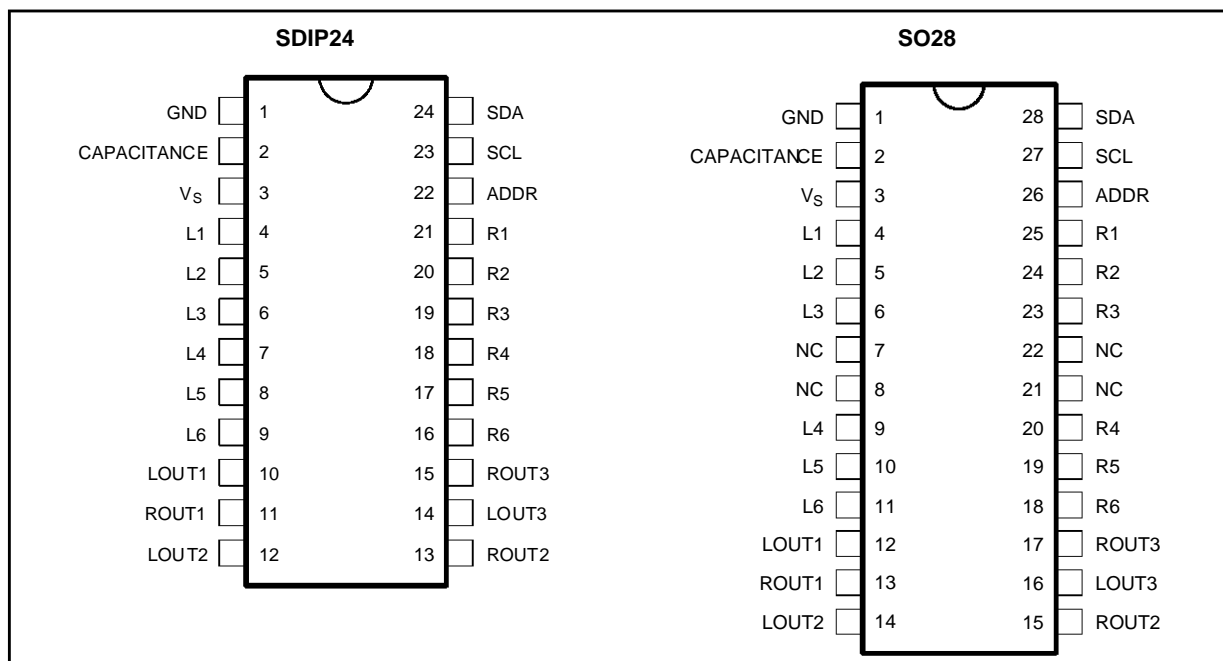
ORDER CODE : TEA6422



**SO28**  
(Plastic Micropackage)

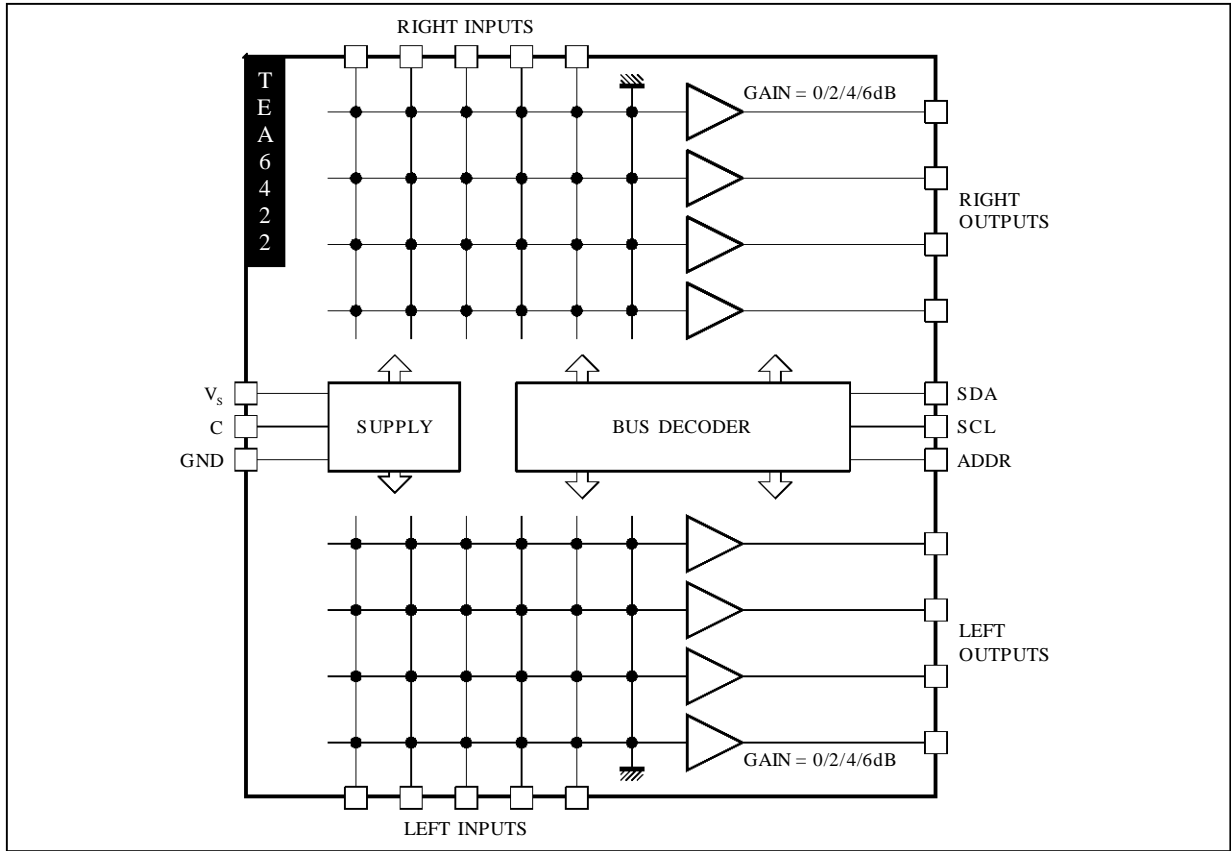
ORDER CODE : TEA6422D

### PIN CONNECTIONS



6422-01.EPS / 6422-02.EPS

**BLOCK DIAGRAM**



6422-03.EPS

**ABSOLUTE MAXIMUM RATINGS**

| Symbol            | Parameter             | Value       | Unit |
|-------------------|-----------------------|-------------|------|
| V <sub>CC</sub>   | Supply Voltage        | 12          | V    |
| T <sub>oper</sub> | Operating Temperature | 0, + 70     | °C   |
| T <sub>stg</sub>  | Storage Temperature   | - 20, + 150 | °C   |

6422-01.TBL

**THERMAL DATA**

| Symbol               | Parameter                             | Value  | Unit |
|----------------------|---------------------------------------|--------|------|
| R <sub>th(j-a)</sub> | Junction - ambient Thermal Resistance | SDIP24 | 75   |
|                      |                                       | SO28   | 75   |

6422-02.TBL

**ELECTRICAL CHARACTERISTICS**

$T_A = 25^{\circ}\text{C}$ ,  $V_S = 9\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $R_G = 600\Omega$ ,  $f = 1\text{kHz}$  (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

**SUPPLY**

|       |                  |  |    |    |      |    |
|-------|------------------|--|----|----|------|----|
| $V_S$ | Supply Voltage   |  | 8  | 9  | 10.2 | V  |
| $I_S$ | Supply Current   |  |    | 3  | 8    | mA |
| SVR   | Ripple Rejection | $V_{IN} = 500\text{mV}_{\text{RMS}}$ , $f = 1\text{kHz}$ | 70 | 80 |      | dB |

**MATRIX**

|          |                    |   |    |     |     |                  |
|----------|--------------------|---|----|-----|-----|------------------|
| $V_{IN}$ | Input DC Level     |   |    | 4.5 |     | V                |
| $R_I$    | Input Resistance   |   | 30 | 50  | 100 | $\text{k}\Omega$ |
| $C_S$    | Channel Separation | $V_{IN} = 2\text{V}_{\text{RMS}}$ , $f = 1\text{kHz}$ | 80 | 90  |     | dB               |

**OUTPUT BUFFER**

|           |                        |   |     |      |      |                         |
|-----------|------------------------|---|-----|------|------|-------------------------|
| $V_{OUT}$ | Output DC Level        |   | 4.2 | 4.5  | 4.8  | V                       |
| $R_{OUT}$ | Output Resistance      |   |     | 50   | 100  | $\Omega$                |
| $e_{NI}$  | Input Noise            | $\text{BW} = 20 - 20\text{kHz}$ , flat      |     | 3    |      | $\mu\text{V}$           |
| S/N       | Signal to Noise Ratio  | $V_{IN} = V_{OUT} = 1\text{V}_{\text{RMS}}$ |     | 110  |      | dB                      |
| G         | Gain                   |   | -1  | 0    | + 1  | dB                      |
| d         | Distortion             | $V_{IN} = V_{OUT} = 1\text{V}_{\text{RMS}}$ |     | 0.01 | 0.05 | %                       |
| $V_{CL}$  | Clipping Level         | $d = 0.3\%$                                 | 2   | 2.5  |      | $\text{V}_{\text{RMS}}$ |
| $R_L$     | Output Load Resistance |   | 2   |      |      | $\text{k}\Omega$        |

6422-03.TBL

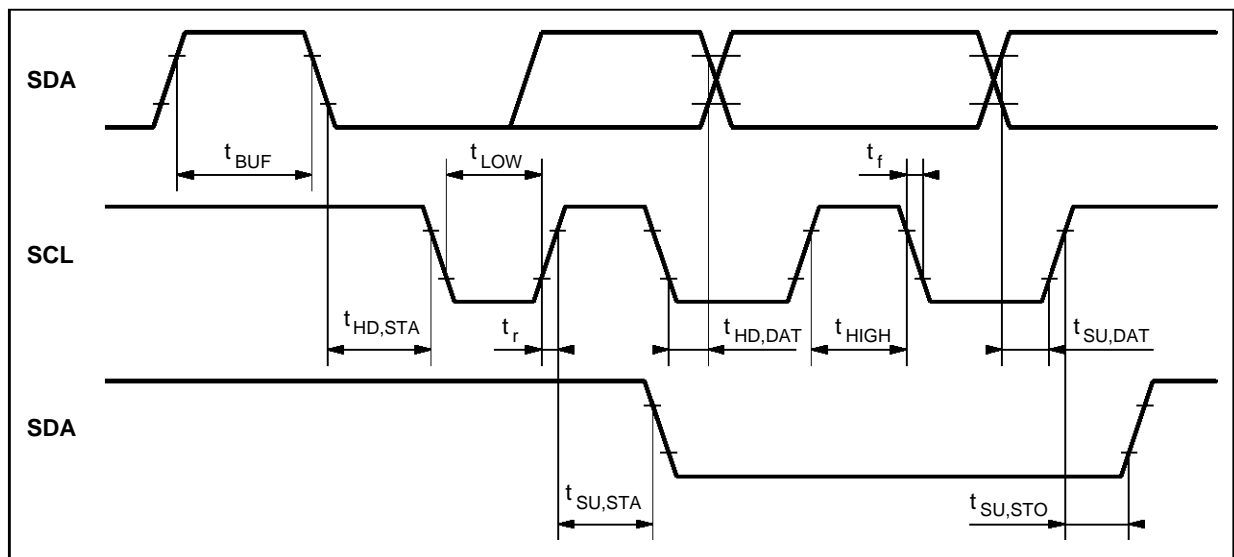
**I<sup>2</sup>C BUS CHARACTERISTICS**

| Symbol           | Parameter                | Test Conditions                       | Min.  | Max.                  | Unit |
|------------------|--------------------------|---------------------------------------|-------|-----------------------|------|
| SCL              |                          |                                       |       |                       |      |
| V <sub>IL</sub>  | Low Level Input Voltage  |                                       | - 0.3 | + 1.5                 | V    |
| V <sub>IH</sub>  | High Level Input Voltage |                                       | 3.0   | V <sub>CC</sub> + 0.5 | V    |
| I <sub>LI</sub>  | Input Leakage Current    | V <sub>I</sub> = 0 to V <sub>CC</sub> | - 10  | + 10                  | μA   |
| f <sub>SCL</sub> | Clock Frequency          |                                       | 0     | 100                   | kHz  |
| t <sub>R</sub>   | Input Rise Time          | 1.5V to 3V                            |       | 1000                  | ns   |
| t <sub>F</sub>   | Input Fall Time          | 1.5V to 3V                            |       | 300                   | ns   |
| C <sub>I</sub>   | Input Capacitance        |                                       |       | 10                    | pF   |

|                 |                          |                                       |       |                       |    |
|-----------------|--------------------------|---------------------------------------|-------|-----------------------|----|
| SDA             |                          |                                       |       |                       |    |
| V <sub>IL</sub> | Low Level Input Voltage  |                                       | - 0.3 | + 1.5                 | V  |
| V <sub>IH</sub> | High Level Input Voltage |                                       | 3.0   | V <sub>CC</sub> + 0.5 | V  |
| I <sub>LI</sub> | Input Leakage Current    | V <sub>I</sub> = 0 to V <sub>CC</sub> | - 10  | + 10                  | μA |
| C <sub>I</sub>  | Input Capacitance        |                                       |       | 10                    | pF |
| t <sub>R</sub>  | Input Rise Time          | 1.5V to 3V                            |       | 1000                  | ns |
| t <sub>F</sub>  | Input Fall Time          | 1.5V to 3V                            |       | 300                   | ns |
| V <sub>OL</sub> | Low Level Output Voltage | I <sub>OL</sub> = 3mA                 |       | 0.4                   | V  |
| t <sub>F</sub>  | Output Fall Time         | 3V to 1.5V                            |       | 250                   | ns |
| C <sub>L</sub>  | Load Capacitance         |                                       |       | 400                   | pF |

|                      |  |  |     |     |    |
|----------------------|--|--|-----|-----|----|
| TIMING               |  |  |     |     |    |
| t <sub>LOW</sub>     | Clock Low Period   |  | 4.7 |     | μs |
| t <sub>HIGH</sub>    | Clock High Period  |  | 4.0 |     | μs |
| t <sub>SU, DAT</sub> | Data Set-up Time   |  | 250 |     | ns |
| t <sub>HD, DAT</sub> | Data Hold Time   |  | 0   | 340 | ns |
| t <sub>SU, STO</sub> | Set-up Time from Clock High to Stop                      |  | 4.0 |     | μs |
| t <sub>BUF</sub>     | Start Set-up Time following a Stop                       |  | 4.7 |     | μs |
| t <sub>HD, STA</sub> | Start Hold Time  |  | 4.0 |     | μs |
| t <sub>SU, STA</sub> | Start Set-up Time following Clock Low-to High Transition |  | 4.7 |     | μs |

**Figure 1 : I<sup>2</sup>C Bus Timing**



**POWER ON RESET**

After power-on reset all outputs are in mute mode

| Symbol | Parameter      | Conditions     | Min. | Typ. | Max. | Unit |
|--------|----------------|----------------|------|------|------|------|
| Reset  | Start of Reset | Incr. $V_{CC}$ | 4.5  |      | 2.5  | V    |
|        | End of Reset   | Decr. $V_{CC}$ |      |      | 4.2  | V    |
|        |                | Incr. $V_{CC}$ |      |      |      | V    |

6422-05.TBL

**SOFTWARE SPECIFICATION****1. Chip address**

| Address   | HEX | ADDR |
|-----------|-----|------|
| 1001 1000 | 98  | 0    |
| 1001 1010 | 9A  | 1    |

**2. Data bytes**

Output select

| X | 0<br>0<br>1 | 0<br>1<br>0 | X | X | $l_2$ | $l_1$ | $l_0$ | Output 1<br>Output 2<br>Output 3 |
|---|-------------|-------------|---|---|-------|-------|-------|----------------------------------|
|   |             |             |   |   |       |       |       |                                  |

Input select

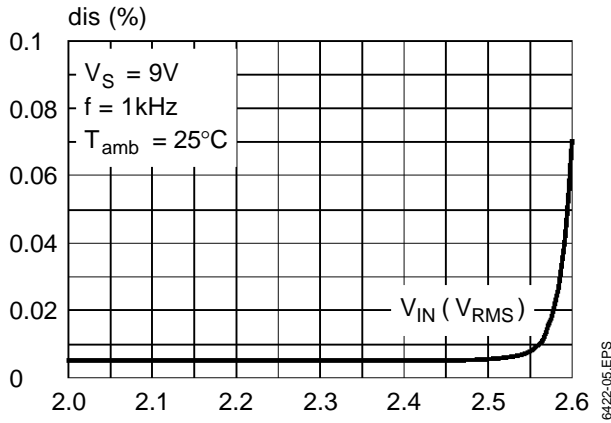
| X | $Q_1$ | $Q_0$ | X | X | 0<br>0<br>0<br>0<br>1<br>1<br>1 | 0<br>0<br>1<br>1<br>0<br>0<br>1 | 0<br>1<br>0<br>1<br>0<br>1<br>0 | Input 1<br>Input 2<br>Input 3<br>Input 4<br>Input 5<br>Input 6<br>Mute |
|---|-------|-------|---|---|---------------------------------|---------------------------------|---------------------------------|--|
|   |       |       |   |   |                                 |                                 |                                 |  |

6422-06.TBL

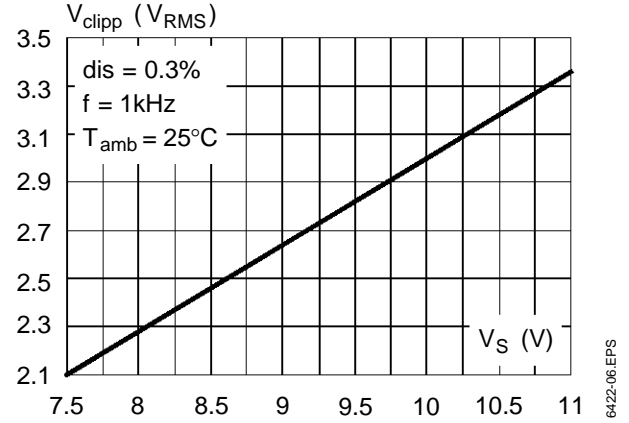
X = don't care - MSB is transmitted first

**Example :** 0 10 XX 10Q connects outputs 3 with input 5.

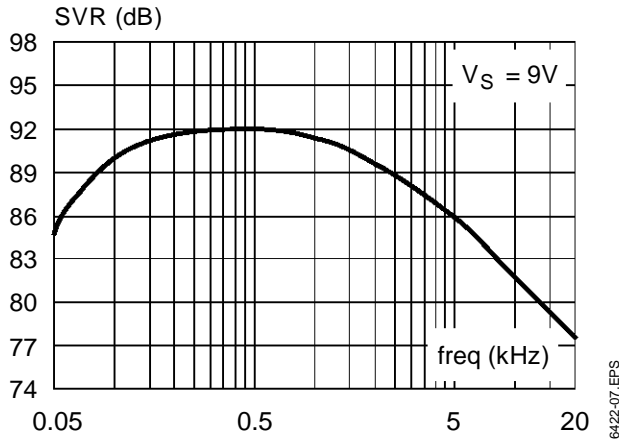
**Figure 2 : Distorsion Level versus Input Voltage**



**Figure 3 : Clipping Level versus Supply Voltage**

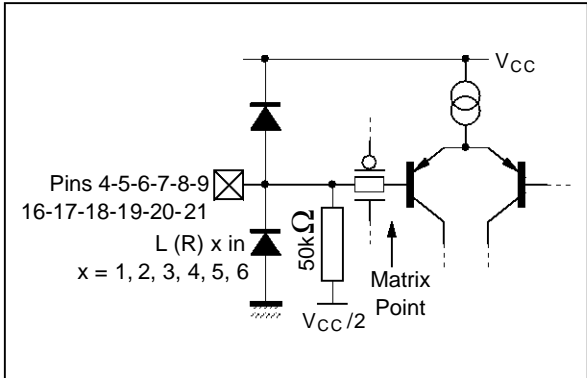


**Figure 4 : Supply Voltage Rejection versus frequency ( $V_{IN} = 500mV_{RMS}$ )**

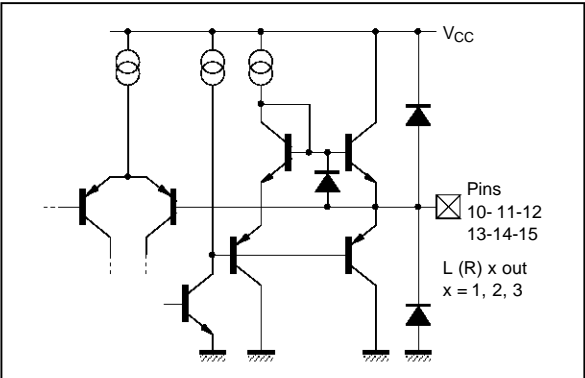


**PIN CONFIGURATIONS (SDIP24 Package)**

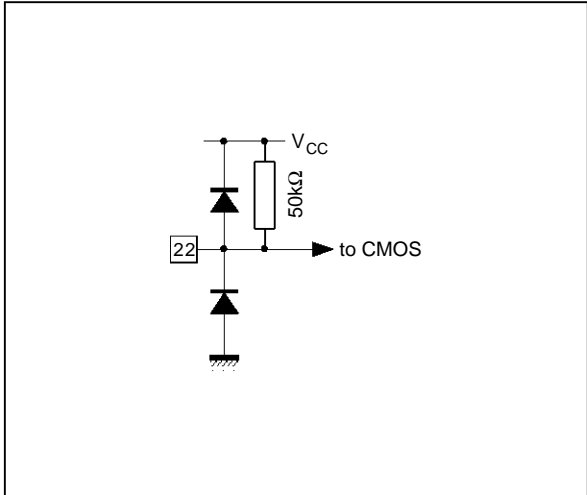
**Figure 5 : Audio IN**



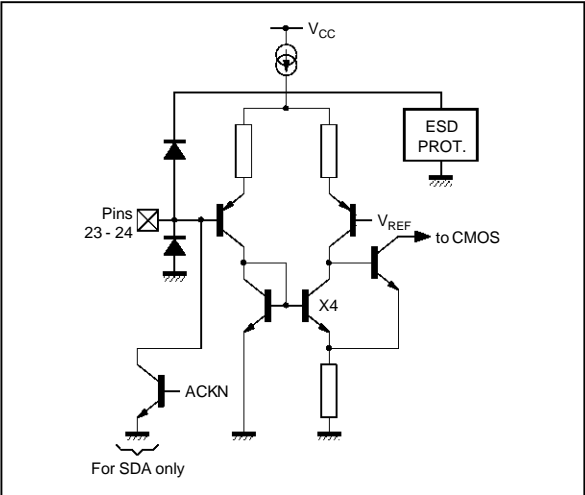
**Figure 6 : Audio OUT**



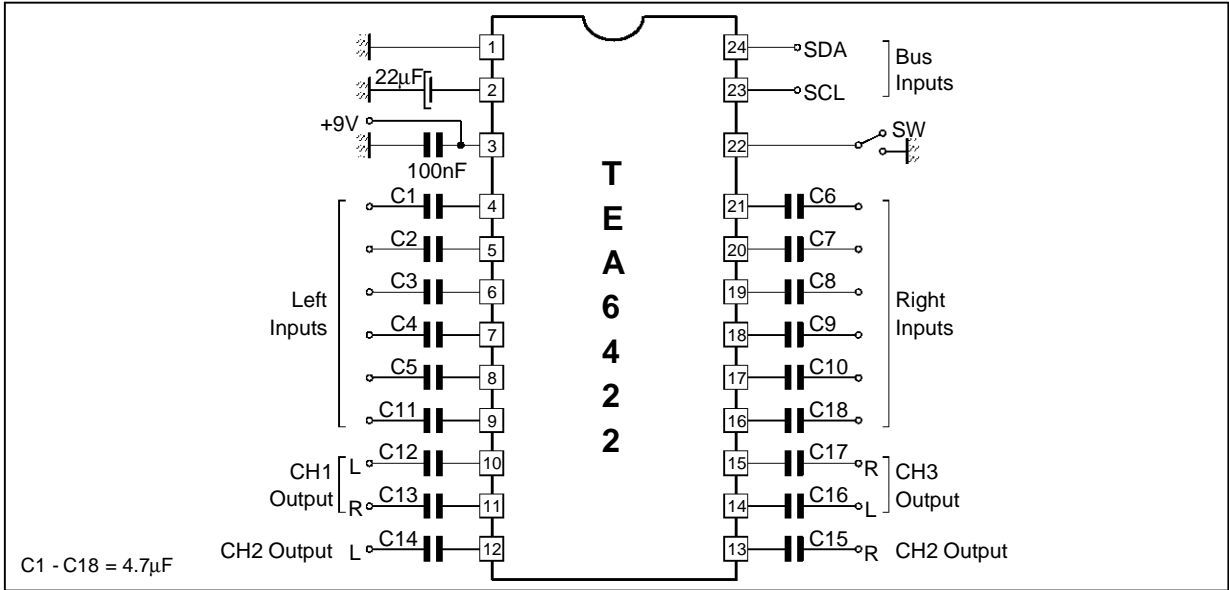
**Figure 7 : ADDR**



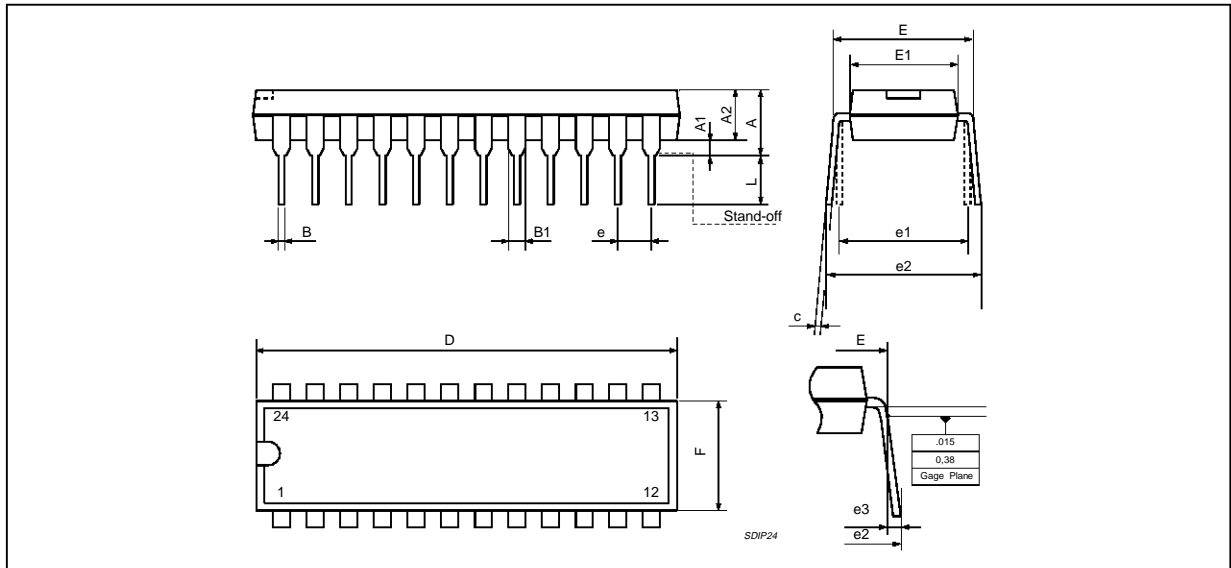
**Figure 8 : Bus Inputs (SDA, SCL)**



**TYPICAL APPLICATION (SDIP24 Package)**



**PACKAGE MECHANICAL DATA**  
24 PINS - PLASTIC SHRINK



PMSDIP24.EPS

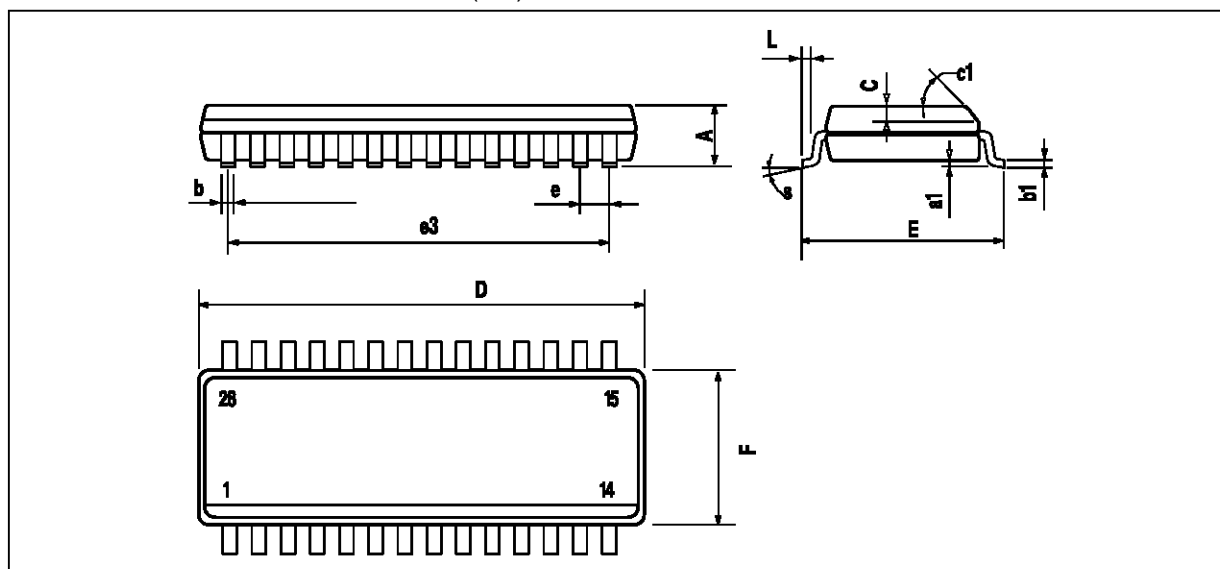
| Dimensions | Millimeters |       |       | Inches |        |        |
|------------|-------------|-------|-------|--------|--------|--------|
|            | Min.        | Typ.  | Max.  | Min.   | Typ.   | Max.   |
| A          |             |       | 5.08  |        |        | 0.20   |
| A1         | 0.51        |       |       | 0.020  |        |        |
| A2         | 3.05        | 3.30  | 4.57  | 0.120  | 0.130  | 0.180  |
| B          | 0.36        | 0.46  | 0.56  | 0.0142 | 0.0181 | 0.0220 |
| B1         | 0.76        | 1.02  | 1.14  | 0.030  | 0.040  | 0.045  |
| C          | 0.23        | 0.25  | 0.38  | 0.0090 | 0.0098 | 0.0150 |
| D          | 22.61       | 22.86 | 23.11 | 0.890  | 0.90   | 0.910  |
| E          | 7.62        |       | 8.64  | 0.30   |        | 0.340  |
| E1         | 6.10        | 6.40  | 6.86  | 0.240  | 0.252  | 0.270  |
| e          |             | 1.778 |       |        | 0.070  |        |
| e1         |             | 7.62  |       |        | 0.30   |        |
| e2         |             |       | 10.92 |        |        | 0.430  |
| e3         |             |       | 1.52  |        |        | 0.060  |
| L          | 2.54        | 3.30  | 3.81  | 0.10   | 0.130  | 0.150  |

SDIP24.TBL



## PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO28-EPS

| Dimensions | Millimeters |       |       | Inches |       |       |
|------------|-------------|-------|-------|--------|-------|-------|
|            | Min.        | Typ.  | Max.  | Min.   | Typ.  | Max.  |
| A          |             |       | 2.65  |        |       | 0.104 |
| a1         | 0.1         |       | 0.3   | 0.004  |       | 0.012 |
| b          | 0.35        |       | 0.49  | 0.014  |       | 0.019 |
| b1         | 0.23        |       | 0.32  | 0.009  |       | 0.013 |
| C          |             | 0.5   |       |        | 0.020 |       |
| c1         | 45° (Typ.)  |       |       |        |       |       |
| D          | 17.7        |       | 18.1  | 0.697  |       | 0.713 |
| E          | 10          |       | 10.65 | 0.394  |       | 0.419 |
| e          |             | 1.27  |       |        | 0.050 |       |
| e3         |             | 16.51 |       |        | 0.65  |       |
| F          | 7.4         |       | 7.6   | 0.291  |       | 0.299 |
| L          | 0.4         |       | 1.27  | 0.016  |       | 0.050 |
| S          | 8° (Max.)   |       |       |        |       |       |

SO28-TBL

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