DATA SHEET

TDA9901
Wideband differential digital controlled variable gain amplifier

Product specification
Supersedes data of 1998 Apr 15
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

Wideband differential digital controlled variable gain amplifier

TDA9901

FEATURES

- 130 MHz, –3 dB small signal bandwidth
- Digitally controlled gain
- TTL/CMOS compatible digital inputs (3.3 or 5 V)
- TTL single ended or differential clock input with PECL compatibility
- 24 dB gain control range
- Five steps of 6 dB plus 6 dB fixed gain
- 30 dB gain maximum
- High impedance differential inputs
- Low impedance differential outputs
- High power supply rejection
- 125 nV/√Hz output voltage noise density at 30 dB gain
- Fast gain settling
- Dual control modes: transparent or latched.

APPLICATIONS

- Linear AGC systems
- IF amplifier in IF conversion systems (e.g. base stations or satellite receivers)
- Instrumentation
- Multi-purpose amplifier
- Driver for differential ADCs (e.g. TDA8768).

GENERAL DESCRIPTION

The TDA9901 is a wideband, low noise amplifier with differential inputs and outputs. The TDA9901 incorporates an AGC function with digital control. The TDA9901 is optimized for fast switching between different gain settings, preserving small phase and amplitude error.

The TDA9901 presents an excellent combination of low noise and good linearity for a wide input frequency range.

The TDA9901 is optimized for processing IF signals in GSM base stations. It is also suited for many other applications as a general purpose digitally controlled variable gain amplifier.

The TDA9901 is able to operate from 4.75 to 5.25 V supply for the analog part and from 3.0 to 5.25 V for the digital part.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
I_{DDA}	analog supply current		–	30	36	mA
I_{DDD}	digital supply current		–	3.0	5.0	mA
G_{dif}	differential gain	minimum gain	5.7	6.11	6.46	dB
		maximum gain	29.3	30.5	31.5	dB
B_{-3dB}	–3 dB small signal bandwidth	$V_{o(dif)(p-p)}$ = 0.125 V; T_{amb} = 25 °C	110	130	–	MHz
P_{tot}	total power dissipation		–	160	216	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9901TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

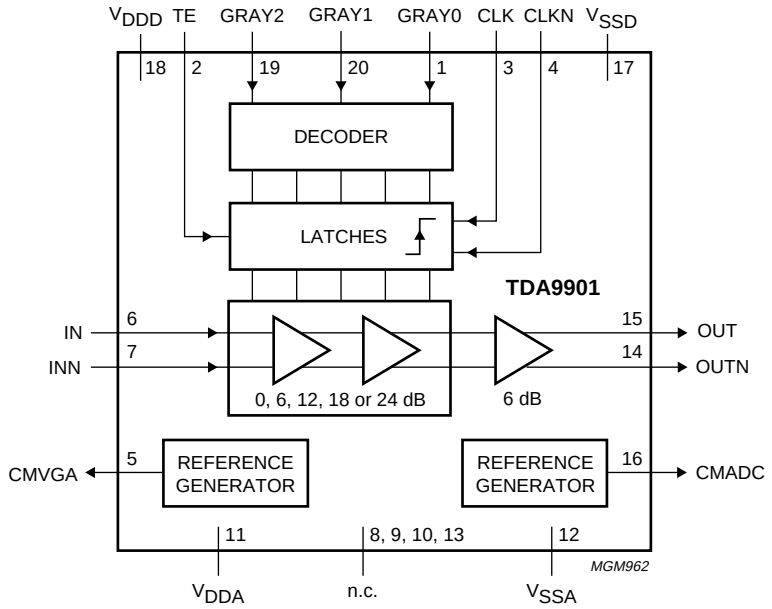


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GRAY0	1	digital control signal bit 0 input (LSB)
TE	2	transparent enable input
CLK	3	clock input for gain control setting
CLKN	4	inverting clock input for gain control setting (active low)
CMVGA	5	regulator output common mode VGA input
IN	6	non-inverting analog input
INN	7	inverting analog input (active low)
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected
OUTN	14	inverting analog output (active low)
OUT	15	non-inverting analog output
CMADC	16	regulator output common mode ADC input
V_{SSD}	17	digital ground
V_{DDD}	18	digital supply voltage
GRAY2	19	digital control signal bit 2 input (MSB)
GRAY1	20	digital control signal bit 1 input

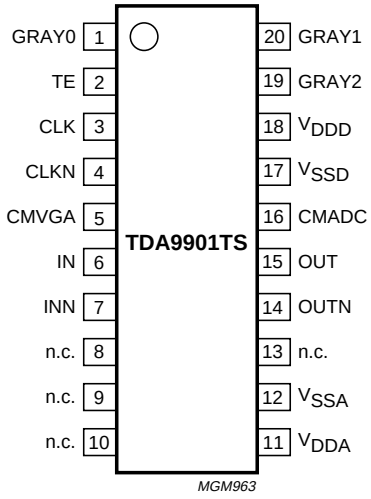


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9901 provides a digitally controlled variable gain function for high-frequency applications.

The TDA9901 can be operated in two different modes, depending on the value at pin TE. When TE is at logic 1, the gain can be instantly controlled when the clock signal is HIGH (transparent mode). The gain is fixed during the LOW period of the clock. When TE is at logic 0 the gain of the TDA9901 is changed at the rising edge of the clock signal.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	–0.3	+7.0	V
V_{DDD}	digital supply voltage	–0.3	+7.0	V
ΔV_{DD}	supply voltage difference between V_{DDA} and V_{DDD}	–1.0	+4.0	V
V_I	input voltage level	–0.3	+7.0	V
I_O	output current	–	10	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	ambient temperature	–40	+85	°C
T_j	junction temperature	–	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W

CHARACTERISTICS

$V_{DDA} = V_{11}$ to V_{12} = 4.75 to 5.25 V; $V_{DDD} = V_{18}$ to V_{17} = 3.0 to 5.25 V; V_{SSA} and V_{SSD} shorted together; T_{amb} = –40 to +85 °C; typical values measured at V_{DDA} = 5.0 V; V_{DDD} = 3.3 V and T_{amb} = 25 °C; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		3.0	3.3	5.25	V
ΔV_{DD}	voltage difference between V_{DDA} and V_{DDD}		–0.2	–	+2.5	V
I_{DDA}	analog supply current		–	30	36	mA
I_{DDD}	digital supply current		–	3.0	5.0	mA
Variable gain amplifier transfer characteristics						
B_{-3dB}	–3 dB small signal bandwidth	$V_{o(dif)(p-p)}$ = 0.125 V; T_{amb} = 25 °C	110	130	–	MHz
$t_{d(g)}$	group delay time	up to f_i = 20 MHz; minimum gain; T_{amb} = 25 °C	–	2.5	–	ns
$\Delta t_{d(g)}$	group delay difference	6 dB gain step; T_{amb} = 25 °C	–	–	300	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{st}	settling time	10 to 90% maximum output transition; $C_{L(max)}$ = 5 pF on each output; T_{amb} = 25 °C	–	–	3.6	ns
G_{step}	gain step size	DC input				
		T_{amb} = 25 °C	5.88	6.09	6.28	dB
		all temperatures	5.6	6.09	6.56	dB
$G_{(min)}$	minimum gain setting	DC input				
		T_{amb} = 25 °C	5.76	6.11	6.40	dB
		all temperatures	5.7	6.11	6.46	dB
$G_{(max)}$	maximum gain setting	DC input				
		T_{amb} = 25 °C	29.9	30.5	30.9	dB
		all temperatures	29.3	30.5	31.5	dB
$\Delta G/\Delta T$	gain stability as a function of temperature	minimum gain	–	–1.0	–	mdB/°C
		maximum gain	–	–7.5	–	mdB/°C
$\lvert\Delta G/\Delta V_{DD}\rvert$	gain stability as a function of power supply	minimum gain	–	15	25	mdB/V
$\Delta V_{i(offset)}$	input offset voltage difference	6 dB gain step	–	0.8	–	mV
F	noise figure	R_S = 100 Ω; f_i = 20 MHz				
		minimum gain	–	29.1	–	dB
		maximum gain	–	9.9	–	dB
$V_{n(o)(eq)}$	equivalent output noise voltage spectral density	R_S = 100 Ω; f_i = 20 MHz; T_{amb} = 25 °C				
		G = 6 dB	–	75	–	nV/√Hz
		G = 12 dB	–	82	–	nV/√Hz
		G = 18 dB	–	97	–	nV/√Hz
		G = 24 dB	–	91	–	nV/√Hz
		G = 30 dB	–	124	–	nV/√Hz
$PSRR_{(VDDA)}$	power supply ripple rejection of V_{DDA}	minimum gain				
		0 to 20 MHz	–	57	–	dB
		20 to 100 MHz	–	39	–	dB
$PSRR_{(VDDD)}$	power supply ripple rejection of V_{DDD}	minimum gain				dB
		0 to 20 MHz	–	67	–	dB
		20 to 100 MHz	–	51	–	dB
CMRR	common mode rejection ratio	0 to 20 MHz	–	75	–	dB
		20 to 150 MHz	–	45	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
$V_{i(max)(p-p)}$	maximum input voltage (peak-to-peak value)	minimum gain	–	1.0	–	V
		maximum gain	–	60.4	–	mV
$V_{i(cm)}$	common mode input voltage		2.0	2.7	V_{DDA} – 1.9	V
I_i	input current	$V_{i(cm)}$ = 2.7 V	–	55	–	µA
R_i	input resistance		10	–	–	kΩ
C_i	input capacitance		–	–	5	pF
Analog outputs; note 2						
$V_{o(max)(p-p)}$	maximum differential output voltage (peak-to-peak value)	maximum gain	2.0	–	–	V
		minimum gain	2.0	–	–	V
$V_{o(cm)}$	common mode output voltage	referenced to V_{DDA}; T_{amb} = 25 °C	V_{DDA} – 2.56	V_{DDA} – 2.42	V_{DDA} – 2.29	V
$\Delta V_{o(cm)}/\Delta T$	common mode output voltage variation with temperature		–	–1.8	–	mV/°C
$SR_{o(se)}$	single-ended output slew rate		–	275	–	V/µs
R_o	output resistance		–	15	26	Ω
C_o	output capacitance		–	3	–	pF
Variable gain amplifier dynamic performance; C_L = 5 pF; R_L = 680 Ω (see Figs 6, 7, 8, 9 and 10)						
HD_2	2nd harmonic distortion	$V_o = V_{o(max)}$				
		f_i = 0.5 MHz	–	–80	–67	dBc
		f_i = 4.43 MHz	–	–77	–67	dBc
		f_i = 12.5 MHz	–	–76	–65	dBc
		f_i = 21.4 MHz	–	–74	–62	dBc
HD_3	3rd harmonic distortion	$V_o = V_{o(max)}$; T_{amb} = 25 °C				
		f_i = 0.5 MHz	–	–64	–60	dBc
		f_i = 4.43 MHz	–	–64	–59	dBc
		f_i = 12.5 MHz	–	–62	–58	dBc
		f_i = 21.4 MHz	–	–61	–57	dBc
$\Delta HD_3/\Delta T$	3rd harmonic distortion variation with temperature	f_i = 21.4 MHz	–	80	–	mdB/°C
Reference voltage output ADC: pin CMADC						
$V_{ref(CMADC)}$	ADC reference output voltage	referenced to V_{DDA}; T_{amb} = 25 °C	V_{DDA} – 1.64	V_{DDA} – 1.45	V_{DDA} – 1.26	V
$R_{o(CMADC)}$	output resistance	T_{amb} = 25 °C	–	17	26	Ω
$\Delta V_{ref(CMADC)}/\Delta T$	ADC reference output voltage variation with temperature		–	–0.11	–	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(CMADC)(max)}$	maximum output current		–	1.0	–	mA
$C_{o(CMADC)}$	output capacitance		–	3	–	pF
Reference voltage output VGA: pin CMVGA						
$V_{ref(CMVGA)}$	VGA reference output voltage	referenced to V_{DDA}; T_{amb} = 25 °C	V_{DDA} – 2.48	V_{DDA} – 2.30	V_{DDA} – 2.17	V
$R_{o(CMVGA)}$	output resistance	T_{amb} = 25 °C	–	9	20	Ω
$\Delta V_{ref(CMVGA)}/\Delta T$	VGA reference output voltage variation with temperature		–	1.75	–	mV/°C
$I_{o(CMVGA)(max)}$	maximum output current		–	1.0	–	mA
$C_{o(CMVGA)}$	output capacitance		–	3	–	pF
Gain switching characteristics (in latched mode); f_{CLK} = 52 MHz; T_{amb} = 25°C; (see Fig.3)						
t_h	input data hold time		2.0	–	–	ns
t_{su}	input data set-up time		3.8	–	–	ns
t_W	input data pulse width		5.8	–	–	ns
t_{PD1}	propagation delay time		–	4.2	5.9	ns
t_{set1}	gain settling time	10 to 90% full scale if ±6 dB gain change; note 3	–	2.6	3.2	ns
Gain switching characteristics (in transparent mode); f_{CLK} = 52 MHz; T_{amb} = 25°C; (see Fig.4)						
t_{PD2}	propagation delay time		–	6.7	9.5	ns
t_{set2}	gain settling time	10 to 90% full scale if ±6 dB gain change; note 4	–	5.4	6.9	ns
Clock timing input: pins CLK and CLKN (see Fig.3)						
$f_{CLK(max)}$	maximum clock frequency		52	–	–	MHz
t_{CPL}	clock LOW pulse width		4.0	–	–	ns
t_{CPH}	clock HIGH pulse width		4.0	–	–	ns
t_r	rise time		–	4	–	ns
t_f	fall time		–	4	–	ns
Digital inputs: pins TE, GRAY0, GRAY1 and GRAY2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		–10	–	+10	µA
I_{IL}	LOW-level input current		–10	–	+10	µA
C_i	input capacitance		–	–	3	pF
Clock inputs in TTL mode						
V_{IL}	LOW-level input voltage	note 5	0	–	0.8	V
V_{IH}	HIGH-level input voltage	note 5	2.0	–	V_{DDD}	V
I_{IH}	HIGH-level input current		15	–	80	µA
I_{IL}	LOW-level input current		–40	–	–10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_i	input capacitance		–	–	2	pF
Clock inputs in differential mode						
V_{IL}	LOW-level input voltage	V_{DDA} = 5.0 V; note 6	3.19	–	3.52	V
V_{IH}	HIGH-level input voltage	V_{DDA} = 5.0 V; note 6	3.83	–	4.12	V
I_{IH}	HIGH-level input current		15	–	80	µA
I_{IL}	LOW-level input current		–40	–	–5	µA
C_i	input capacitance		–	–	2	pF
$\Delta V_{i(CLK)(p-p)}$	differential AC input voltage for switching CLK or CLKN (peak-to-peak value)	DC voltage level = 2.5 V	0.1	–	2.0	V

Notes

1. Due to on-chip regulator behaviour a warm-up time of 1 minute (typical) is recommended for optimal performance.
2. The analog output voltages are positive with respect to AGND.
3. In latching mode (TE = 0), the gain settling is latched at the rising edge of the clock input.
4. In transparent mode, the gain settling is directly controlled by the input data pattern.
5. The circuit may be used with a single TTL clock on CLK or CLKN. The non used clock pin has to be decoupled to ground with a 100 nF capacitance.
6. There are four modes of operation for the clock inputs in non TTL mode:
   a) PECL mode 1: (DC level vary 1 : 1 with V_{DDA}) CLK and CLKN inputs are differential PECL levels.
   b) PECL mode 2: (DC level vary 1 : 1 with V_{DDA}) CLK input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLKN decoupled to V_{SSD} via a 100 nF capacitor.
   c) PECL mode 3: (DC level vary 1 : 1 with V_{DDA}) CLKN input is at PECL level and gain change takes place on the rising edge of the clock input signal when in latched mode. A DC level of 3.65 V has to be applied on CLK decoupled to V_{SSD} via a 100 nF capacitor.
   d) AC driving mode 4: when driving the CLK input directly and with any AC signal of minimum 0.1 V (p-p) and with a DC level of 2.5 V, the gain change takes place on the rising edge of the clock signal. When driving the CLKN input with the same signal, gain change takes place on the falling edge of the clock signal. It is recommended to decouple the CLKN or CLK input to V_{SSD} via a 100 nF capacitor.

Table 1 Input coding

STATE	GREY INPUT DATA CODE			GAIN (dB)
	D2	D1	D0	
0	0	0	0	minimum
1	0	0	1	minimum + 6
2	0	1	1	minimum + 12
3	0	1	0	minimum + 18
4	1	1	0	minimum + 24
Other	–	–	–	minimum + 24

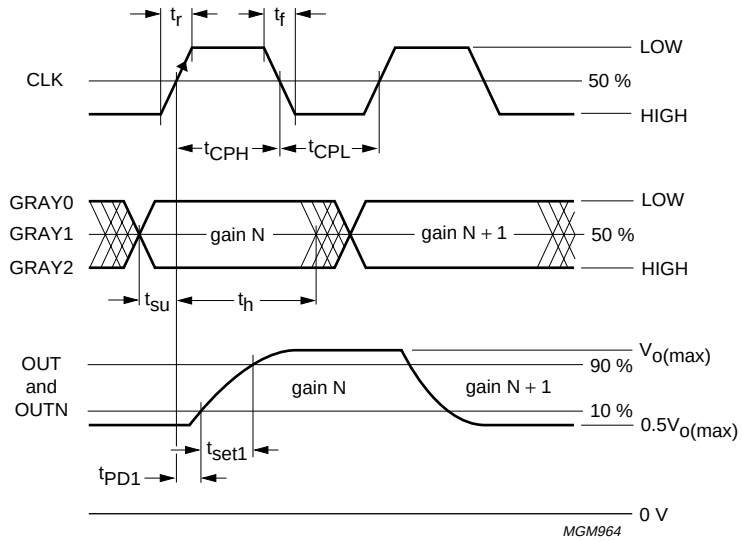


Fig.3 Latched mode timing diagram.

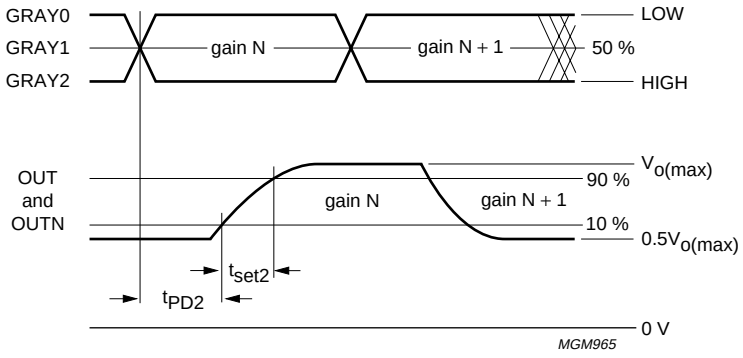
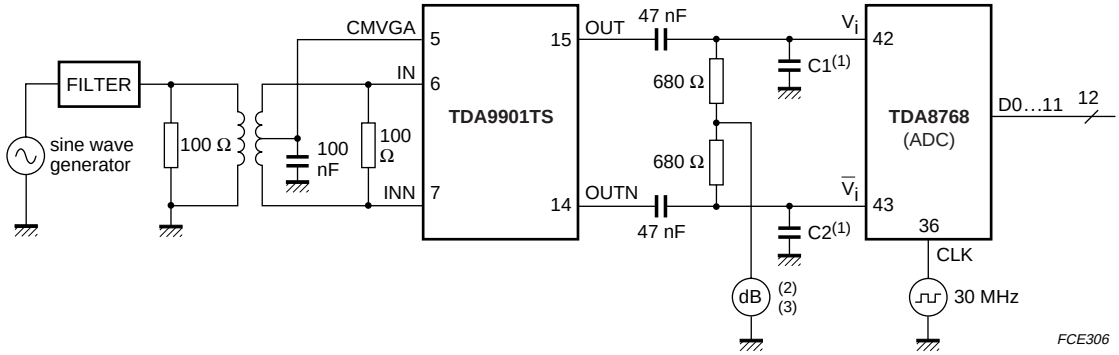


Fig.4 Transparent mode timing diagram with CLK HIGH.

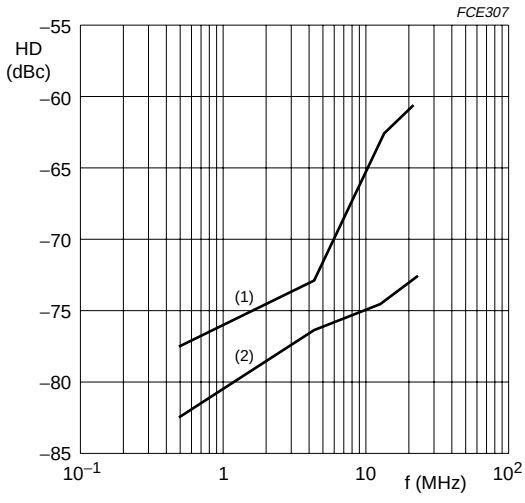


(1) C1 and C2 represent the board line capacitance. They represent about 5 pF with the TDA8768 input capacitance. Special care has to be taken to minimize this load in order to have the best dynamic performance.

(2) The HD_2 and HD_3 of the TDA8768 is lower than that measured on the TDA9901.This measurement method is preferred to conventional methods due to its low contribution to the HD_2.

(3) The chain measurement shows the harmonic distortion of the TDA9901 as the measurement from TDA8768 is negligible.

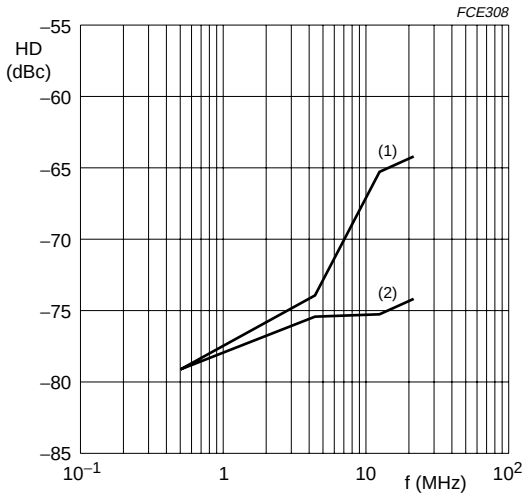
Fig.5 Dynamic distortion measurement diagram.



(1) HD_3
(2) HD_2

Typical condition; 2 V (p-p) differential output.

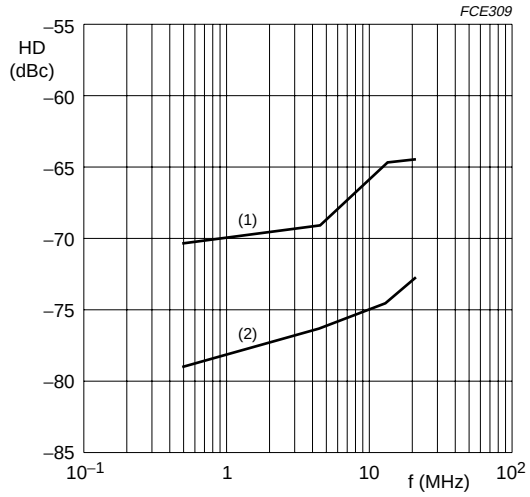
Fig.6 Harmonic distortion as a function of frequency for minimum gain.



(1) HD_3
(2) HD_2

Typical condition; 2 V (p-p) differential output.

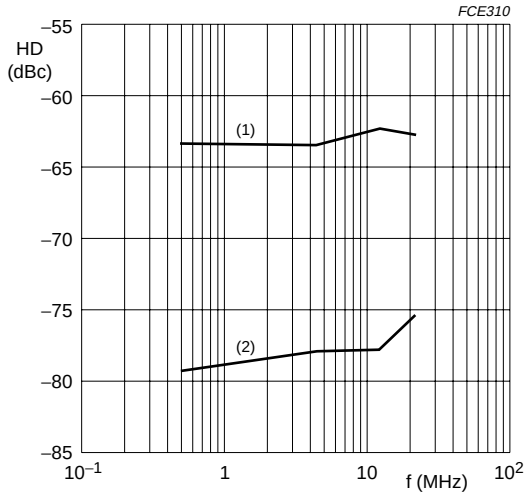
Fig.7 Harmonic distortion as a function of frequency for minimum gain plus 6 dB.



(1) HD_3
(2) HD_2

Typical condition; 2 V (p-p) differential output.

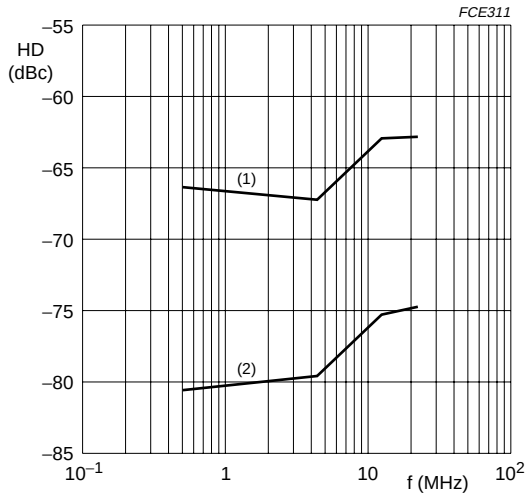
Fig.8 Harmonic distortion as a function of frequency for minimum gain plus 12 dB.



(1) HD_3
(2) HD_2

Typical condition; 2 V (p-p) differential output.

Fig.9 Harmonic distortion as a function of frequency for minimum gain plus 18 dB.

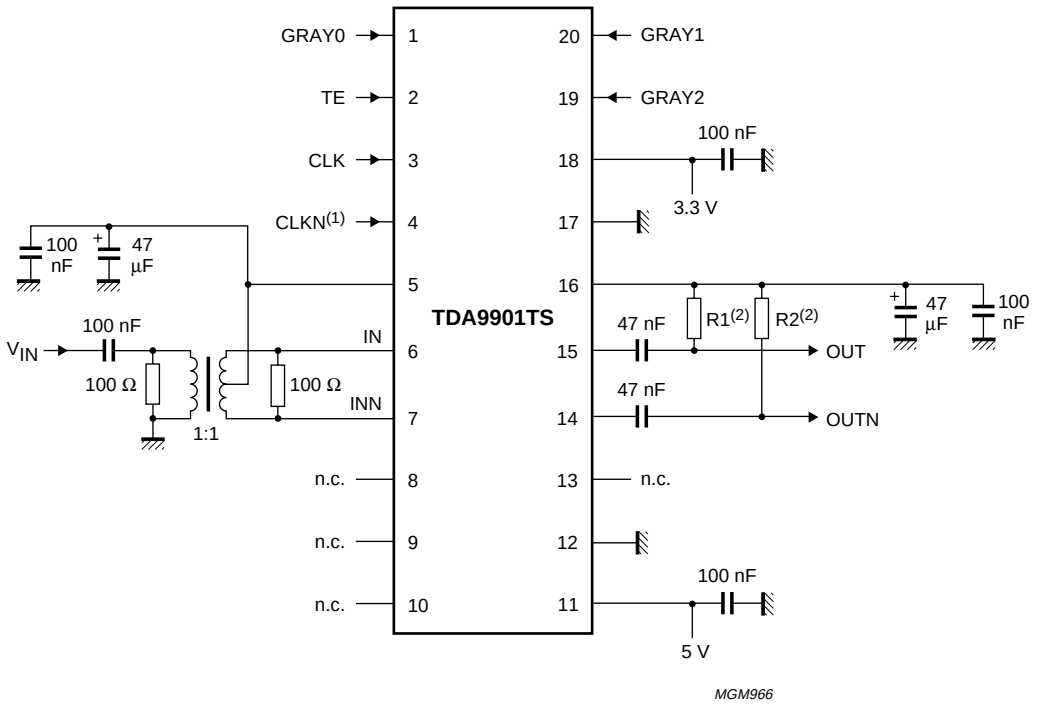


(1) HD_3
(2) HD_2

Typical condition; 2 V (p-p) differential output.

Fig.10 Harmonic distortion as a function of frequency for minimum gain plus 24 dB.

APPLICATION INFORMATION

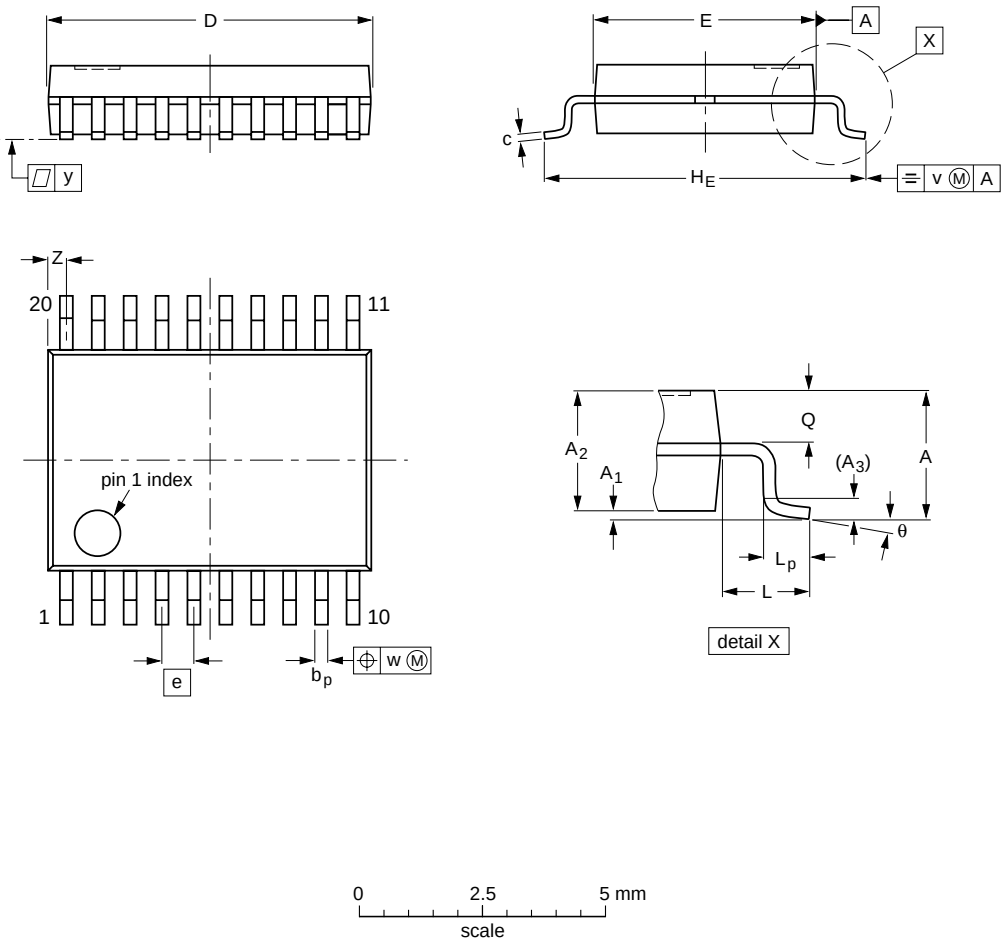


(1) Single-ended clock signal can be applied if required.
(2) R1 and R2 should be at least 680 Ω.

Fig.11 Application diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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