DATA SHEET

TDA9850
I²C-bus controlled BTSC stereo/SAP decoder

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

I²C-bus controlled BTSC stereo/SAP decoder TDA9850

FEATURES

- Quasi alignment-free application due to automatic adjustment of channel separation via I²C-bus
- Dbx noise reduction circuit
- Dbx decoded stereo, Second Audio Program (SAP) or mono selectable at the AF outputs
- Additional SAP output without dbx, including de-emphasis
- High integration level with automatically tuned integrated filters
- Input level adjustment I²C-bus controlled
- Alignment-free SAP processing
- Stereo pilot PLL circuit with ceramic resonator, automatic adjustment procedure for stereo channel separation, two pilot thresholds selectable via I²C-bus
- Automatic pilot cancellation
- Composite input noise detector with I²C-bus selectable thresholds for stereo and SAP off
- I²C-bus transceiver.

GENERAL DESCRIPTION

The TDA9850 is a bipolar-integrated BTSC stereo/SAP decoder (I²C-bus controlled) for application in TV sets, VCRs and multimedia.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.5	9	9.5	V
I_{CC}	supply current		–	58	75	mA
$V_{comp(rms)}$	input signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	250	–	mV
$V_{oR(rms)}$; $V_{oL(rms)}$	output signal voltage (RMS value)	100% modulation L + R; f_i = 300 Hz	–	500	–	mV
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
α_{cs}	stereo channel separation	f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz	–	0.2	–	%
S/N	signal-to-noise ratio	500 mV (RMS) mono output signal				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9850	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TDA9850T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

License information

A license is required for the use of this product. For further information, please contact:

COMPANY	BRANCH	ADDRESS
THAT Corporation	Licensing Operations	734 Forest St. Marlborough, MA 01752 USA Tel.: (508) 229-2500 Fax: (508) 229-2590
	Tokyo Office	405 Palm House, 1-20-2 Honmachi Shibuya-ku, Tokyo 151 Japan Tel.: (03) 3378-0915 Fax: (03) 3374-5191

BLOCK DIAGRAM

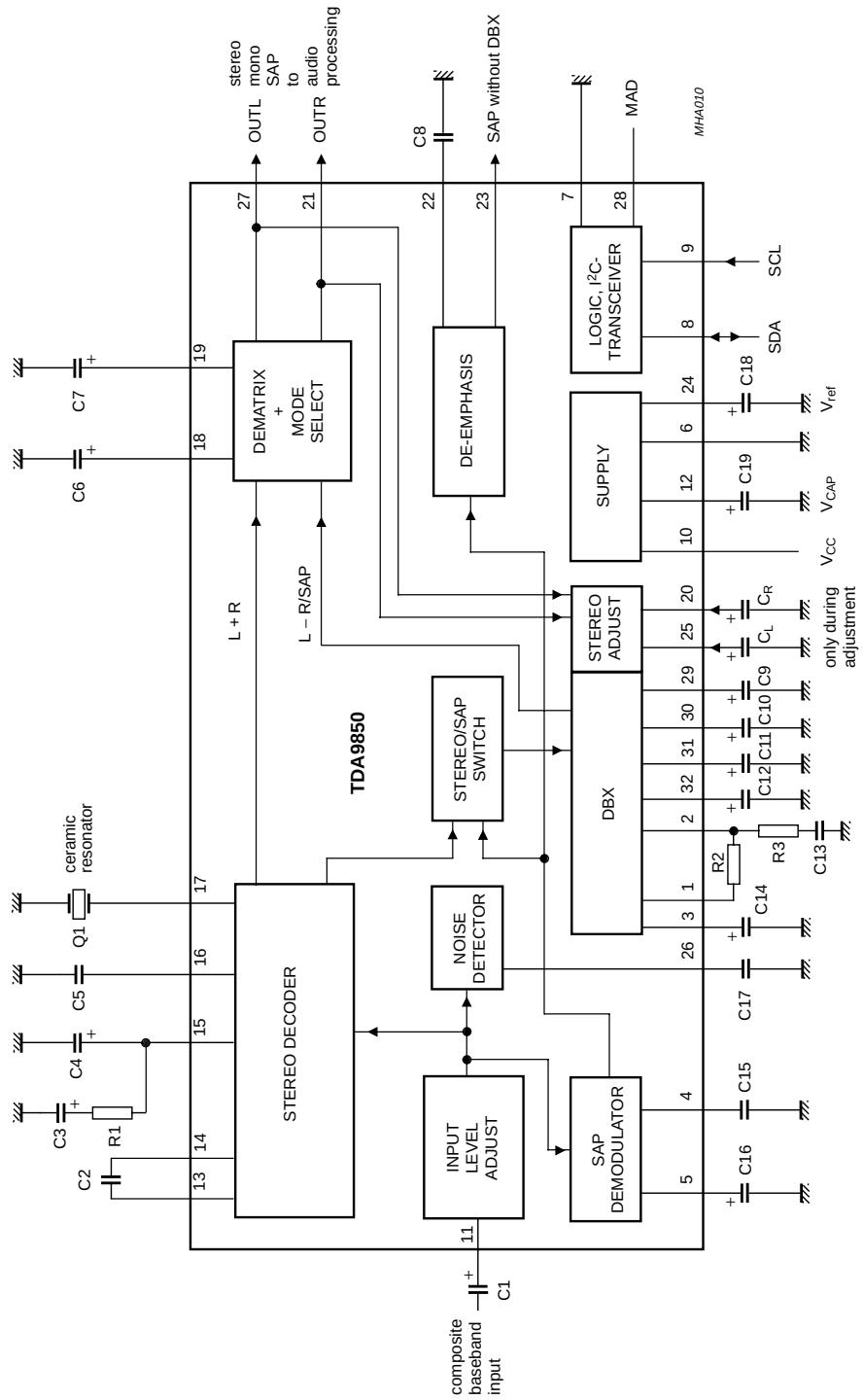


Fig.1 Block, application and test diagram.

COMPONENT LIST

Electrolytic capacitors ±20%; foil capacitors ±10%; resistors ±5%; unless otherwise specified; see Fig.1.

COMPONENT	VALUE	TYPE	REMARK
C1	10 µF	electrolytic	63 V
C2	470 nF	foil	
C3	4.7 µF	electrolytic	63 V
C4	220 nF	foil	
C5	10 µF	electrolytic	63 V; I_{leak} < 1.5 µA
C6	4.7 µF	electrolytic	63 V
C7	4.7 µF	electrolytic	63 V
C8	15 nF	foil	
C9	10 µF	electrolytic	63 V ±10%
C10	10 µF	electrolytic	63 V ±10%
C11	1 µF	electrolytic	63 V
C12	1 µF	electrolytic	63 V
C13	47 nF	foil	±5%
C14	10 µF	electrolytic	63 V
C15	100 nF	foil	
C16	4.7 µF	electrolytic	63 V
C17	100 nF	foil	
C18	100 µF	electrolytic	16 V
C19	100 µF	electrolytic	16 V
CR	2.2 µF	electrolytic	63 V
CL	2.2 µF	electrolytic	63 V
R1	2.2 kΩ		
R2	8.2 kΩ		±2%
R3	160 Ω		±2%
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

PINNING

SYMBOL	PIN	DESCRIPTION
VEO	1	variable emphasis output for dbx
VEI	2	variable emphasis input for dbx
C_{NR}	3	capacitor noise reduction for dbx
C_M	4	capacitor mute for SAP
C_{DEC}	5	capacitor DC-decoupling for SAP
AGND	6	analog ground
DGND	7	digital ground
SDA	8	serial data input/output
SCL	9	serial clock input
V_{CC}	10	supply voltage (+9 V)
COMP	11	composite input signal
V_{CAP}	12	capacitor for electronic filtering of supply
C_{P1}	13	capacitor for pilot detector
C_{P2}	14	capacitor for pilot detector
C_{PH}	15	capacitor for phase detector
C_{ADJ}	16	capacitor for filter adjustment
CER	17	ceramic resonator
C_{MO}	18	capacitor DC-decoupling mono
C_{SS}	19	capacitor DC-decoupling stereo/SAP
C_R	20	adjustment capacitor, right channel
OUTR	21	output, right channel
C_{SDE}	22	capacitor SAP de-emphasis
SAP	23	SAP output
V_{ref}	24	reference voltage $0.5 \times (V_{CC} - 1.5\ V)$
C_L	25	adjustment capacitor, left channel
C_{ND}	26	noise detector capacitor
OUTL	27	output, left channel
MAD	28	programmable address bit
C_{TW}	29	capacitor timing wideband for dbx
C_{TS}	30	capacitor timing spectral for dbx
C_W	31	capacitor wideband for dbx
C_S	32	capacitor spectral for dbx

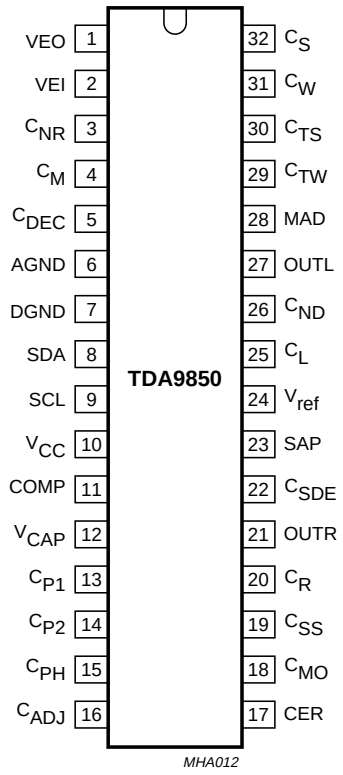


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Input level adjustment

The composite input signal is fed to the input level adjustment stage. The control range is from −3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 4 of Tables 5 and 6 and the level adjust setting of Table 10 allows an optimum signal adjustment during the set alignment. The maximum input signal voltage is 2 V (RMS).

Stereo decoder

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L − R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation is adjusted by an automatic procedure to be performed during set production. For a detailed description see Section “Adjustment procedure”. The stereo identification can be read by the I²C-bus (see Table 2). Two different pilot thresholds (data STS = 1; STS = 0) can be selected via the I²C-bus (see Table 14).

SAP demodulator

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a $5f_H$ band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes an internal field strength detector that mutes the SAP output in the event of insufficient signal conditions. The SAP identification signal can be read by the I²C-bus (see Table 2).

Noise detector

The composite input noise increases with decreasing antenna signal. This makes it necessary to switch stereo or SAP off at certain thresholds. These thresholds can be set via the I²C-bus. With ST0 to ST3 (see Table 6) the stereo threshold can be selected and with SP0 to SP3 the SAP threshold. A hysteresis can be achieved via software by making the threshold dependent of the identification bits STP and SAPP (see Table 2).

Mode selection

The stereo/SAP switch feeds either the L − R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/switching circuit. Table 8 shows the different switch modes provided at the output pins OUTR and OUTL.

dbx decoder

The dbx circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73 μs fixed de-emphasis circuit to the dematrix block.

SAP output

Independent of the stereo/SAP switch, the SAP signal is also available at pin SAP. At SAP, the SAP signal is not dbx decoded. The capacitor at SDE provides a recommended de-emphasis (150 μs) at SAP.

Integrated filters

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transconductor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

Adjustment procedure

Composite input level adjustment

Feed in from FM demodulator the composite signal with 100% modulation (25 kHz deviation) L + R; f_i = 300 Hz. Set input level control via I²C-bus monitoring OUTL or OUTR (500 mV ±20 mV). Store the setting in a non-volatile memory.

Automatic adjustment procedure

- Connect 2.2 μF capacitors from ACR and ACL to ground.
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel.
- Mode selection setting bits: STEREO = 1, SAP = 0 (see Table 8).
- Start adjustment by transmission ADJ = 1 in register ALI3. The decoder will align itself.
- After 1 second minimum stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I²C-bus read operation from ALR1 and ALR2 (see Chapter "I²C-bus protocol") and store it in a non-volatile memory. The alignment procedure overwrites the previous data stored in ALI1 and ALI2.
- The capacitors from ACR and ACL may be disconnected after alignment.

Manual adjustment

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

After every power-on, the alignment data and the input level adjustment data must be loaded from the non-volatile memory.

Timing current for release rate

Due to possible internal and external spreading, the timing current can be adjusted via I²C-bus, see Table 9, as recommended by dbx.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		0	10	V
V_{VCAP}	voltage of V_{CAP} to GND		0	V_{CC}	V
V_{VEO}	voltage of VEO to GND		0	$\frac{1}{2}V_{CC}$	V
V_{SDA}	voltage of SDA to GND		0	8.5	V
V_{SCL}	voltage of SCL to GND		0	8.5	V
V_n	voltage of all other pins to GND	$V_{CC} \geq 8.5$ V	0	8.5	V
		$V_{CC} < 8.5$ V	0	V_{CC}	V
T_{amb}	operating ambient temperature	$T_j < 125$ °C	−20	+70	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	HBM; note 1			

Note

1. Human Body Model (HBM): C = 100 pF; R = 1.5 kΩ; V = 2 kV; charge device model: C = 200 pF; R = 0 Ω; V = 300 V.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT232-1	55	K/W
	SOT287-1	68	K/W

REQUIREMENTS FOR THE COMPOSITE INPUT SIGNAL TO ENSURE CORRECT SYSTEM PERFORMANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$COMP_{L+R(rms)}$	composite input level for 100% modulation L + R (25 kHz deviation); RMS value; f_i = 300 Hz	measured at COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T_{amb} = –20 to +70 °C; aging; power supply influence	–0.5	–	+0.5	dB
Z_{source}	source impedance	note 1	–	low-ohmic	5	kΩ
f_{lf}	low frequency roll-off	25 kHz deviation L + R; –2 dB	–	–	5	Hz
f_{hf}	high frequency roll-off	25 kHz deviation L + R; –2 dB	100	–	–	kHz
$THD_{L,R}$	total harmonic distortion L + R	f_i = 1 kHz; 25 kHz deviation	–	–	0.5	%
		f_i = 1 kHz; 125 kHz deviation; note 2	–	–	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f_i = 1 kHz; 75 μs de-emphasis				
	critical picture modulation; note 3		44	–	–	dB
	with sync only		54	–	–	dB
α_{SB}	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f_i = 1 kHz; side band: SAP carrier frequency ±1 kHz	40	–	–	dB
α_{SP}	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n × f_H; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference				
	n = 1, 4, 5, 6		35	–	–	dB
	n = 2, 3		26	–	–	dB

Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z_O and the composite input impedance (see Chapter “Characteristics”; row head “Input level adjustment control”) must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).
3. For example colour bar or flat field white; 100% video modulation.

CHARACTERISTICS

All voltages are measured relative to GND; V_{CC} = 9 V; R_s = 600 Ω; R_L = 10 kΩ; AC-coupled; C_L = 2.5 nF; f_i = 1 kHz; T_{amb} = +25 °C; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		8.5	9	9.5	V
$V_{ripple(p-p)}$	allowed supply voltage ripple (peak-to-peak value)	f_i = 50 Hz to 100 kHz	–	–	100	mV
I_{CC}	supply current		–	58	75	mA
V_{ref}	internal reference voltage at pin V_{ref}		–	3.7	–	V
α_{ct}	crosstalk between bus inputs and signal outputs	notes 1 and 2	–	110	–	dB
Input level adjustment control						
G_{LA}	input level adjustment control		–3.5	–	+4.0	dB
G_{step}	step resolution		–	0.5	–	dB
$V_{i(rms)}$	maximum input voltage level (RMS value)		2	–	–	V
Z_i	input impedance		29.5	35	40.5	kΩ
Stereo decoder						
MPX_{L+R}	input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring OUTL or OUTR	–	250	–	mV
MPX_{L-R}	input voltage level for 100% modulation L – R; 50 kHz deviation (peak value)		–	707	–	mV
$MPX_{(max)}$	maximum headroom for L + R, L, R	f_{mod} < 15 kHz; THD < 15%	9	–	–	dB
MPX_{pilot}	nominal stereo pilot voltage level (RMS value)		–	50	–	mV
$ST_{on(rms)}$	pilot threshold voltage stereo on (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
$ST_{off(rms)}$	pilot threshold voltage stereo off (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
Hys	hysteresis		–	2.5	–	dB
OUT_{L+R}	output voltage level for 100% modulation L + R at OUTL, OUTR	input level adjusted via I²C-bus (L + R; f_i = 300 Hz); monitoring OUTL or OUTR	480	500	520	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cs}	stereo channel separation L/R	aligned with dual tone 14% modulation for each channel; see Section "Adjustment procedure"				
		f_L = 300 Hz; f_R = 3 kHz	25	35	–	dB
		f_L = 300 Hz; f_R = 8 kHz	20	30	–	dB
		f_L = 300 Hz; f_R = 10 kHz	15	25	–	dB
$f_{L, R}$	L, R frequency response	14% modulation; f_{ref} = 300 Hz L or R				
		f_i = 50 Hz to 10 kHz	–3	–	–	dB
		f_i = 12 kHz	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R	modulation L or R 1% to 100%; f_i = 1 kHz	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal	50	60	–	dB
Stereo decoder, oscillator (VCXO); note 3						
f_o	nominal VCXO output frequency ($32f_H$)	with nominal ceramic resonator	–	503.5	–	kHz
f_{of}	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
Δf_H	capture range frequency (nominal pilot)		±190	±265	–	Hz
SAP demodulator; note 4						
$SAP_{i(rms)}$	nominal SAP carrier input voltage level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
$SAP_{on(rms)}$	threshold voltage SAP on (RMS value)		–	–	68	mV
$SAP_{off(rms)}$	threshold voltage SAP off (RMS value)		28	–	–	mV
SAP_{hys}	hysteresis		–	2	–	dB
SAP_{LEV}	SAP output voltage level at OUTL, OUTR	mode selector in position SAP/SAP; f_{mod} = 300 Hz; 100% modulation	–	500	–	mV
f_{res}	frequency response	14% modulation; 50 Hz to 8 kHz; f_{ref} = 300 Hz	–3	–	–	dB
THD	total harmonic distortion	f_i = 1 kHz	–	0.5	2.0	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SAP output						
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		–	$0.5V_{CC}$–1.5	–	V
R_L	output load resistance (AC-coupled)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
$V_{o(rms)}$	nominal output voltage (RMS value)	150 μs de-emphasis	see Fig.3			
Outputs OUTL and OUTR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
$HEAD_o$	output headroom		9	–	–	dB
Z_o	output impedance		–	80	120	Ω
V_O	DC output voltage		$0.45V_{CC}$–1.5	$0.5V_{CC}$–1.5	$0.55V_{CC}$–1.5	V
R_L	output load resistance (AC-coupled)		5	–	–	kΩ
C_L	output load capacitance		–	–	2.5	nF
α_{ct}	crosstalk L, R into SAP	100% modulation; f_i = 1 kHz; L or R; mode selector switched to SAP/SAP	50	75	–	dB
	crosstalk SAP into L, R	100% modulation; f_i = 1 kHz; SAP; mode selector switched to stereo	50	70	–	dB
ΔV_{ST-SAP}	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
Dbx noise reduction circuit						
t_{adj}	stereo adjustment time	see Section “Adjustment procedure”	–	–	1	s
I_s	nominal timing current for nominal release rate of spectral RMS detector	I_s can be measured at pin C_{TS} via current meter connected to $\frac{1}{2}V_{CC}$ + 0.25 V	–	24	–	μA
ΔI_s	spread of timing current		–15	–	+15	%
$I_{s\ range}$	timing current range	7 steps via I²C-bus	–	±30	–	%
I_t	timing current for release rate of wideband RMS detector		–	$\frac{1}{3}I_s$	–	μA
Rel_{rate}	nominal RMS detector release rate	nominal timing current and external capacitor values				
	wideband		–	125	–	dB/s
	spectral		–	381	–	dB/s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Noise detector						
f_0	noise band-pass centre frequency	composite input level 100 mV (RMS)	–	185	–	kHz
Q	quality factor		–	6	–	–
Ster1, SAP1	lowest noise threshold for stereo off respectively SAP off (RMS value; see Tables 11 and 12)	f_i = 185 kHz	17	24	34	mV
Ster16, SAP16	highest noise threshold for stereo off respectively SAP off (RMS value)	f_i = 185 kHz	210	290	400	mV
ΔSter, ΔSAP	noise threshold step width	f_i = 185 kHz	0	1.5	3	dB
Power-on reset; note 5						
$V_{RESET(STA)}$	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
$V_{RESET(END)}$	end of reset voltage	increasing supply voltage	5.2	6	6.8	V
Digital part (I²C-bus pins); note 6						
V_{IH}	HIGH level input voltage		3	–	8.5	V
V_{IL}	LOW level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH level input current		–10	–	+10	μA
I_{IL}	LOW level input current		–10	–	+10	μA
V_{OL}	LOW level output voltage	I_{IL} = 3 mA	–	–	0.4	V

Notes to the characteristics

1. Crosstalk: $20 \log \frac{V_{bus(p-p)}}{V_{o(rms)}}$
2. The transmission contains:
   a) Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
   b) Clock frequency = 50 kHz
   c) Repetition burst rate = 400 Hz
   d) Maximum bus signal amplitude = 5 V (p-p).
3. The oscillator is designed to operate together with MURATA resonator CSB503F58 or CSB503JF958 as SMD. Change of the resonator supplier is possible, but the resonator specification must be close to the specified ones.
4. The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
5. When reset is active the SMU-bit (SAP mute) and the LMU-bit (OUTL, OUTR mute) is set and the I²C-bus receiver is in the reset position.
6. The AC characteristics are in accordance with the I²C-bus specification for standard mode (clock frequency maximum 100 kHz). A higher frequency, up to 280 kHz, can be used if all clock and data times are interpolated between standard mode (100 kHz) and fast mode (400 kHz) in accordance with the I²C-bus specification. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011).

I²C-BUS PROTOCOL

I²C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	DATA	MA	DATA	P

Table 1 Explanation of I²C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS (MAD)	1011011 pin MAD not connected
Pin programmable SLAVE ADDRESS	1011010 pin MAD connected to ground
R/$\overline{W}$	1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
MA	acknowledge; generated by the master
P	STOP condition; generated by the master

Table 2 Definition of the transmitted bytes after read condition

FUNCTION	BYTE	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20

Table 3 Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1X to A2X	stereo alignment read data
A1X	for wideband expander
A2X	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word, ALR1, then the slave transmits the next data word ALR2. The master next generates an acknowledge, then slave begins transmitting the first data word ALR1, and so on until the master generates no acknowledge and transmits a STOP condition.

I²C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/$\overline{W}$	A	SUBADDRESS	A	DATA	A	P

Table 4 Explanation of I²C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS (MAD)	101 101 1 pin MAD not connected
Pin programmable SLAVE ADDRESS	101 101 0 pin MAD connected to ground
R/$\overline{W}$	0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

Table 5 Subaddress second byte after MAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Control 1	CON1	0	0	0	0	0	1	0	0
Control 2	CON2	0	0	0	0	0	1	0	1
Control 3	CON3	0	0	0	0	0	1	1	0
Control 4	CON4	0	0	0	0	0	1	1	1
Alignment 1	ALI1	0	0	0	0	1	0	0	0
Alignment 2	ALI2	0	0	0	0	1	0	0	1
Alignment 3	ALI3	0	0	0	0	1	0	1	0

Table 6 Definition of third byte, third byte after MAD and SAD

FUNCTION	REGISTER	MSB							LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Control 1	CON1	0	0	0	0	ST3	ST2	ST1	ST0
Control 2	CON2	0	0	0	0	SP3	SP2	SP1	SP0
Control 3	CON3	SAP	STEREO	0	SMU	LMU	0	0	0
Control 4	CON4	0	0	0	0	L3	L2	L1	L0
Alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10
Alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20
Alignment 3	ALI3	ADJ	0	0	0	0	TC2	TC1	TC0

Table 7 Function of the bits in Table 6

BITS	FUNCTION
ST0 to ST3	noise threshold for stereo
SP0 to SP3	noise threshold for SAP
STEREO, SAP	mode selection
LMU	mute control OUTL and OUTR
SMU	mute control SAP
L0 to L3	input level adjustment
ADJ	stereo adjustment on/off
A1X to A2X	stereo alignment data
A1X	for wideband expander
A2X	for spectral expander
TC0 to TC2	timing current alignment data
STS	stereo level switch

Table 8 Mode selection

FUNCTION MODE AT		DATA TRANSMISSION STATUS INTERNAL SWITCH, READABLE BITS: STP, SAPP	SETTING BITS	
OUTL	OUTR		STEREO	SAP
SAP	SAP	SAP received	1	1
Mute	mute	no SAP received	1	1
Left	right	STEREO received	1	0
Mono	mono	no STEREO received	1	0
Mono	SAP	SAP received	0	1
Mono	mute	no SAP received	0	1
Mono	mono	independent	0	0

Table 9 Timing current setting

FUNCTION I_S RANGE	DATA		
	TC2	TC1	TC0
+30%	1	0	0
+20%	1	0	1
+10%	1	1	1
Nominal	0	1	1
–10%	0	1	0
–20%	0	0	1
–30%	0	0	0

Table 10 Level adjust setting

G_L (dB)	DATA			
	L3	L2	L1	L0
+4.0	1	1	1	1
+3.5	1	1	1	0
+3.0	1	1	0	1
+2.5	1	1	0	0
+2.0	1	0	1	1
+1.5	1	0	1	0
+1.0	1	0	0	1
+0.5	1	0	0	0
0.0	0	1	1	1
−0.5	0	1	1	0
−1.0	0	1	0	1
−1.5	0	1	0	0
−2.0	0	0	1	1
−2.5	0	0	1	0
−3.0	0	0	0	1
−3.5	0	0	0	0

Table 11 Stereo noise threshold (Ster)

THRESHOLD	DATA			
	ST3	ST2	ST1	ST0
Ster1	0	0	0	0
Ster2	0	0	0	1
Ster3	0	0	1	0
Ster4	0	0	1	1
Ster5	0	1	0	0
Ster6	0	1	0	1
Ster7	0	1	1	0
Ster8	0	1	1	1
Ster9	1	0	0	0
Ster10	1	0	0	1
Ster11	1	0	1	0
Ster12	1	0	1	1
Ster13	1	1	0	0
Ster14	1	1	0	1
Ster15	1	1	1	0
Ster16	1	1	1	1

Table 12 SAP noise threshold (SAP)

THRESHOLD	DATA			
	SP3	SP2	SP1	SP0
SAP1	0	0	0	0
SAP2	0	0	0	1
SAP3	0	0	1	0
SAP4	0	0	1	1
SAP5	0	1	0	0
SAP6	0	1	0	1
SAP7	0	1	1	0
SAP8	0	1	1	1
SAP9	1	0	0	0
SAP10	1	0	0	1
SAP11	1	0	1	0
SAP12	1	0	1	1
SAP13	1	1	0	0
SAP14	1	1	0	1
SAP15	1	1	1	0
SAP16	1	1	1	1

Table 13 ADJ bit setting

FUNCTION	DATA
Stereo decoder operation mode	0
Auto adjustment of channel separation	1

Table 14 STS bit setting (pilot threshold stereo on)

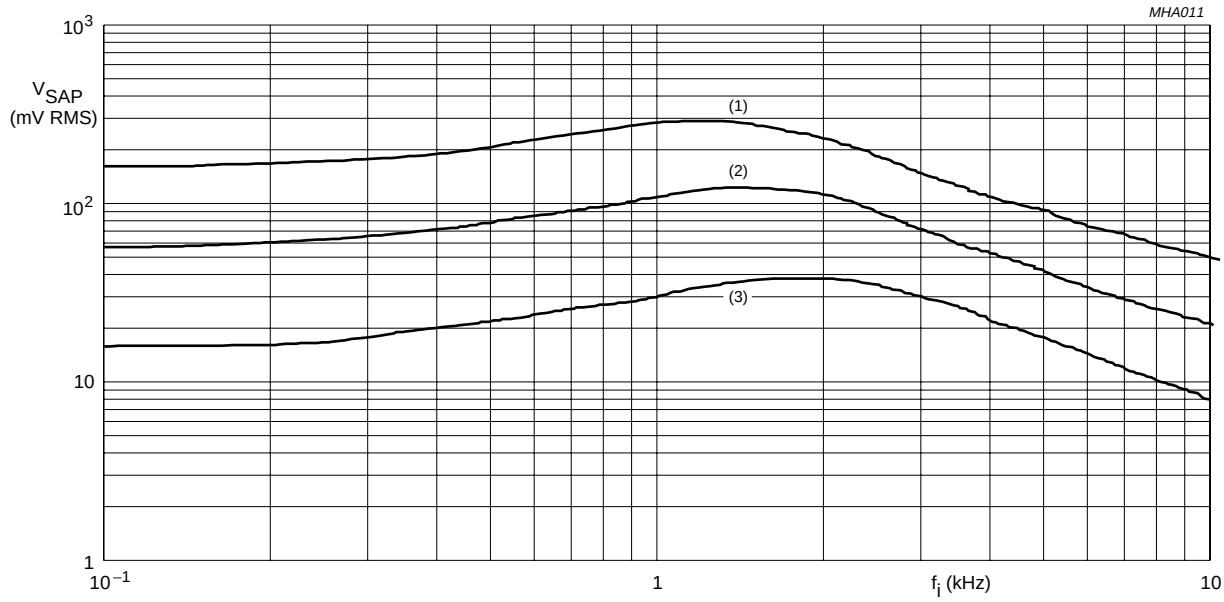
FUNCTION	DATA
$ST_{on} \leq 35$ mV	1
$ST_{on} \leq 30$ mV	0

Table 15 Mute setting

FUNCTION	DATA LMU	FUNCTION	DATA SMU
Forced mute at OUTR, OUTL	1	forced mute at SAP	1
No forced mute at OUTR, OUTL	0	no forced mute at SAP	0

Table 16 Alignment data for expander in read register ALR1 and ALR2 and in write register ALI1 and ALI2

FUNCTION	DATA				
	D4 AX4	**D3 AX3**	**D2 AX2**	**D1 AX1**	**D0 AX0**
Gain increase	1	1	1	1	1
	1	1	1	1	0
	1	1	1	0	1
	1	1	1	0	0
	1	1	0	1	1
	1	1	0	1	0
	1	1	0	0	1
	1	1	0	0	0
	1	0	1	1	1
	1	0	1	1	0
	1	0	1	0	1
	1	0	1	0	0
	1	0	0	1	1
	1	0	0	1	0
	1	0	0	0	1
Nominal gain	1	0	0	0	0
	0	1	1	1	1
Gain decrease	0	1	1	1	0
	0	1	1	0	1
	0	1	1	0	0
	0	1	0	1	1
	0	1	0	1	0
	0	1	0	0	1
	0	1	0	0	0
	0	0	1	1	1
	0	0	1	1	0
	0	0	1	0	1
	0	0	1	0	0
	0	0	0	1	1
	0	0	0	1	0
	0	0	0	0	1
	0	0	0	0	0



150 μs de-emphasis.
(1) 100% modulation.
(2) 14% modulation.
(3) 1% modulation.

Fig.3 Voltage at SAP output.

INTERNAL PIN CONFIGURATIONS

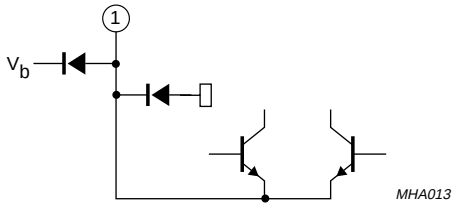


Fig.4 Pin 1; VEO.

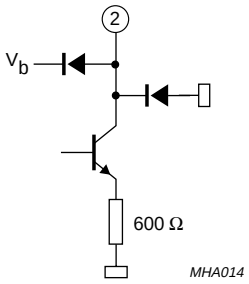


Fig.5 Pin 2; VEI.

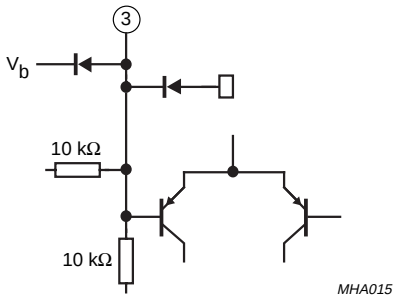


Fig.6 Pin 3; C_{NR}.

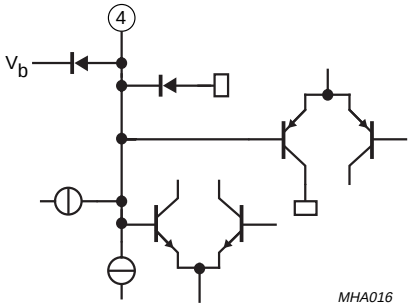


Fig.7 Pin 4; C_M.

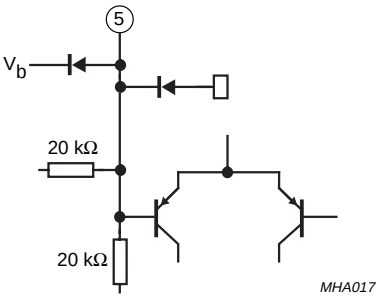


Fig.8 Pin 5; C_{DEC}.

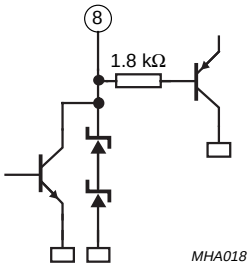


Fig.9 Pin 8; SDA.

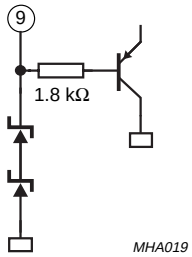


Fig.10 Pin 9; SCL.

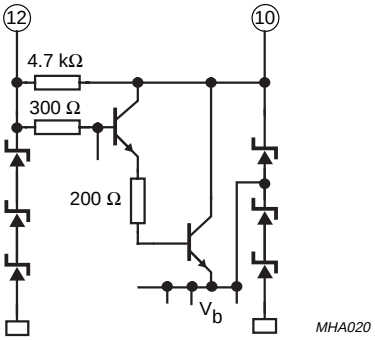


Fig.11 Pin 10; V_{CC} and pin 12; V_{CAP}.

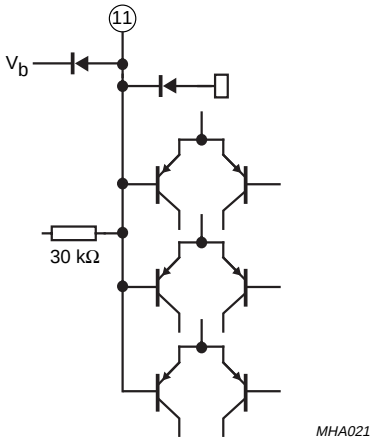


Fig.12 Pin 11; COMP.

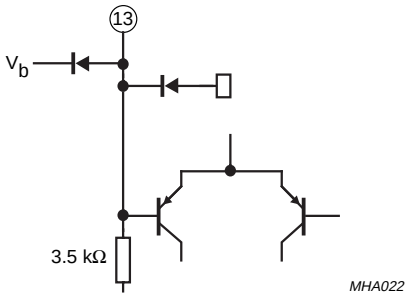


Fig.13 Pin 13; C_{P1}.

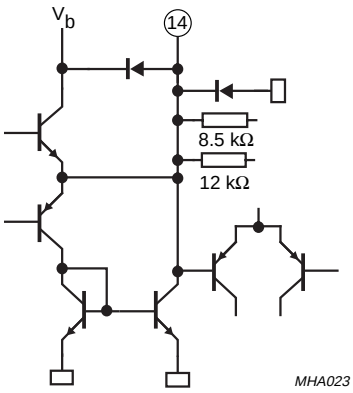


Fig.14 Pin 14; C_{P2}.

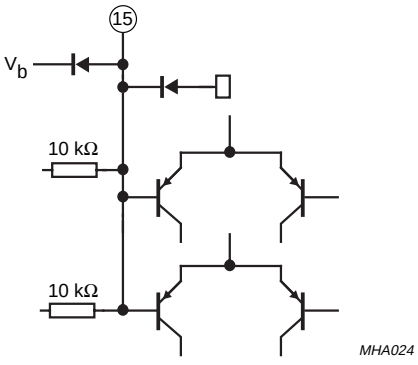


Fig.15 Pin 15; $C_{PH.}$

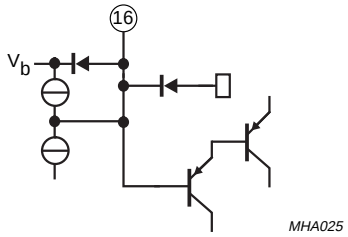


Fig.16 Pin 16; C_{ADJ}.

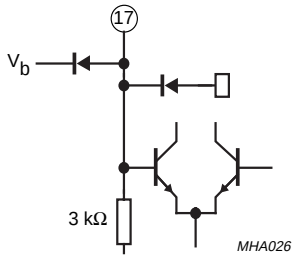


Fig.17 Pin 17; CER.

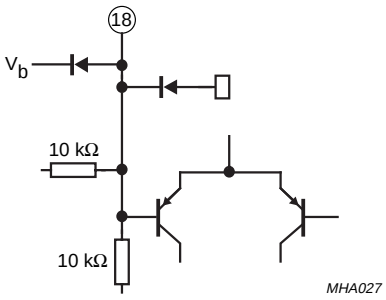


Fig.18 Pin 18; C_{MO} and pin 19; C_{SS}.

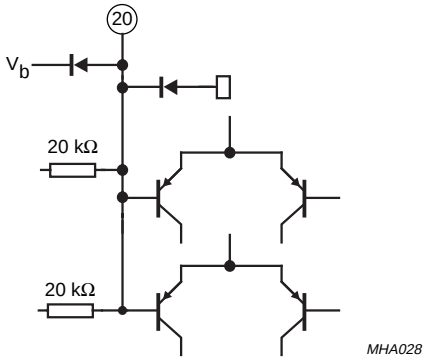


Fig.19 Pin 20; C_R and pin 25; C_L.

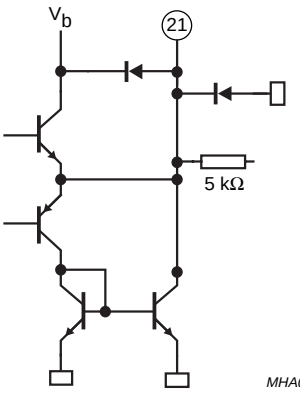


Fig.20 Pin 21; OUTR and pin 27 OUTL.

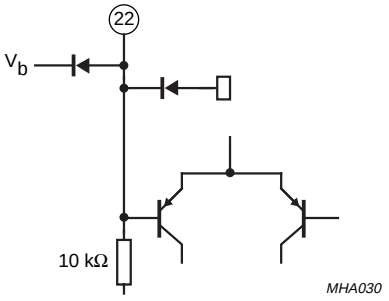


Fig.21 Pin 22; C_{SDE}.

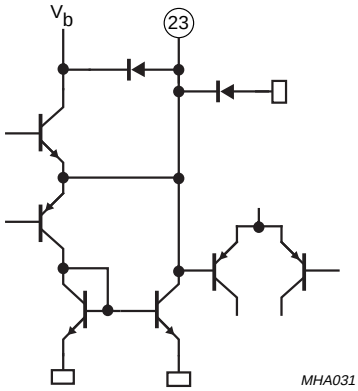


Fig.22 Pin 23; SAP.

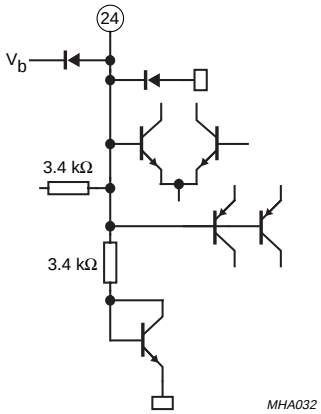


Fig.23 Pin 24; V_{ref}.

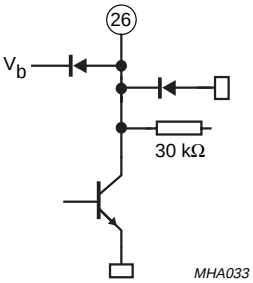


Fig.24 Pin 26; C_{ND}.

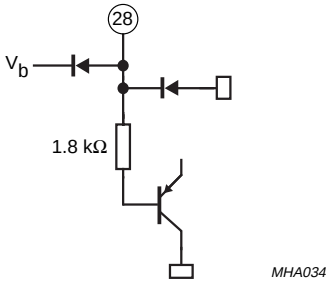


Fig.25 Pin 28; MAD.

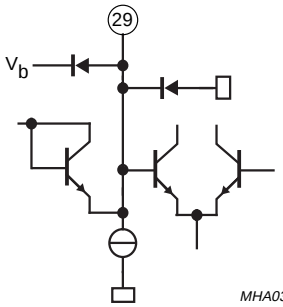


Fig.26 Pin 29; C_{TW} and pin 30; C_{TS}.

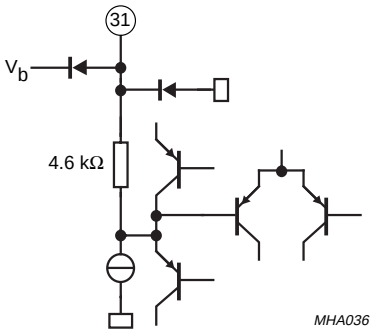
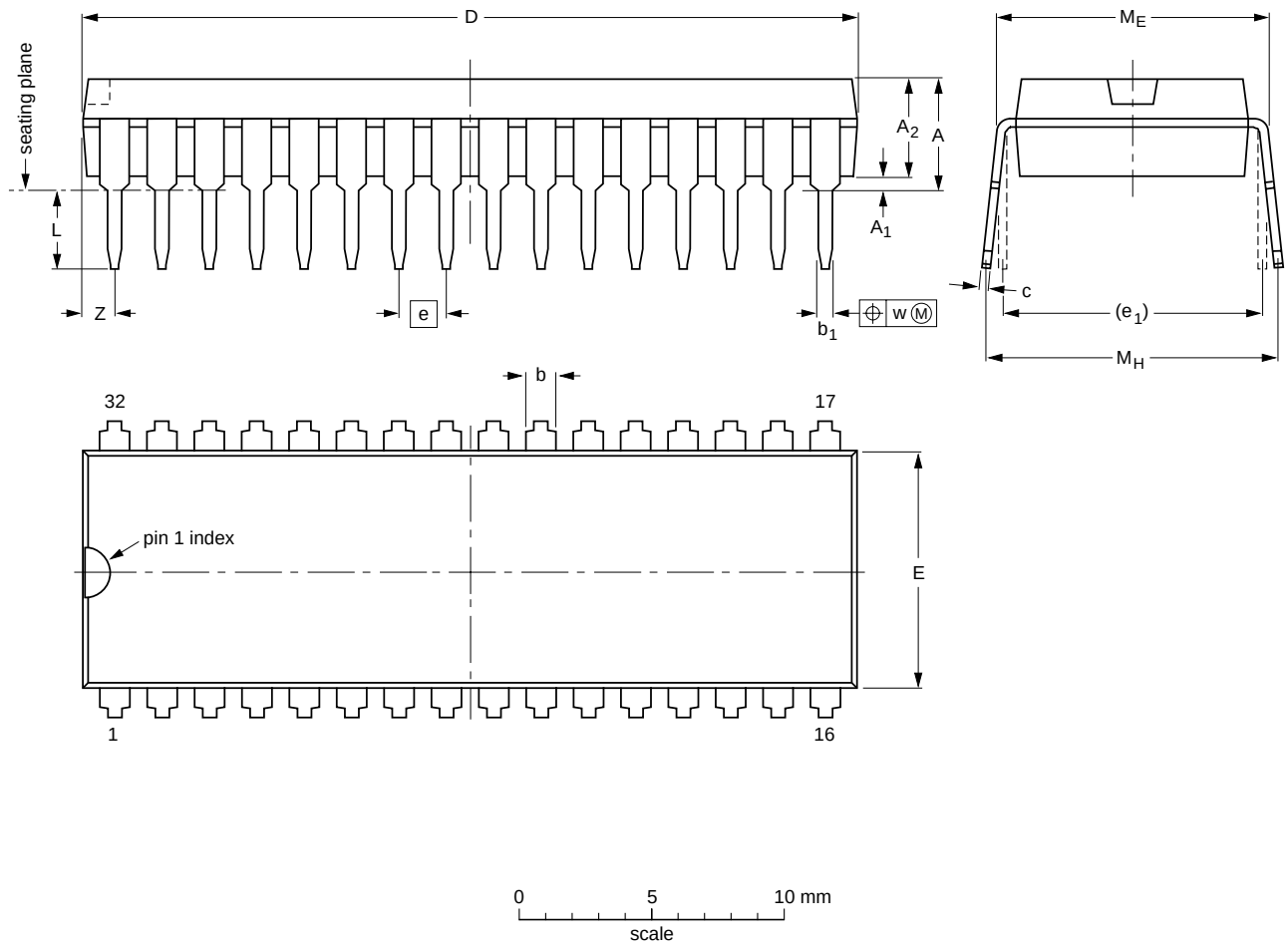


Fig.27 Pin 31; C_W and pin 32; C_S.

PACKAGE OUTLINES

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

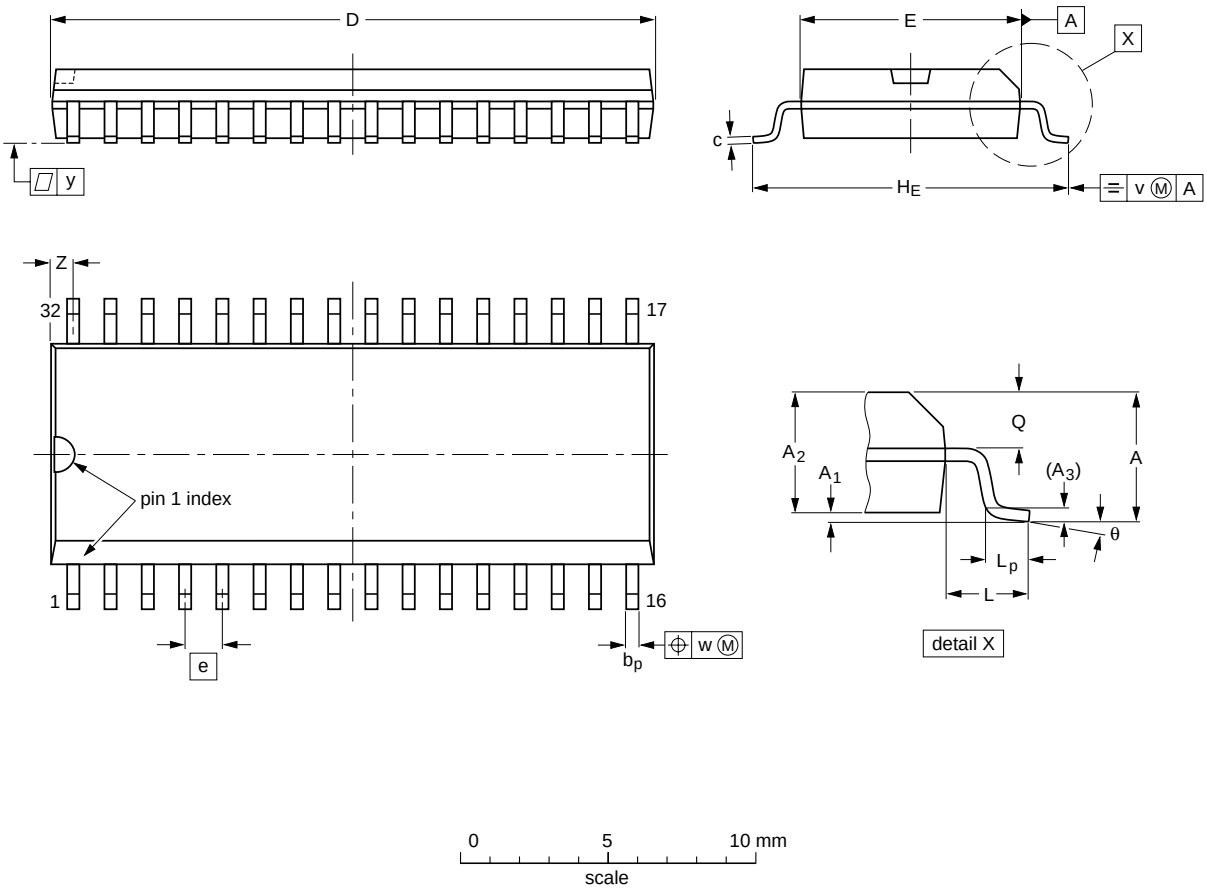
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.086	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT287-1						~~95-01-25~~ 97-05-22

SOLDERING DIP, SDIP, HDIP, DBS and SIL

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dip or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SOLDERING SO

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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NOTES

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