

# DATA SHEET

## **TDA8581**

**Multi-purpose high-gain power  
amplifier**

Preliminary specification  
File under Integrated Circuits, IC01

1998 May 27

**Multi-purpose high-gain power amplifier****TDA8581****FEATURES****General**

- High gain
- Operating voltage from 8 to 28 V
- Low distortion
- Few external components, fixed gain
- High output power
- Can be used as a stereo amplifier in bridge-tied load (BTL) or quad single-ended (SE) amplifiers
- Single-ended mode without loudspeaker capacitor
- Mute and standby mode with one- or two-pin operation
- Diagnostic information for Dynamic Distortion Detector (DDD), high temperature (145 °C) and short-circuit
- No switch on/off plops when switching between 'standby' to 'mute' and from 'mute' to 'on'
- Low offset variation at outputs between 'mute' and 'on'
- Fast mute on supply voltage drops.

**Protection**

- Reverse polarity safe (with protection diode added)
- Short-circuit proof to ground, positive supply voltage on all pins and across load
- ESD protected on all pins
- Thermal protection against temperatures exceeding 150 °C
- Load dump protection
- Protected against open-circuit ground pins and output short-circuited to supply ground.

**GENERAL DESCRIPTION**

The TDA8581 is a stereo bridge-tied load (BTL) or a quad single-ended amplifier that operates over a wide supply voltage range from 8 to 28 V. This makes it suitable for many applications, such as car radios, television and home-sound systems.

Because of an internal voltage buffer, this device can be used without a capacitor connected in series with the load (SE application). A combined BTL and 2 × SE application can also be configured.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8581	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

## Multi-purpose high-gain power amplifier

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## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	operating supply voltage		8.0	–	28	V
$I_{q(\text{tot})}$	total quiescent current	$V_P = 14.4 \text{ V}$	–	120	140	mA
$I_{\text{stb}}$	standby supply current	$V_P = 14.4 \text{ V}$	–	1	50	$\mu\text{A}$
$G_V$	voltage gain	single-ended	38	40	42	dB
		bridge-tied load	44	46	48	dB
<b>Bridge-tied load application</b>						
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	–	16	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$ ; $R_L = 8 \Omega$	–	28	–	W
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$ ; $P_o = 1 \text{ W}$ ; $V_P = 14.4 \text{ V}$ ; $R_L = 8 \Omega$	–	0.05	–	%
		$f_i = 1 \text{ kHz}$ ; $P_o = 10 \text{ W}$ ; $V_P = 24 \text{ V}$ ; $R_L = 8 \Omega$	–	0.05	–	%
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$ ; 'mute' condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$ ; 'on' condition	–	0	120	mV
$V_{\text{no}}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$	–	200	320	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ ; 'on' or 'mute' condition; $R_S = 0 \Omega$	55	–	–	dB
<b>Single-ended application</b>						
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}$ ; $R_L = 4 \Omega$	–	4.2	–	W
		THD = 0.5%; $V_P = 24 \text{ V}$ ; $R_L = 4 \Omega$	–	13	–	W
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}$ ; 'mute' condition; $R_L = 4 \Omega$	–	10	20	mV
		$V_P = 14.4 \text{ V}$ ; 'on' condition	–	0	120	mV
$V_{\text{no}}$	noise output voltage	$R_S = 1 \text{ k}\Omega$ ; $V_P = 14.4 \text{ V}$	–	160	280	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1 \text{ kHz}$ ; $V_{\text{ripple(p-p)}} = 2 \text{ V}$ ; 'on' or 'mute' condition; $R_S = 0 \Omega$	42	–	–	dB

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BLOCK DIAGRAM

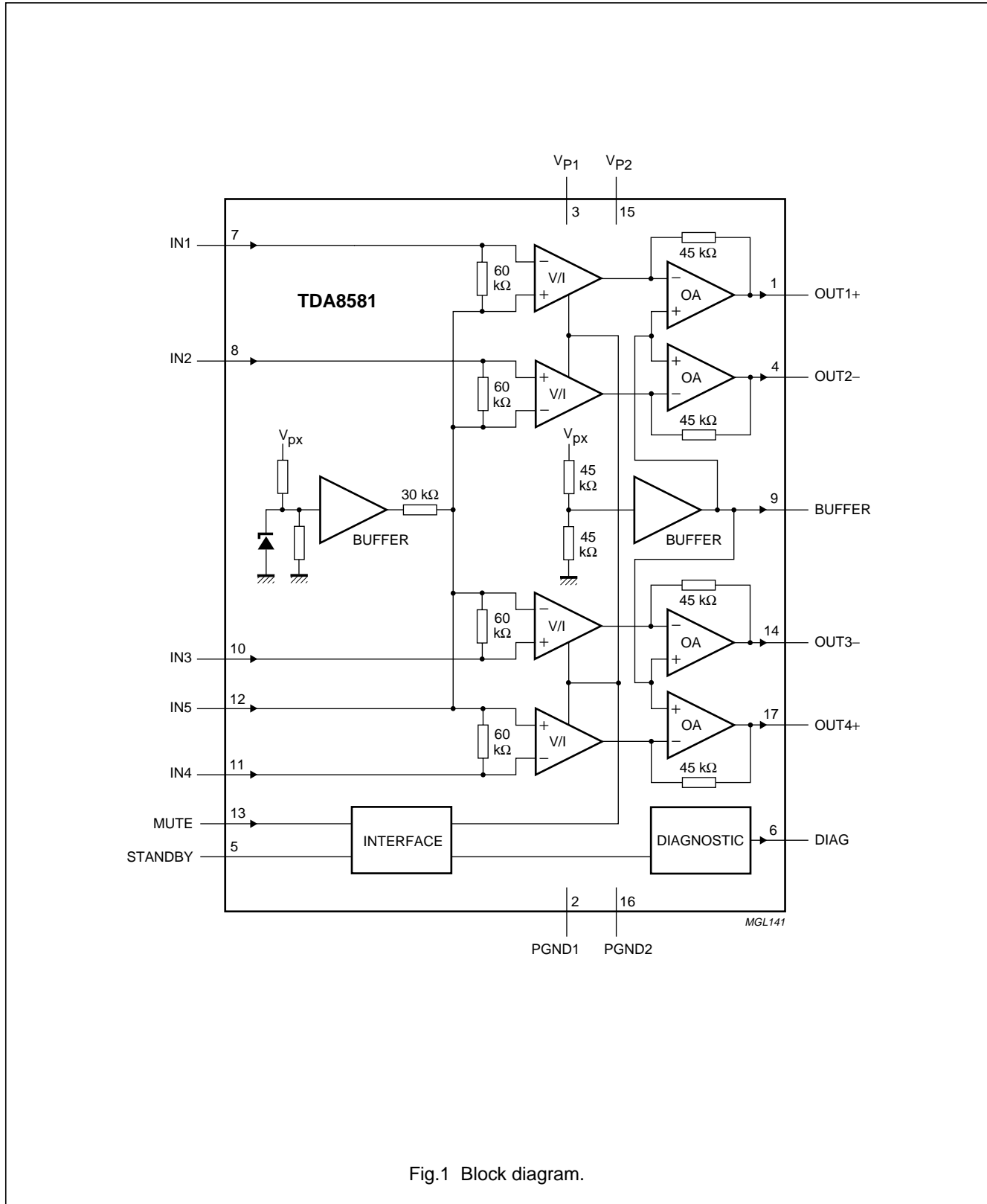


Fig.1 Block diagram.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
OUT1+	1	non-inverting output 1
PGND1	2	power ground 1
V <sub>P1</sub>	3	supply voltage 1
OUT2-	4	inverting output 2
STANDBY	5	'standby'/'mute'/'on' selection
DIAG	6	diagnostic output
IN1	7	input 1
IN2	8	input 2
BUFFER	9	buffer output (single-ended output buffer)
IN3	10	input 3
IN4	11	input 4
IN5	12	input 5; signal ground capacitor
MUTE	13	'mute'/'on' selection
OUT3-	14	inverting output 3
V <sub>P2</sub>	15	supply voltage 2
PGND2	16	power ground 2
OUT4+	17	non-inverting output 4

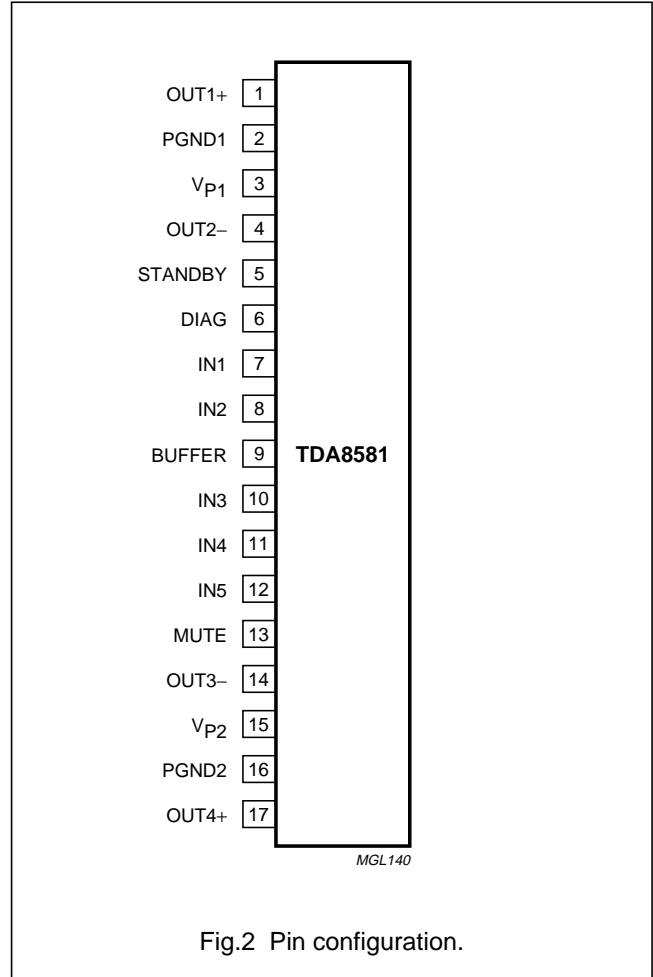


Fig.2 Pin configuration.

# Multi-purpose high-gain power amplifier

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## FUNCTIONAL DESCRIPTION

The TDA8581 is a multi-purpose power amplifier with four amplifiers which can be connected in the following configurations with high output power and low distortion (at minimum quiescent current);

- Dual bridge-tied load (BTL) amplifiers
- Quad single-ended amplifiers
- Dual single-ended amplifiers and one bridge-tied load amplifier.

The amplifier can be switched on (play or 'mute') and off ('standby') by the MUTE and STANDBY pins (for interfacing directly with a microcontroller). One-pin operation is also possible by applying a voltage greater than 8 V to the 'standby'/'mute'/'on' selection pin (pin 5) to switch the amplifier in 'on' mode.

Special attention is given to the dynamic behaviour as follows:

- Noise suppression during engine start.
- No pops when switching from 'standby' to 'on'.
- Slow offset change between 'mute' and 'on' (controlled by MUTE and STANDBY pins).
- Low noise levels, which are independent of the supply voltage.

Protections are included to avoid the IC being damaged at:

- Over temperature:  $T > 150\text{ }^{\circ}\text{C}$ .
- Short-circuit of the output pin(s) to ground or supply rail. When short-circuited, the power dissipation is limited.
- A missing-current limiter which limits the maximum short circuit output current to PGND or  $V_P$  pins to 1.5 A. The dissipation and speaker current will be minimized because the short-circuited amplifier is switched off. The chip temperature is limited by the temperature protection.
- ESD protection (Human Body Model 3000 V, Machine Model 300 V).
- Energy handling. A DC voltage of 6 V can be connected to the output of any amplifier while the supply pins are short-circuited to ground. No high DC current will flow from the supply pins of the amplifier.
- Reverse battery only with protection diode added.

Diagnostics are available for the following conditions (see Figs 4 to 7):

- Amplifier in 'mute'
- Chip temperature greater than  $145\text{ }^{\circ}\text{C}$
- Distortion over 2.0% due to clipping
- Short-circuit protection active.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage	operating	8	28	V
		load dump protected; see Fig.3	–	45	V
$V_{DIAG}$	voltage on diagnostic pin		–	18	V
$I_{OSM}$	non-repetitive peak output current		–	6	A
$I_{ORM}$	repetitive peak output current		–	4.5	A
$V_{rev}$	reverse polarity voltage		–	6	V
$V_{sc}$	AC and DC short-circuit voltage of output pins across loads and to ground or supply pins	no external series resistor in supply line; note 1	–	24	V
$P_{tot}$	total power dissipation		–	75	W
$T_j$	junction temperature		–	150	$^{\circ}\text{C}$
$T_{stg}$	storage temperature		–55	+150	$^{\circ}\text{C}$
$T_{amb}$	operating ambient temperature		–40	+150	$^{\circ}\text{C}$

## Note

1. The maximum supply voltage under short circuit conditions is 28 V with an additional resistor in the supply line of  $tbf\ \Omega$ .

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th\ j-c}$	thermal resistance from junction to case		1.5	K/W

## CHARACTERISTICS

$V_P = 14.4\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $f_i = 1\text{ kHz}$ ;  $R_L = \infty$ ; measured in test circuit of Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_P$	operating supply voltage		8.0	14.4	28	V
$I_{q(tot)}$	total quiescent current		–	120	140	mA
$I_{stb}$	standby current		–	1	50	$\mu\text{A}$
$V_O$	DC output voltage	$V_P = 14.4\text{ V}$	–	7.0	–	V
$V_{P(mute)}$	low supply voltage mute		6.0	7.0	8.0	V
$V_o$	single-ended and bridge-tied load output voltage	$V_P = 14.4\text{ V}$ ; 'mute' condition	–	–	20	mV
$V_I$	DC input voltage	$V_P = 14.4\text{ V}$	–	4.8	–	V
<b>STANDBY PIN (see Table 1)</b>						
$V_{5(stb)}$	voltage at STANDBY pin for 'standby' condition		0	–	0.8	V
$V_{hys(5)(stb)}$	hysteresis voltage at STANDBY pin for 'standby' condition	note 1	–	0.2	–	V
$V_{5(mute)}$	voltage at STANDBY pin for 'mute' condition	$V_{13} < 1\text{ V}$	2.0	–	5.5	V
$V_{5(on)}$	voltage at STANDBY pin for 'on' condition	$V_{13} < 1\text{ V}$ ; $V_P > 9\text{ V}$ ; note 2	8.0	–	18	V
<b>MUTE PIN (see Table 1)</b>						
$V_{13(mute)}$	voltage at MUTE pin for 'mute' condition	$V_5 = 5\text{ V}$	0	–	1.0	V
$V_{13(on)}$	voltage at MUTE pin for 'on' condition	$V_5 = 5\text{ V}$	3.5	–	5.5	V
<b>Diagnostic; output buffer (open-collector); see Figs 4, 5, 6 and 7</b>						
$V_{OL}$	low level output voltage	$I_{sink} = 1\text{ mA}$	–	0.2	0.8	V
$I_{LI}$	leakage current	$V_{DIAG} = 14.4\text{ V}$	–	–	1	$\mu\text{A}$
CD	clip detector	$V_{DIAG} < 0.8\text{ V}$	tbf	2	tbf	%
$T_{j(diag)}$	junction temperature for high temperature warning	$V_{DIAG} < 0.8\text{ V}$	–	145	–	$^{\circ}\text{C}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Stereo BTL application (see Fig.8)</b>						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega; \text{filter: } f < 30 \text{ kHz}$	–	0.2	–	%
		$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; V_P = 14.4 \text{ V}; R_L = 4 \Omega$	–	0.05	–	%
		$f_i = 1 \text{ kHz}; P_o = 10 \text{ W}; V_P = 24 \text{ V}; R_L = 8 \Omega$	–	0.05	–	%
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	15	16	–	W
		THD = 0.5%; $V_P = 24 \text{ V}; R_L = 8 \Omega$	25	28	–	W
		THD = 10%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	18	20	–	W
		THD = 10%; $V_P = 24 \text{ V}; R_L = 8 \Omega$	–	35	–	W
$G_v$	voltage gain	$V_{o(\text{rms})} = 3 \text{ V}$	44	46	48	dB
$\alpha_{cs}$	channel separation	$P_o = 2 \text{ W}; f_i = 1 \text{ kHz}; R_L = 4 \Omega$	40	55	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB
$V_{\text{offset(DC)}}$	DC output offset voltage	$V_P = 14.4 \text{ V}; \text{'on' condition}$	–	0	120	mV
		$V_P = 14.4 \text{ V}; \text{'mute' condition}; R_L = 4 \Omega$	–	10	20	mV
$V_{no}$	noise output voltage	$R_s = 1 \text{ k}\Omega; V_P = 14.4 \text{ V}; \text{note 3}$	–	200	320	$\mu\text{V}$
$V_{no(\text{mute})}$	noise output voltage mute	note 3	–	0	20	$\mu\text{V}$
$V_{o(\text{mute})}$	output voltage mute	$V_{i(\text{rms})} = 1 \text{ V}$	–	15	1500	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega; f_i = 1 \text{ kHz}; V_{\text{ripple(p-p)}} = 2 \text{ V}; \text{'on' or 'mute' condition}$	48	–	–	dB
$Z_i$	input impedance		23	30	37	k $\Omega$
CMRR	common mode rejection ratio	$R_s = 0 \Omega; V_{i(\text{rms})} = 0.5 \text{ V}; f_i = 1 \text{ kHz}$	–	40	–	dB
<b>Quad SE application (see Fig.9)</b>						
THD	total harmonic distortion	$f_i = 1 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega$	–	0.05	0.1	%
		$f_i = 10 \text{ kHz}; P_o = 1 \text{ W}; R_L = 4 \Omega; \text{filter: } f < 30 \text{ kHz}$	–	0.2	–	%
$P_o$	output power	THD = 0.5%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	4	4.2	–	W
		THD = 0.5%; $V_P = 24 \text{ V}; R_L = 4 \Omega$	11.5	13	–	W
		THD = 10%; $V_P = 14.4 \text{ V}; R_L = 4 \Omega$	–	5.5	–	W
		THD = 10%; $V_P = 24 \text{ V}; R_L = 4 \Omega$	14	16	–	W



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_V$	voltage gain	$V_{o(rms)} = 3\text{ V}$	38	40	42	dB
$\alpha_{cs}$	channel separation	$P_o = 2\text{ W}$ ; $f_i = 1\text{ kHz}$ ; $R_L = 4\ \Omega$	40	46	–	dB
$ \Delta G_V $	channel unbalance		–	–	1	dB
$V_{offset(DC)}$	DC output offset voltage	$V_P = 14.4\text{ V}$ ; 'on' condition	–	0	100	mV
		$V_P = 14.4\text{ V}$ ; 'mute' condition; $R_L = 4\ \Omega$	–	10	20	mV
$V_{no}$	noise output voltage	$R_S = 1\text{ k}\Omega$ ; $V_P = 14.4\text{ V}$ ; note 3	–	160	280	$\mu\text{V}$
$V_{no(mute)}$	noise output voltage mute	note 3	–	0	20	$\mu\text{V}$
$V_{o(mute)}$	output voltage mute	$V_{i(rms)} = 1\text{ V}$	–	15	1500	$\mu\text{V}$
SVRR	supply voltage ripple rejection	$f_i = 1\text{ kHz}$ ; $V_{ripple(p-p)} = 2\text{ V}$ , 'on' or 'mute' condition; $R_S = 0\ \Omega$	42	–	–	dB
$Z_i$	input impedance		46	60	74	k $\Omega$
CMRR	common mode rejection ratio	$V_{i(rms)} = 0.5\text{ V}$ ; $f_i = 1\text{ kHz}$ ; $R_S = 0\ \Omega$	–	40	–	dB

**Notes to the characteristics**

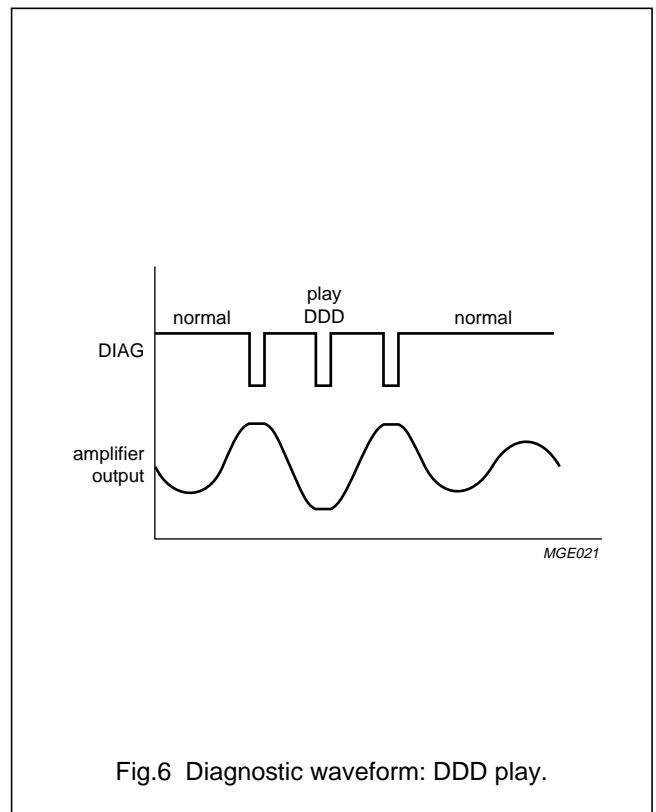
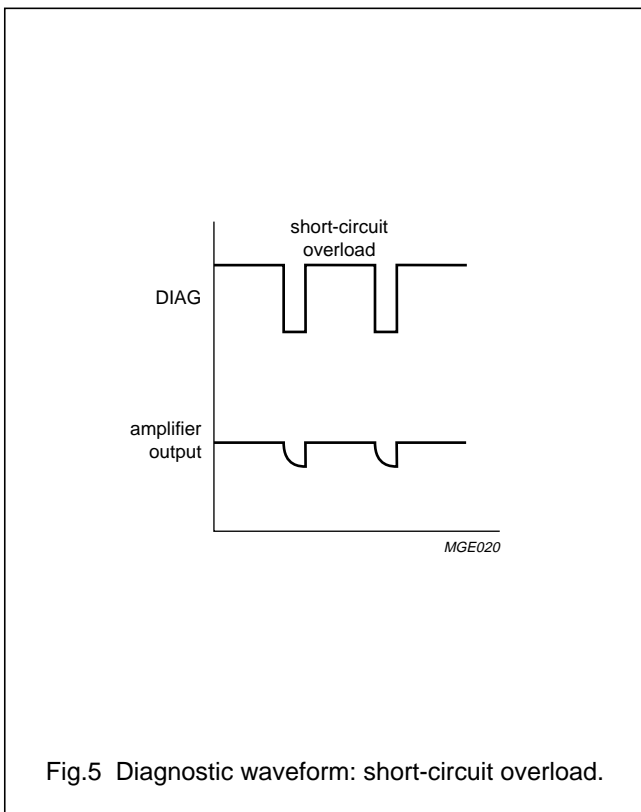
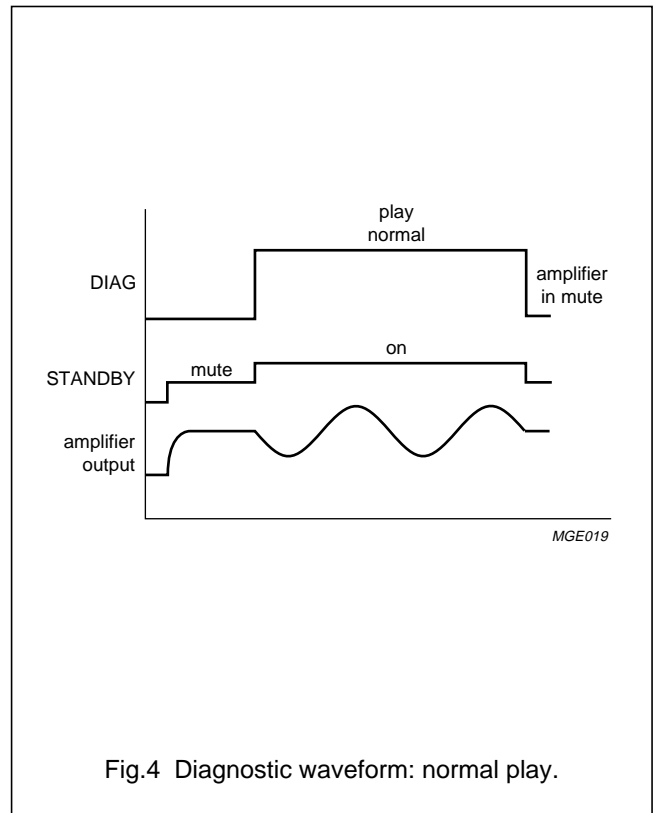
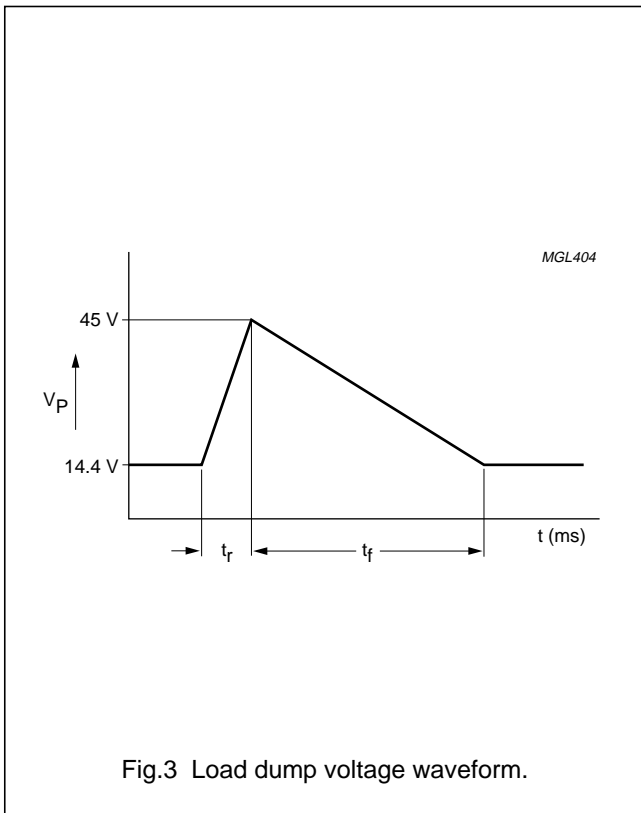
1. Hysteresis between rise and fall voltage.
2. At lower  $V_P$  the voltage at the STANDBY pin for 'on' condition will be adjusted automatically to maintain an 'on' condition at low battery voltage (down to 8 V) when using one-pin operation.
3. The noise output is measured in a bandwidth of 20 Hz to 20 kHz.

**Table 1** Selection of 'standby', 'mute' and 'on'.

VOLTAGE AT PIN 5	VOLTAGE AT PIN 13	FUNCTION
$V_5 < 0.8\text{ V}$	don't care	'standby' (off)
$2\text{ V} < V_5 < 5.3\text{ V}$	$V_{13} < 1\text{ V}$	'mute' (DC settled)
$2\text{ V} < V_5 < 5.3\text{ V}$	$3.5\text{ V} < V_{13} < 5.3\text{ V}$	'on' (AC operating)
$V_5 \geq 8.0\text{ V}$	don't care	'on' (AC operating)

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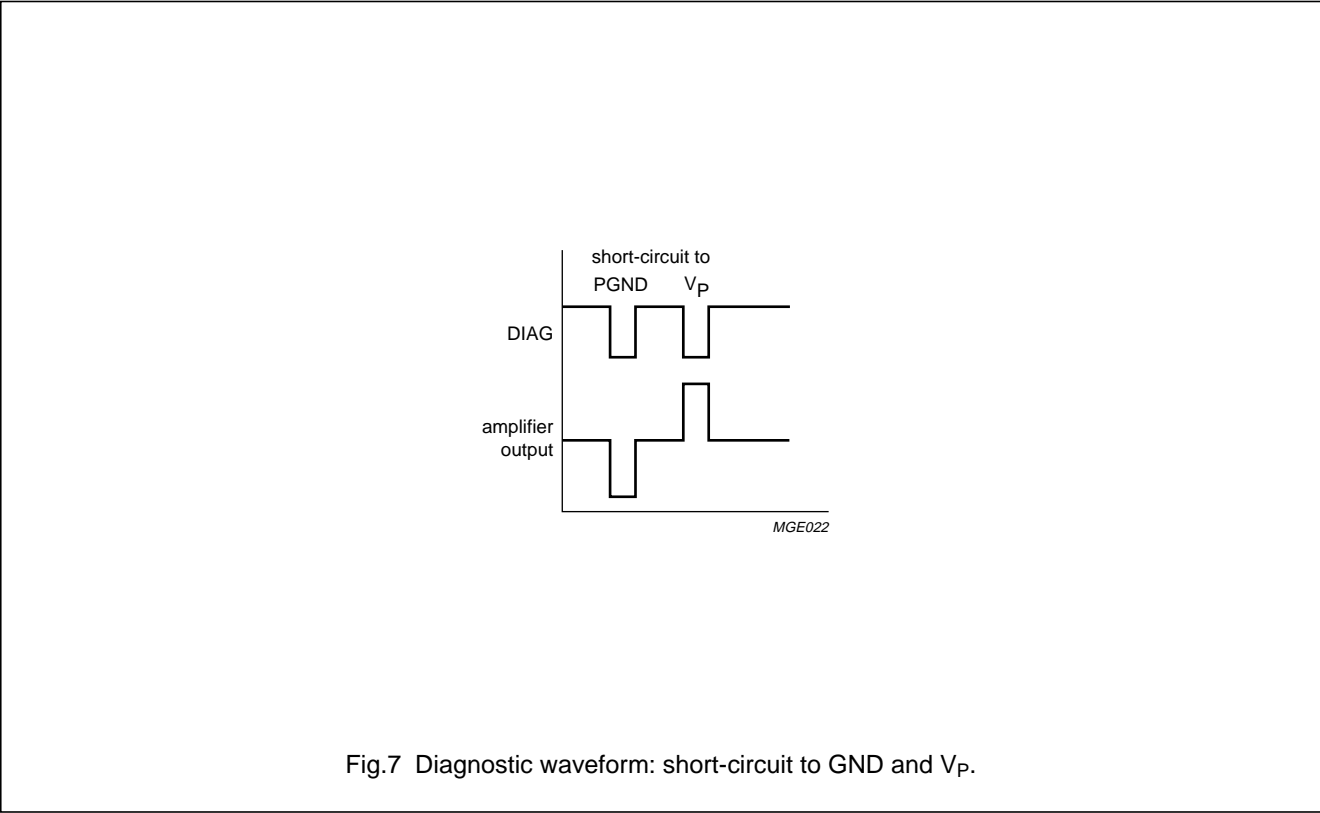


Fig.7 Diagnostic waveform: short-circuit to GND and Vp.

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APPLICATION INFORMATION

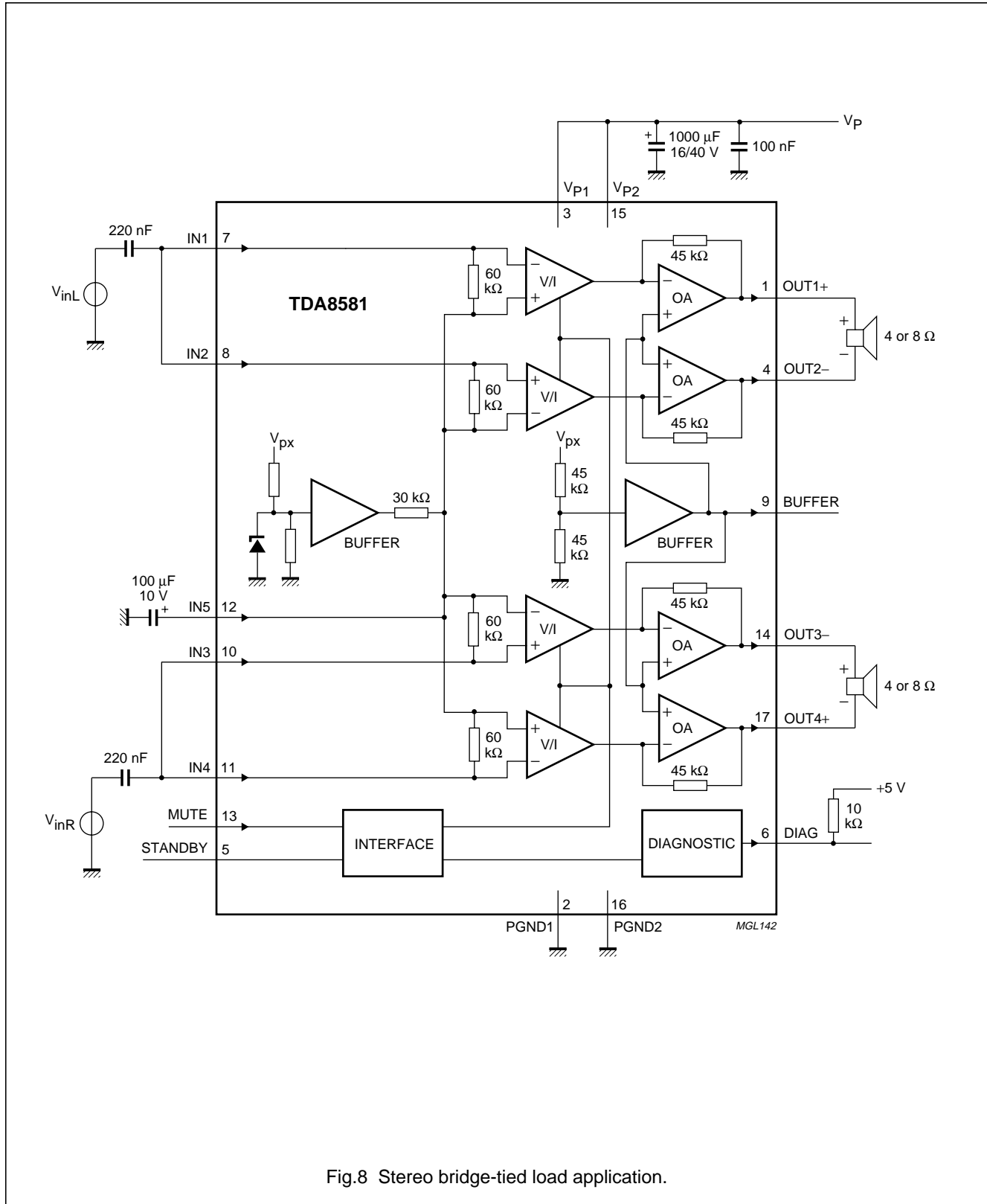


Fig.8 Stereo bridge-tied load application.

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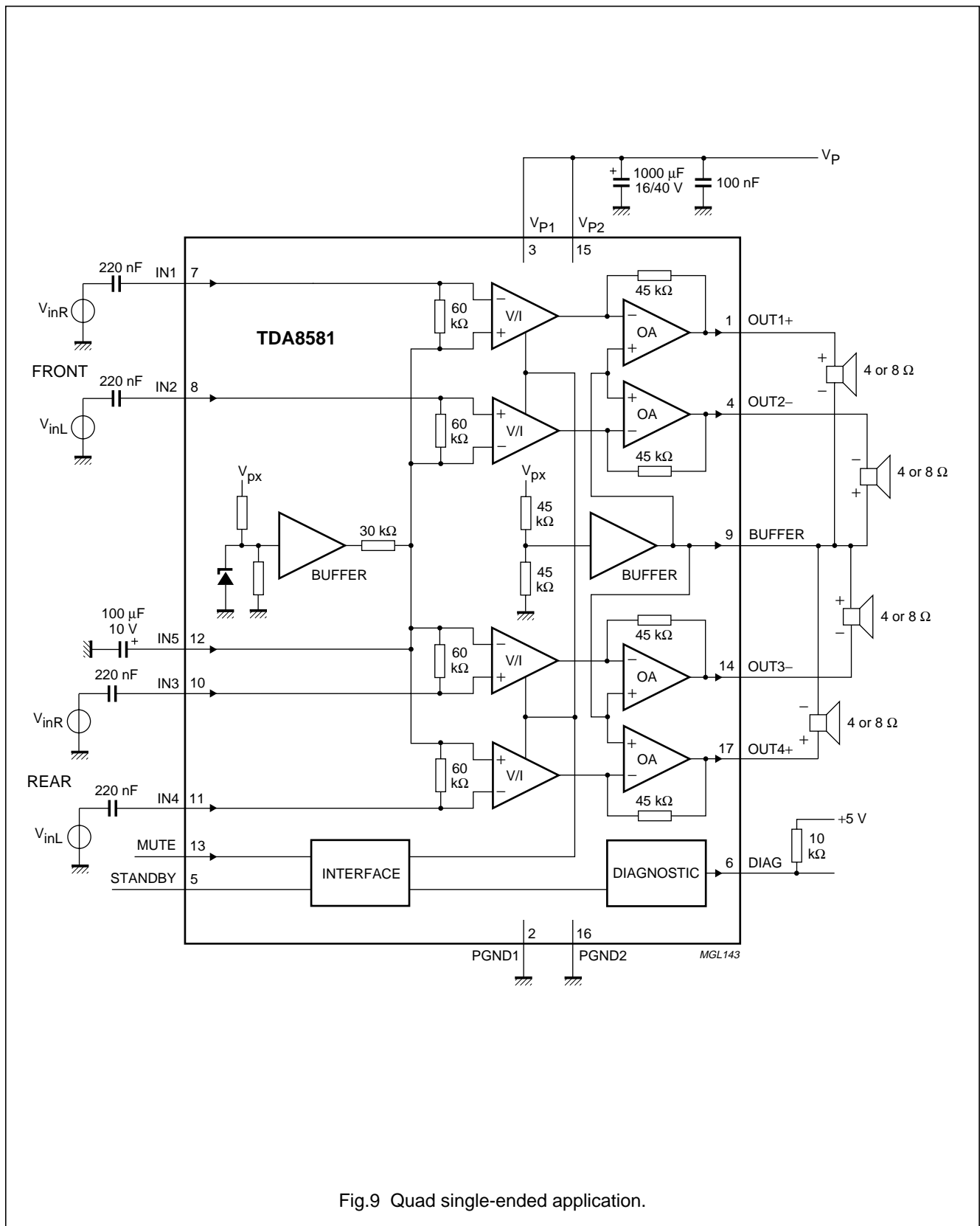


Fig.9 Quad single-ended application.

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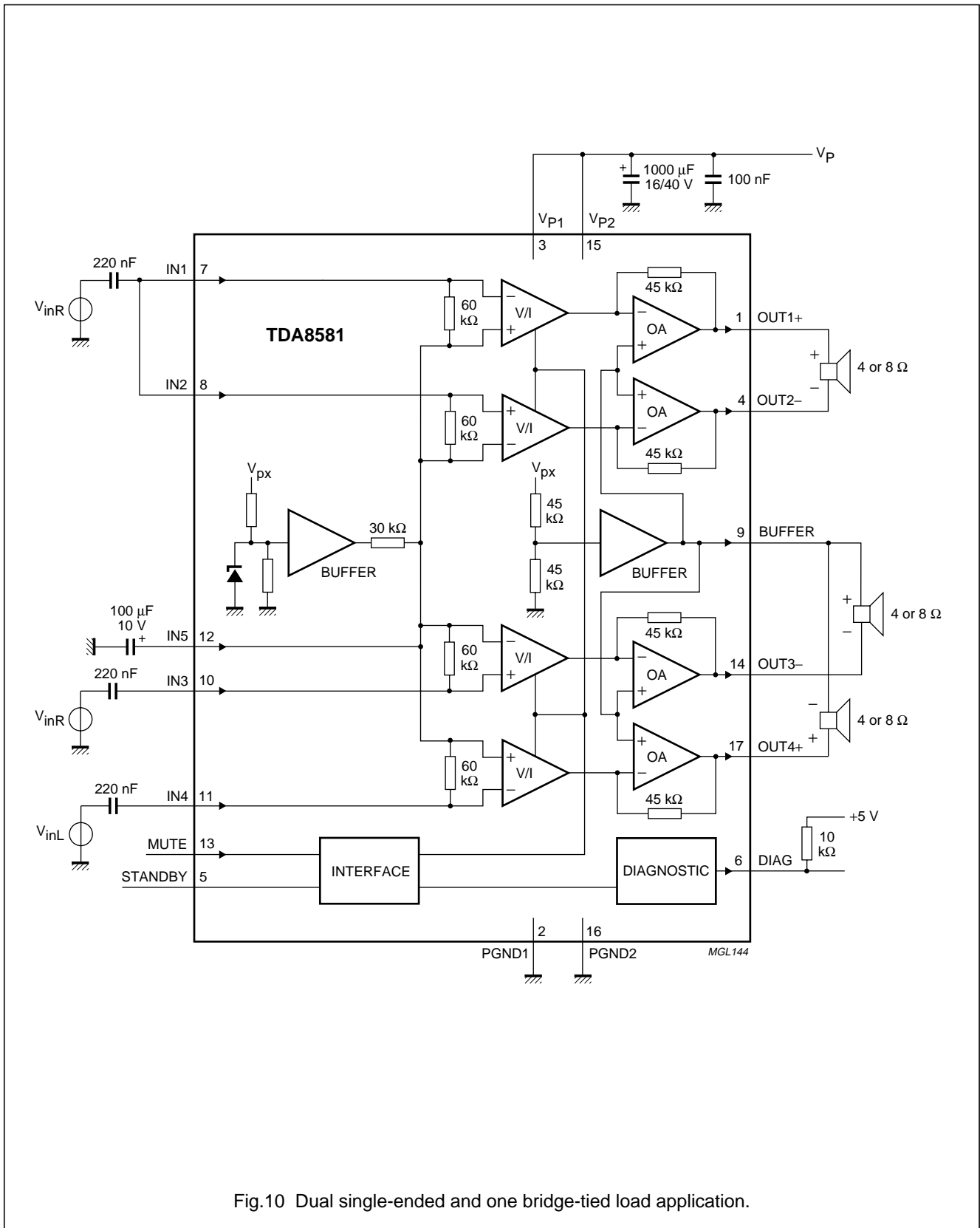
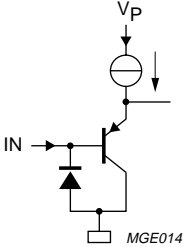
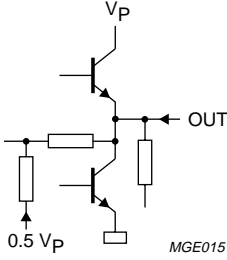
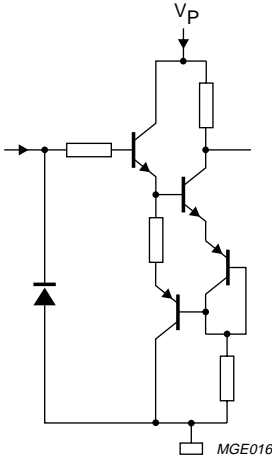


Fig.10 Dual single-ended and one bridge-tied load application.

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INTERNAL PIN CONFIGURATION

PIN	NAME	EQUIVALENT CIRCUIT
7, 8, 10, 11 and 12	inputs	
1, 4, 14 and 17	outputs	
5 and 13	mode select	

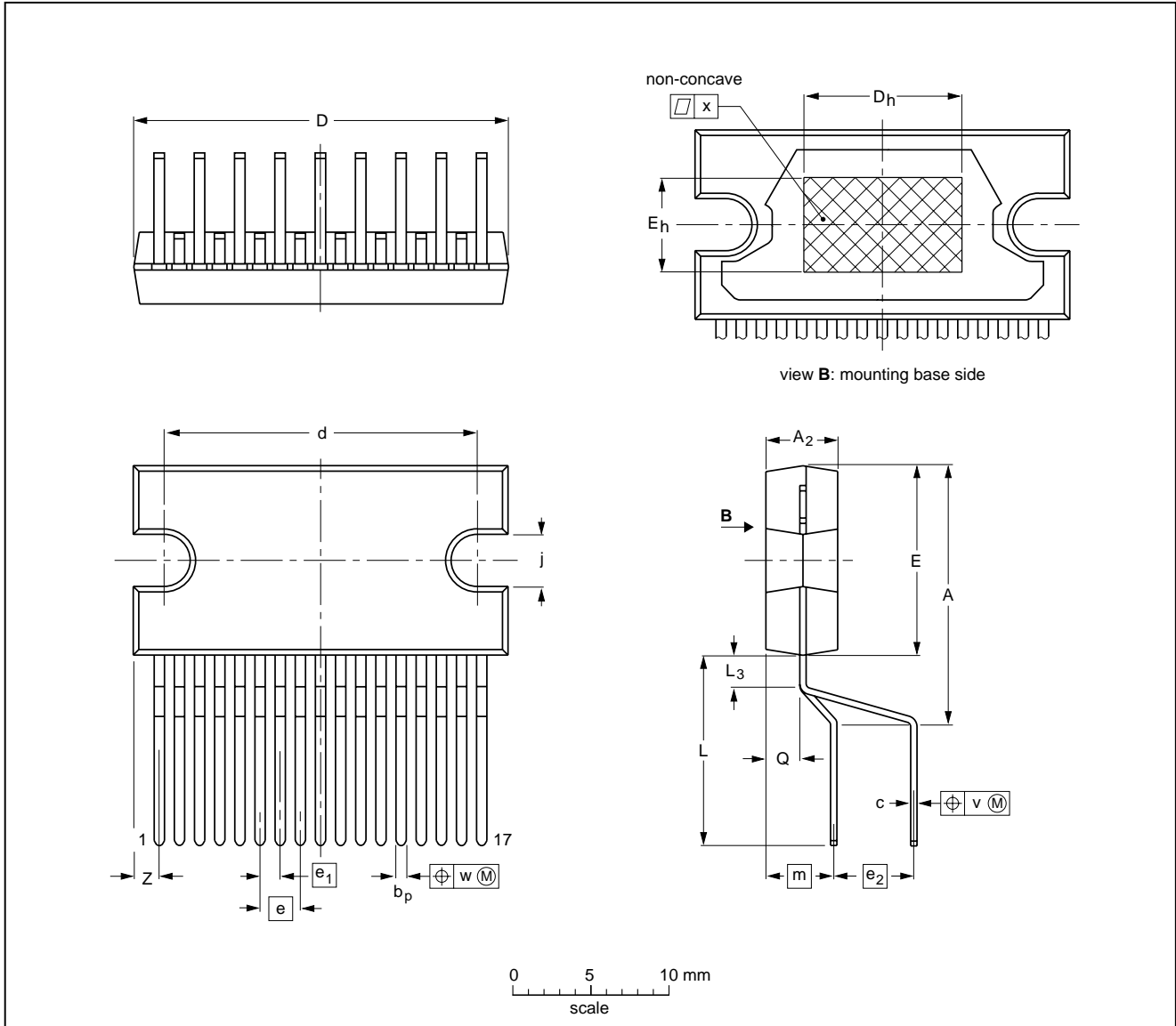
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>2</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	e <sub>1</sub>	e <sub>2</sub>	E <sub>h</sub>	j	L	L <sub>3</sub>	m	Q	v	w	x	z <sup>(1)</sup>
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						95-03-11 97-12-16



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**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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**NOTES**

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**NOTES**

# Philips Semiconductors – a worldwide company

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