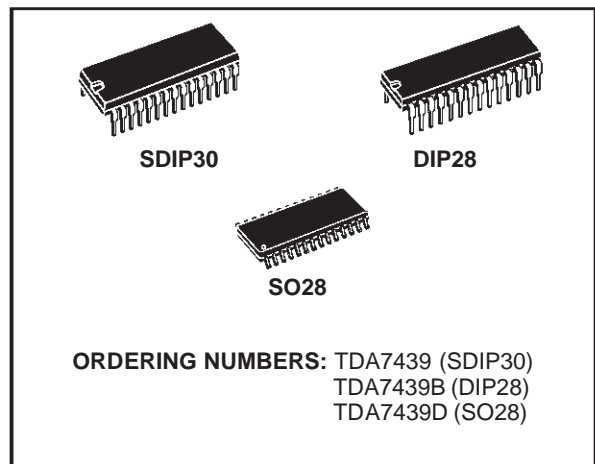


**THREE BANDS
DIGITALLY CONTROLLED AUDIO PROCESSOR**

- INPUT MULTIPLEXER
 - 4 STEREO INPUTS
 - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE, MIDDLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
 - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
 - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS



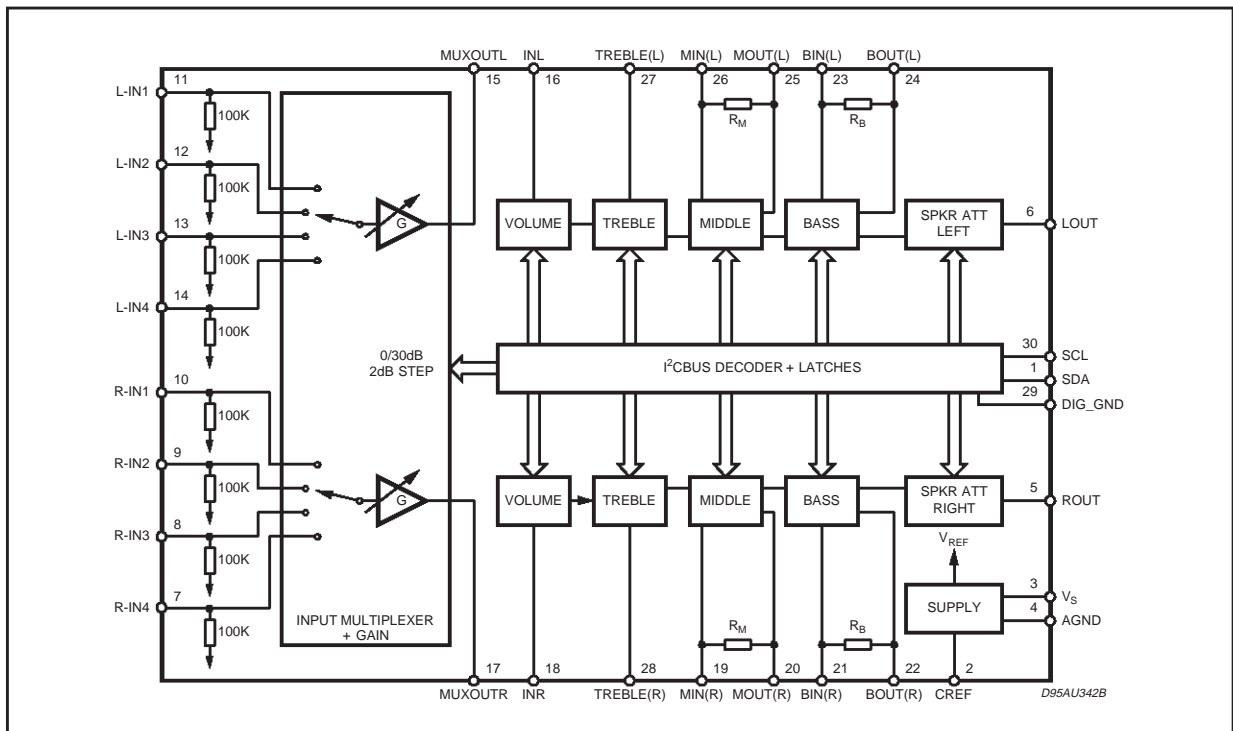
DESCRIPTION

The TDA7439 is a volume tone (bass, middle and treble) balance (Left/Right) processor for quality audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

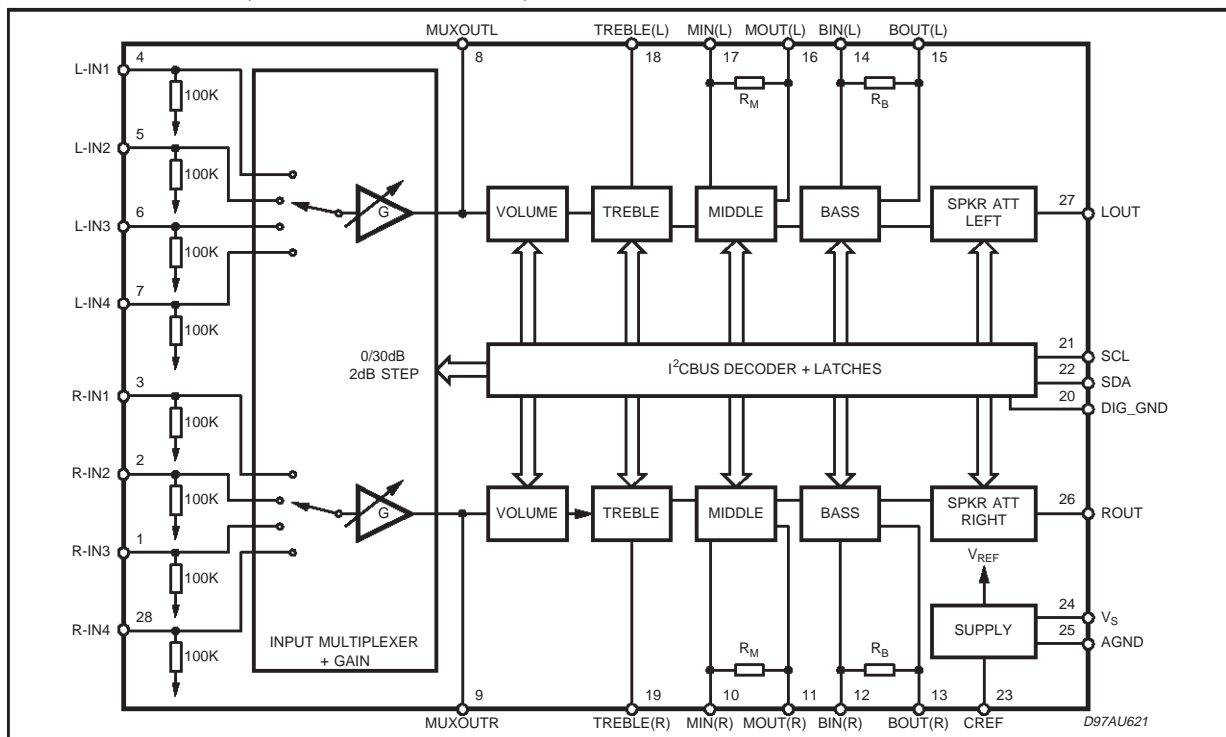
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

BLOCK DIAGRAM (TDA7439)

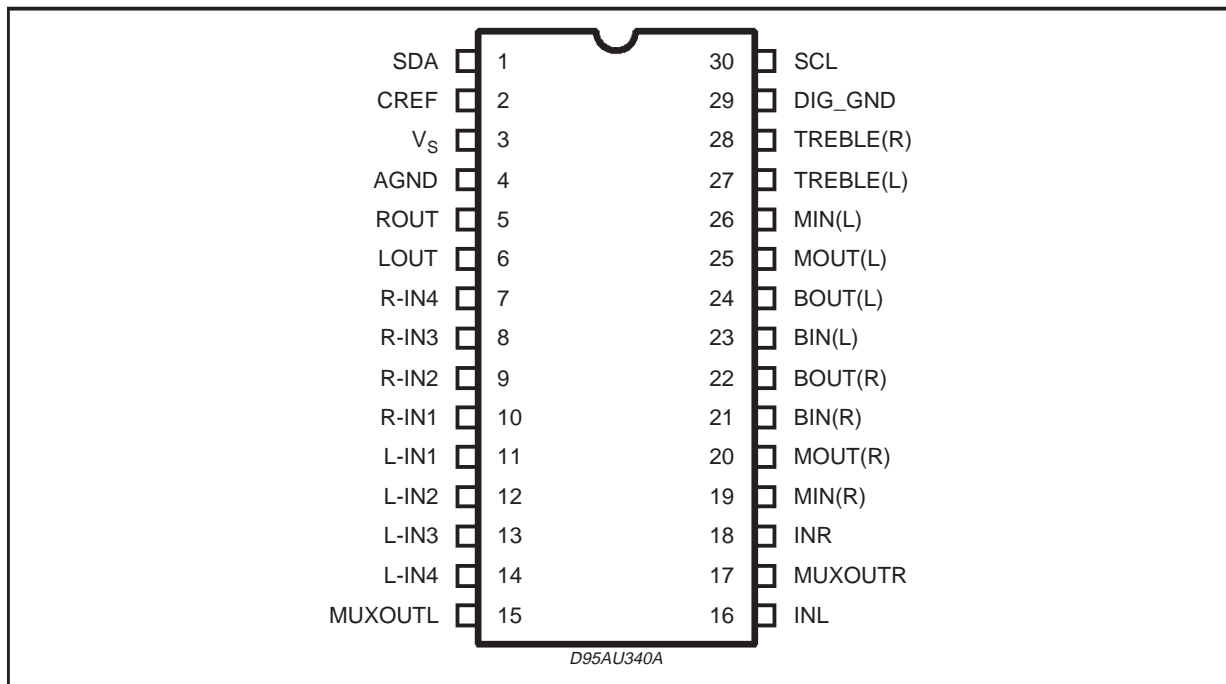


TDA7439

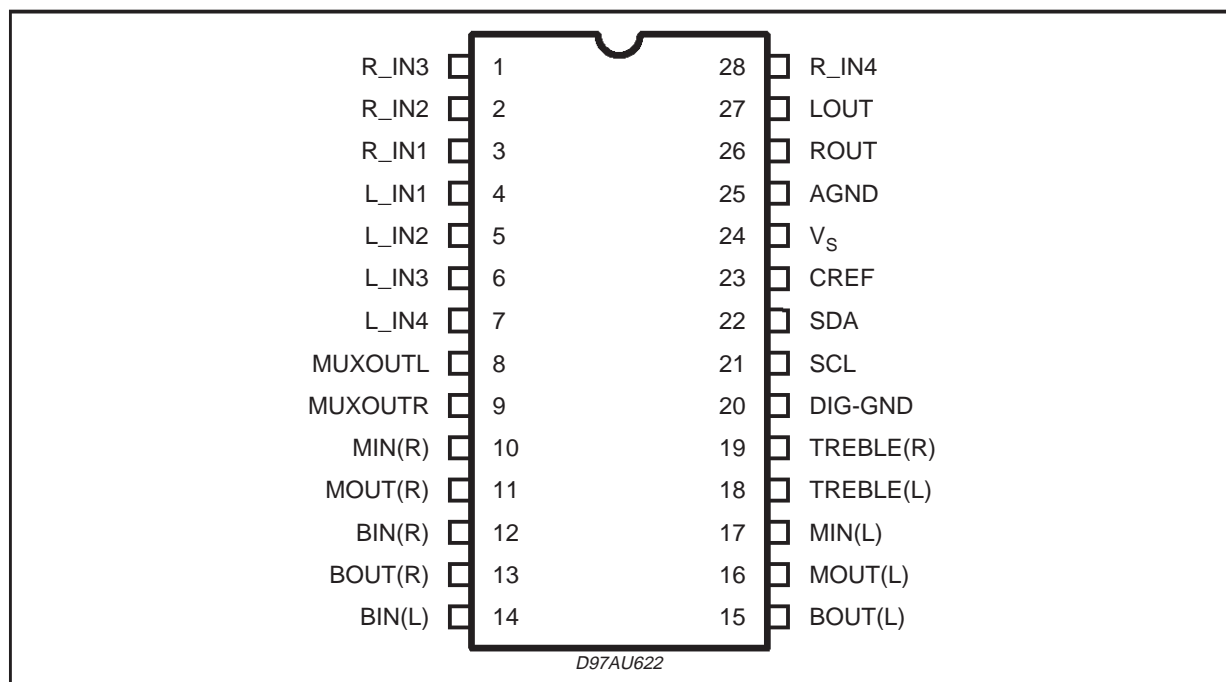
BLOCK DIAGRAM (TDA7439B/TDA7439D)



PIN CONNECTION (SDIP30)



PIN CONNECTION (DIP28/SO28)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _S	Operating Supply Voltage	10.5	V
T _{amb}	Operating Ambient Temperature	-10 to 85	°C
T _{stg}	Storage Temperature Range	-55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-pin}	Thermal Resistance Junction-pins	85	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _S	Supply Voltage	6	9	10.2	V
V _{CL}	Max. input signal handling	2			V _{rms}
THD	Total Harmonic Distortion V = 1V _{rms} f = 1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio V _{out} = 1V _{rms} (mode = OFF)		106		dB
S _C	Channel Separation f = 1KHz		90		dB
	Input Gain in (2dB step)	0		30	dB
	Volume Control (1dB step)	-47		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Middle Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step	-79		0	dB
	Mute Attenuation		100		dB

TDA7439

ELECTRICAL CHARACTERISTICS (refer to the test circuit $T_{amb} = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{K}\Omega$, $R_G = 600\Omega$, all controls flat ($G = 0\text{dB}$), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10.2	V
I_S	Supply Current		4	7	10	mA
SVR	Ripple Rejection		60	90		dB
INPUT STAGE						
R_{IN}	Input Resistance		70	100	130	$\text{K}\Omega$
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V _{rms}
S_{IN}	Input Separation	The selected input is grounded through a 2.2μ capacitor	80	100		dB
G_{inmin}	Minimum Input Gain		-1	0	1	dB
G_{inmax}	Maximum Input Gain		29	30	31	dB
G_{step}	Step Resolution		1.5	2	2.5	dB
VOLUME CONTROL						
R_i	Input Resistance		20	33	50	$\text{K}\Omega$
C_{RANGE}	Control Range		45	47	49	dB
A_{VMAX}	Max. Attenuation		45	47	49	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	$A_V = 0$ to -24dB	-1.0	0	1.0	dB
		$A_V = -24$ to -47dB	-1.5	0	1.5	dB
E_T	Tracking Error	$A_V = 0$ to -24dB		0	1	dB
		$A_V = -24$ to -47dB		0	2	dB
V_{DC}	DC Step	adjacent attenuation steps from 0dB to A_V max		0 0.5	3	mV mV
A_{mute}	Mute Attenuation		80	100		dB
BASS CONTROL (1)						
G_b	Control Range	Max. Boost/cut	± 12.0	± 14.0	± 16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		33	44	55	$\text{K}\Omega$
TREBLE CONTROL (1)						
G_t	Control Range	Max. Boost/cut	± 13.0	± 14.0	± 15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
MIDDLE CONTROL (1)						
G_m	Control Range	Max. Boost/cut	± 12.0	± 14.0	± 16.0	dB
M_{STEP}	Step Resolution		1	2	3	dB
R_M	Internal Feedback Resistance		18.75	25	31.25	$\text{K}\Omega$
SPEAKER ATTENUATORS						
C_{RANGE}	Control Range		70	76	82	dB
S_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	$A_V = 0$ to -20dB	-1.5	0	1.5	dB
		$A_V = -20$ to -56dB	-2	0	2	dB
V_{DC}	DC Step	adjacent attenuation steps		0	3	mV
A_{mute}	Mute Attenuation		80	100		dB

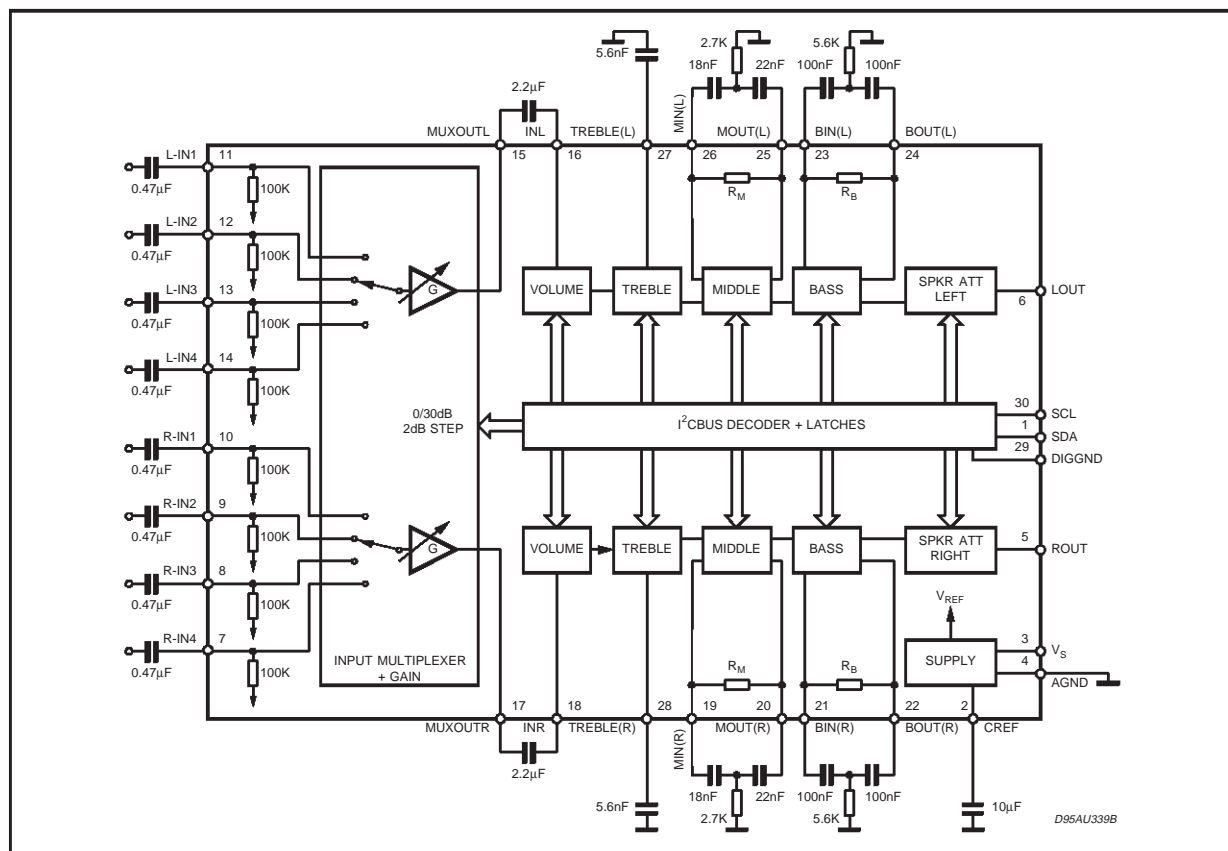
NOTE1:

- 1) The device is functionally good at $V_S = 5\text{V}$. a step down, on V_S , to 4V doesn't reset the device.
- 2) BASS, MIDDLE and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AUDIO OUTPUTS						
V _{CLIP}	Clipping Level	d = 0.3%	2.1	2.6		V _{RMS}
R _L	Output Load Resistance		2			KΩ
R _O	Output Impedance		10	30	50	Ω
V _{DC}	DC Voltage Level		3.5	3.8	4.1	V
GENERAL						
E _{NO}	Output Noise	All gains = 0dB; BW = 20Hz to 20KHz flat		5	15	μV
E _t	Total Tracking Error	A _V = 0 to -24dB		0	1	dB
		A _V = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All gains 0dB; V _O = 1V _{RMS} ;	95	106		dB
S _C	Channel Separation Left/Right		80	100		dB
d	Distortion	A _V = 0; V _I = 1V _{RMS} ;		0.01	0.08	%
BUS INPUT						
V _{IL}	Input Low Voltage				1	V
V _{IH}	Input High Voltage		3			V
I _{IN}	Input Current	V _{IN} = 0.4V	-5	0	5	μA
V _O	Output Voltage SDA Acknowledge	I _O = 1.6mA		0.4	0.8	V

TEST CIRCUIT



APPLICATION SUGGESTIONS

The first and the last stages are volume control blocks. The control range is 0 to -47dB (mute) for the first one, 0 to -79dB (mute) for the last one. Both of them have 1dB step resolution. The very high resolution allows the implementation of systems free from any noisy acoustical effect. The TDA7439 audioprocessor provides 3 bands tones control.

Bass, Middle Stages

The Bass and the middle cells have the same structure. The Bass cell has an internal resistor $R_i = 44K\Omega$ typical. The Middle cell has an internal resistor $R_i = 25K\Omega$ typical. Several filter types can be implemented, connecting external components to the Bass/Middle IN and OUT pins.

Figure 1.

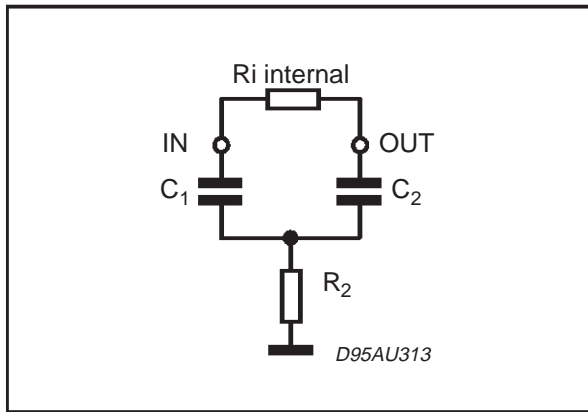
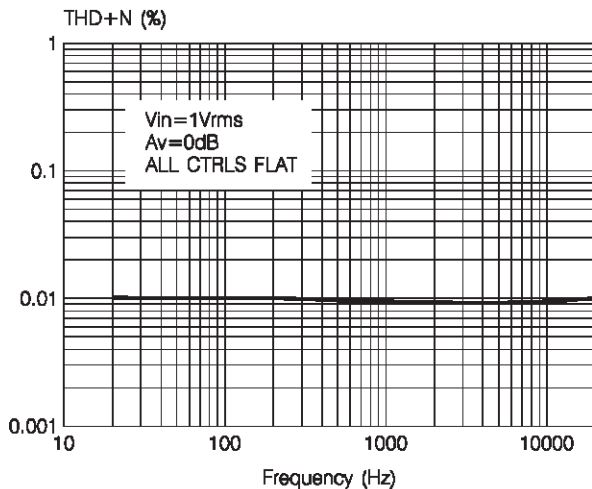


Figure 2: THD vs. frequency



The fig.1 refers to basic T Type Bandpass Filter starting from the filter component values (R_1 internal and R_2, C_1, C_2 external) the centre frequency F_c , the gain A_v at max. boost and the filter Q factor are computed as follows:

$$F_c = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}$$

$$A_v = \frac{R_2 C_2 + R_2 C_1 + R_i C_1}{R_2 C_1 + R_2 C_2}$$

$$Q = \frac{\sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}{R_2 C_1 + R_2 C_2}$$

Viceversa, once F_c , A_v , and R_i internal value are fixed, the external components values will be:

$$C_1 = \frac{A_v - 1}{2 \cdot \pi \cdot F_c \cdot R_i \cdot Q} \quad C_2 = \frac{Q^2 \cdot C_1}{A_v - 1 - Q^2}$$

$$R_2 = \frac{A_v - 1 - Q^2}{2 \cdot \pi \cdot C_1 \cdot F_c \cdot (A_v - 1) \cdot Q}$$

Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25K Ω typical) and an external capacitor connected between treble pins and ground. Typical responses are reported in Figg. 10 to 13.

CREF

The suggested 10 μ F reference capacitor (CREF) value can be reduced to 4.7 μ F if the application requires faster power ON.

Figure 3: THD vs. R_{LOAD}

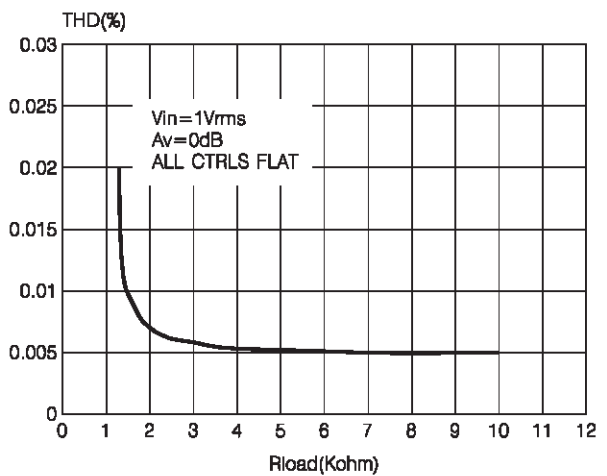


Figure 4: Channel separation vs. frequency

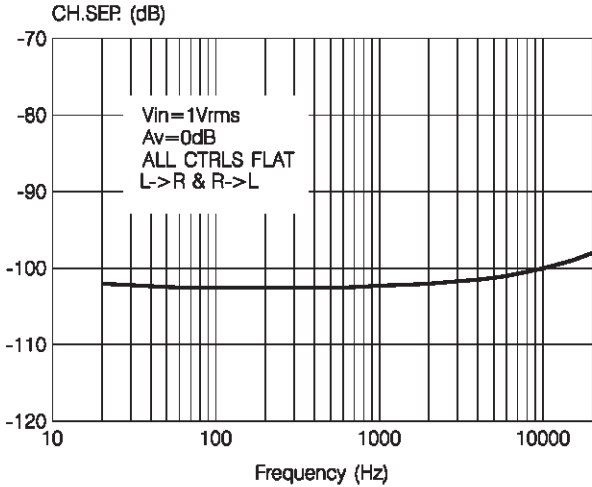


Figure 5: Bass response

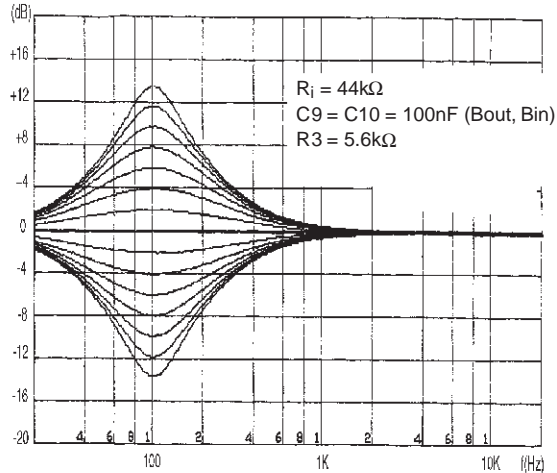


Figure 6: Middle response

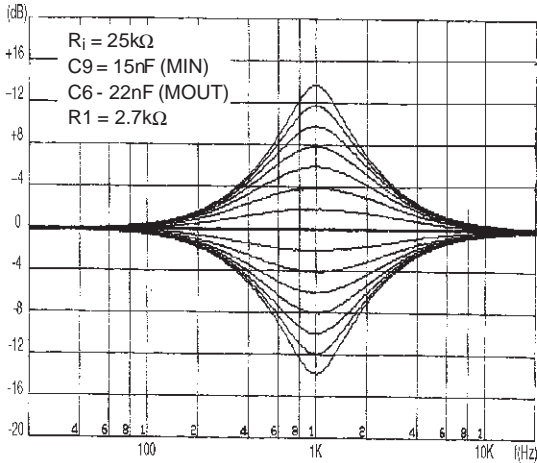


Figure 7: Treble response

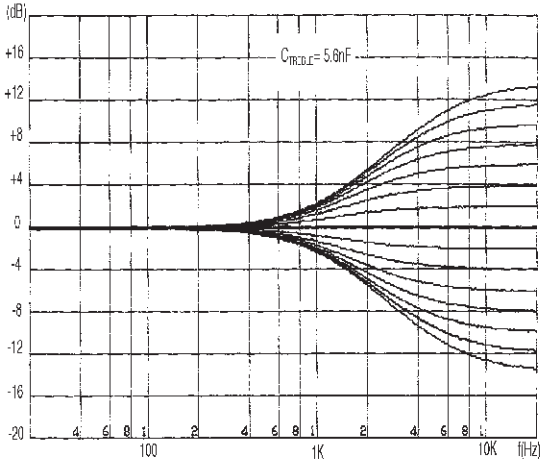
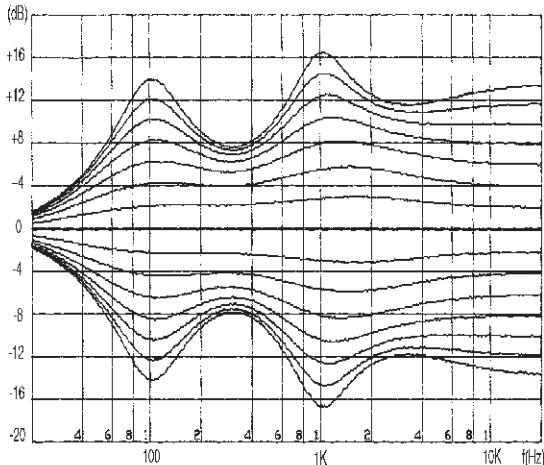


Figure 8: Typical tone response



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7439 and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 9, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.10 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

Acknowledge

The master (μ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 11). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the μ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 9: Data Validity on the I²CBUS

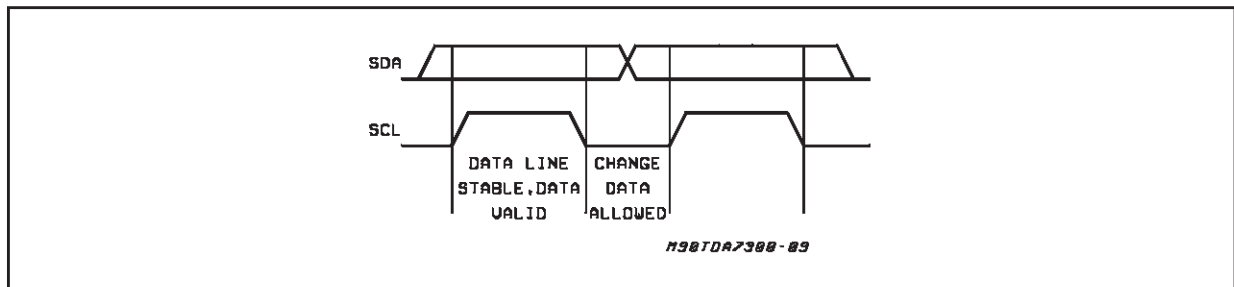


Figure 10: Timing Diagram of I²CBUS

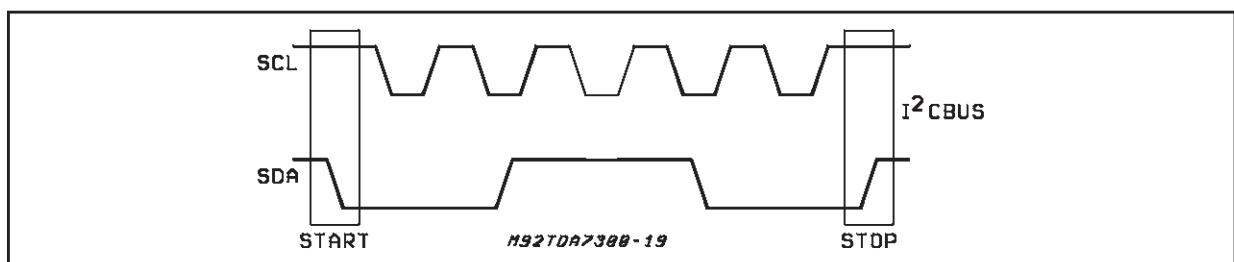
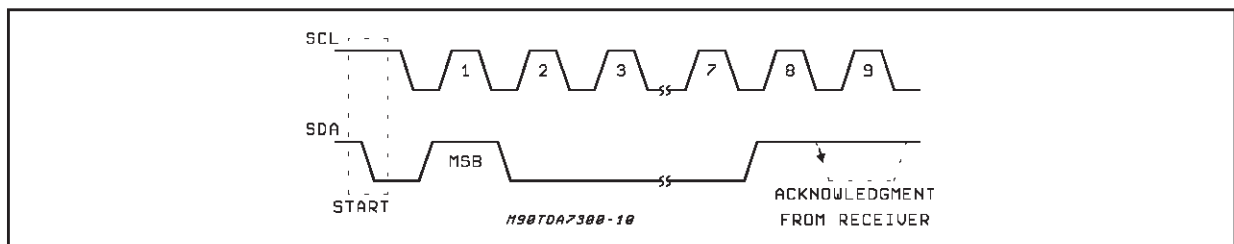


Figure 11: Acknowledge on the I²CBUS



SOFTWARE SPECIFICATION

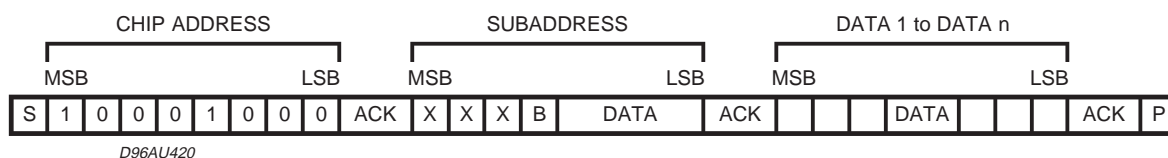
Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7439

address

- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

A = Address

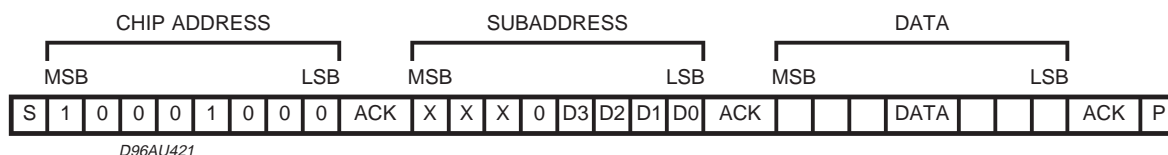
B = Auto Increment

EXAMPLES

No Incremental Bus

The TDA7439 receives a start condition, the cor-

rect chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

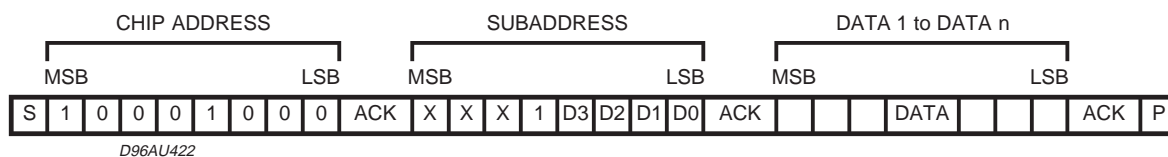


Incremental Bus

The TDA7439 receive a start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas

SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.



TDA7439

POWER ON RESET CONDITION

INPUT SELECTION	IN2
INPUT GAIN	28dB
VOLUME	MUTE
BASS	0dB
MIDDLE	2dB
TREBLE	2dB
SPEAKER	MUTE

DATA BYTES

Address = 88 HEX (ADDR:OPEN).

FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	VOLUME
X	X	X	B	0	0	1	1	BASS
X	X	X	B	0	1	0	0	MIDDLE
X	X	X	B	0	1	0	1	TREBLE
X	X	X	B	0	1	1	0	SPEAKER ATTENUATE "R"
X	X	X	B	0	1	1	1	SPEAKER ATTENUATE "L"

B = 1: INCREMENTAL BUS ACTIVE

B = 0: NO INCREMENTAL BUS

X = DON'T CARE

INPUT SELECTION

MSB							LSB	INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	IN4
X	X	X	X	X	X	0	1	IN3
X	X	X	X	X	X	1	0	IN2
X	X	X	X	X	X	1	1	IN1

DATA BYTES (continued)**INPUT GAIN SELECTION**

MSB							LSB	INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	0dB
				0	0	0	1	2dB
				0	0	1	0	4dB
				0	0	1	1	6dB
				0	1	0	0	8dB
				0	1	0	1	10dB
				0	1	1	0	12dB
				0	1	1	1	14dB
				1	0	0	0	16dB
				1	0	0	1	18dB
				1	0	1	0	20dB
				1	0	1	1	22dB
				1	1	0	0	24dB
				1	1	0	1	26dB
				1	1	1	0	28dB
				1	1	1	1	30dB

GAIN = 0 to 30dB

VOLUME SELECTION

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	X	1	1	1	X	X	X	MUTE

VOLUME = 0 to 47dB/MUTE

TDA7439

DATA BYTES (continued)

BASS SELECTION

MSB							LSB	BASS
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

MIDDLE SELECTION

MSB							LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

DATA BYTES (continued)

TREBLE SELECTION

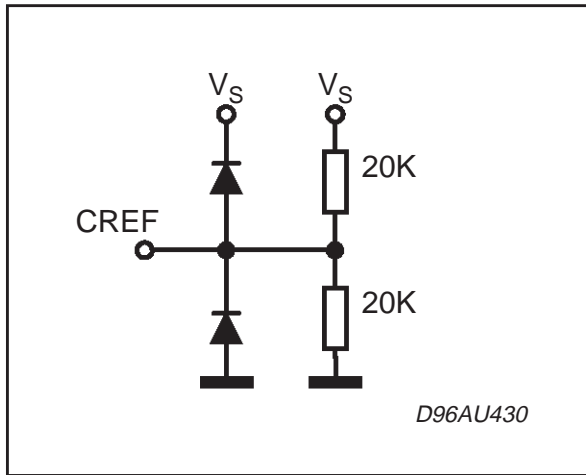
MSB							LSB	TREBLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

SPEAKER ATTENUATE SELECTION

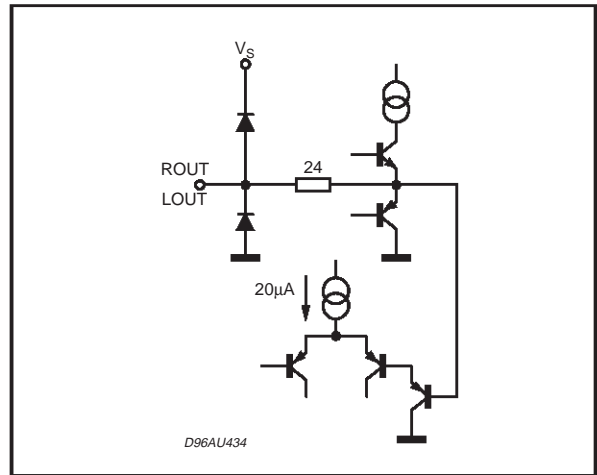
MSB							LSB	SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	MUTE

SPEAKER ATTENUATION = 0 to -79dB/MUTE

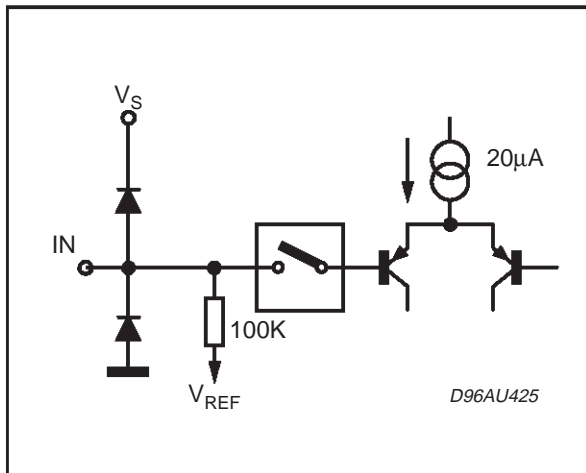
PINS: 2



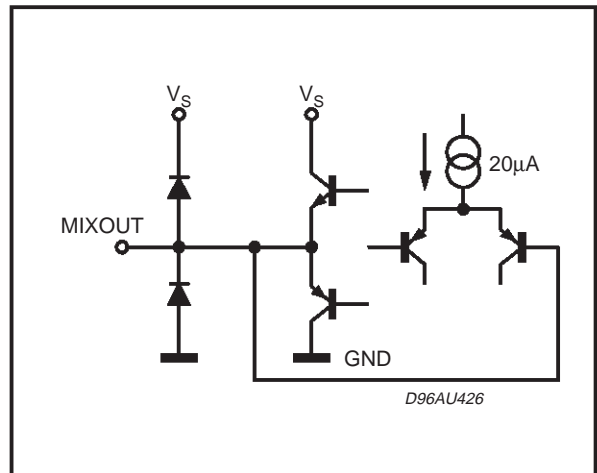
PINS: 5, 6



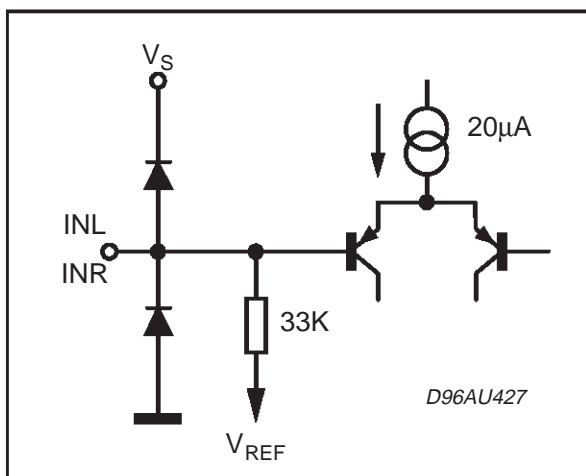
PINS: 7, 8, 9, 10, 11, 12, 13, 14



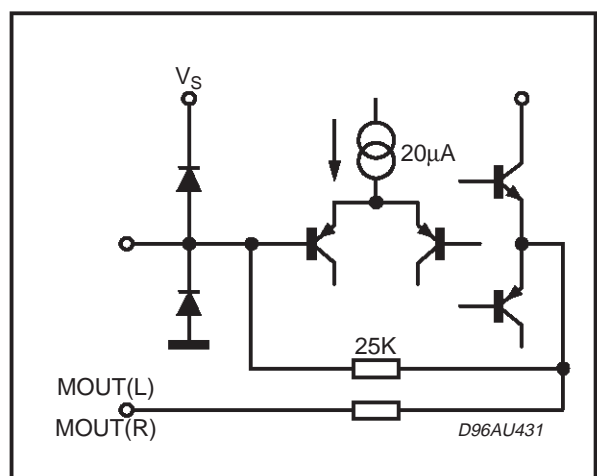
PINS: 15, 17



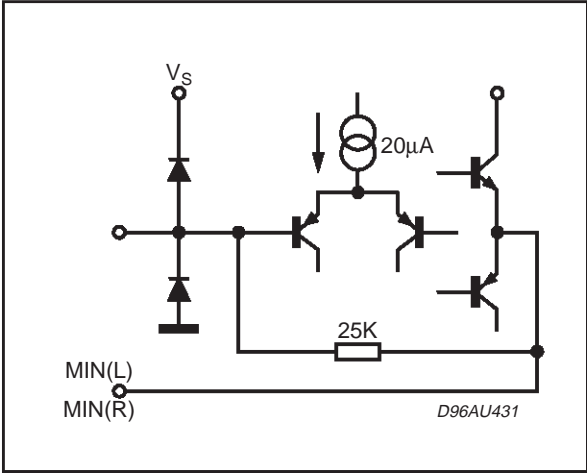
PINS: 16, 18



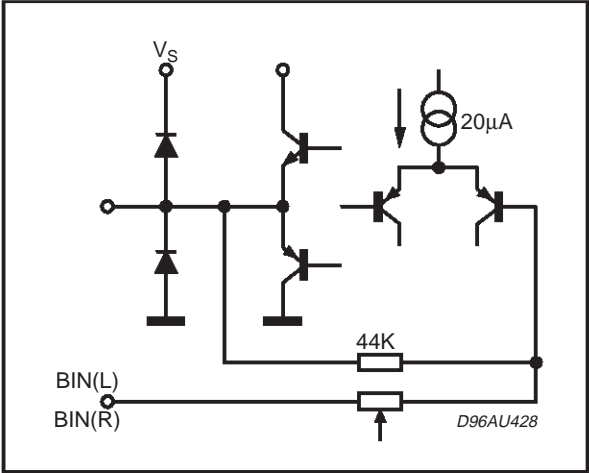
PINS: 19, 26



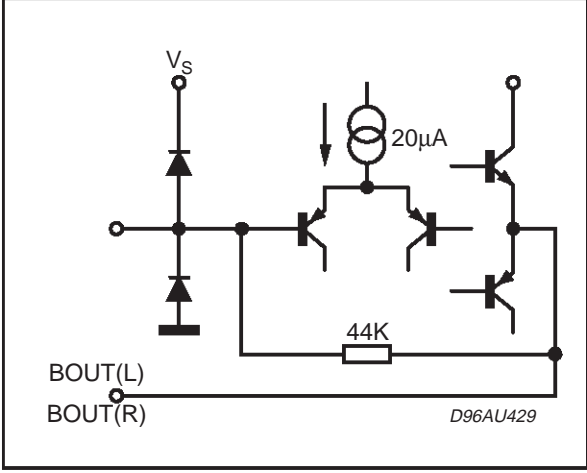
PINS: 20, 25



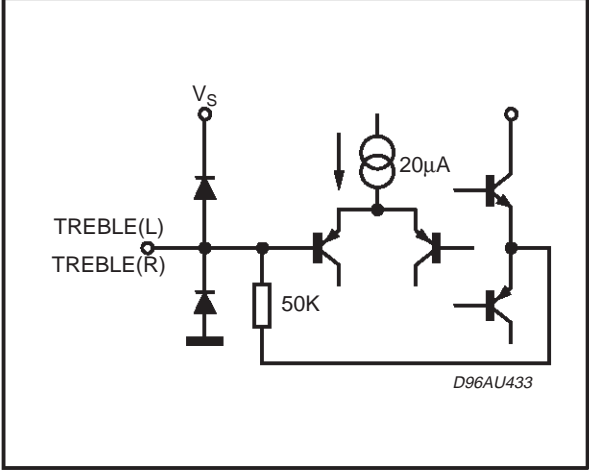
PINS: 21, 23



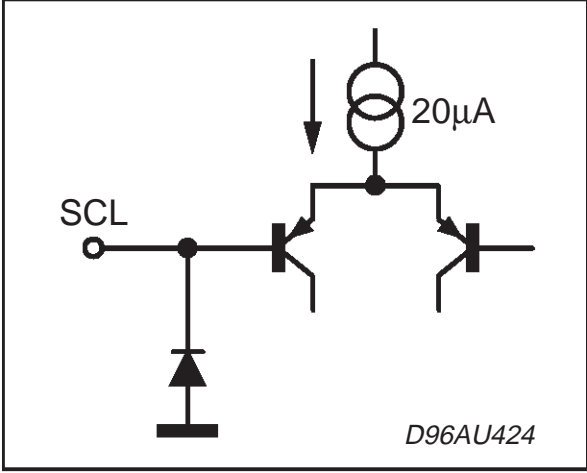
PINS: 22, 24



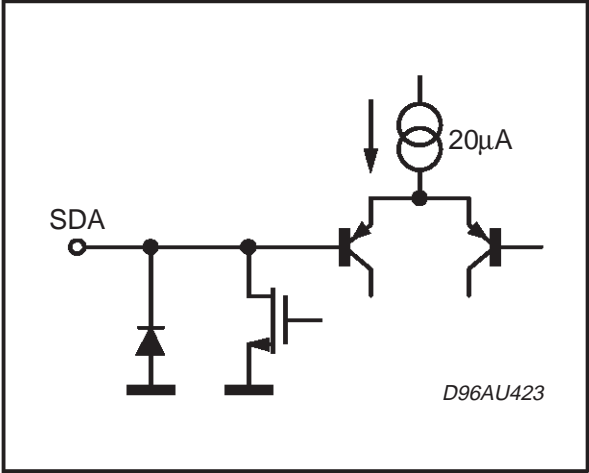
PINS: 27, 28



PINS: 29

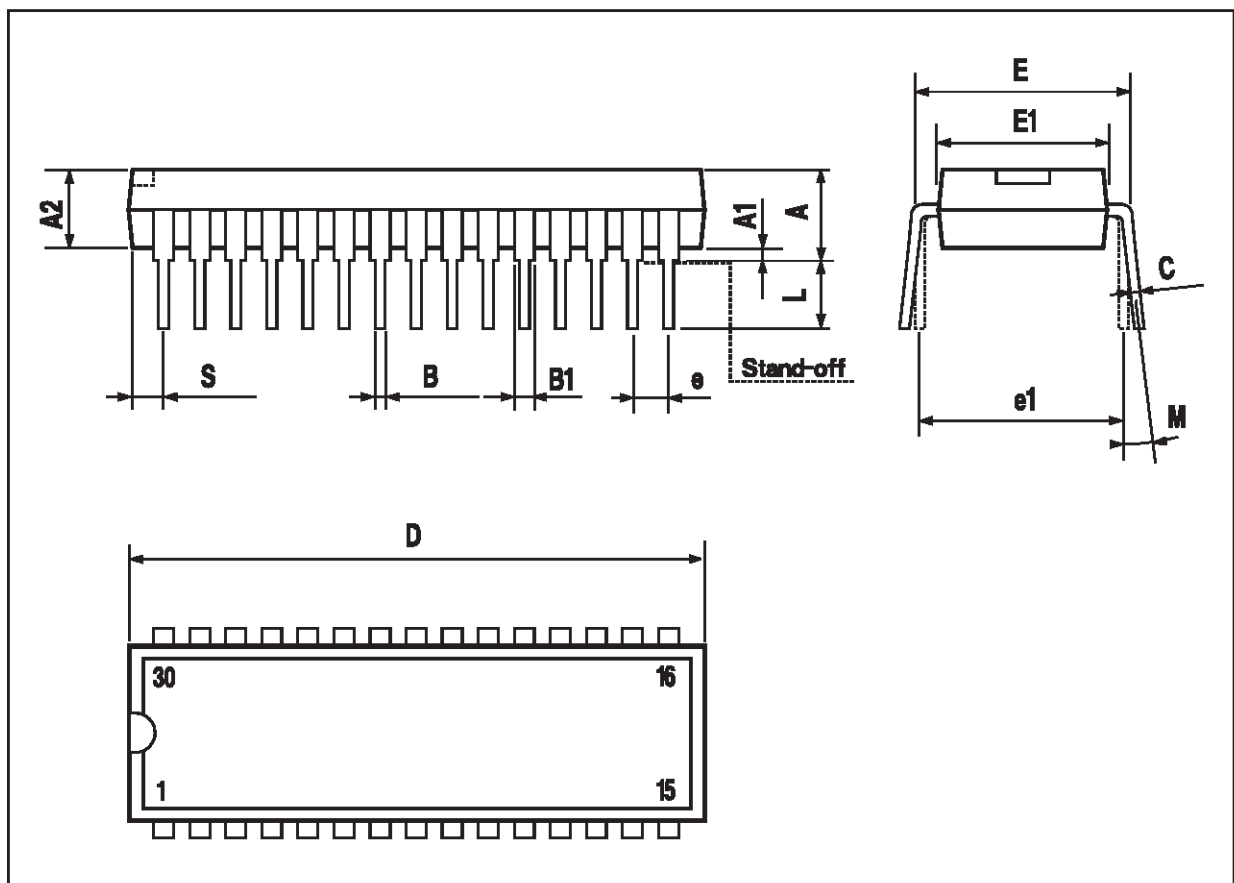


PINS: 30



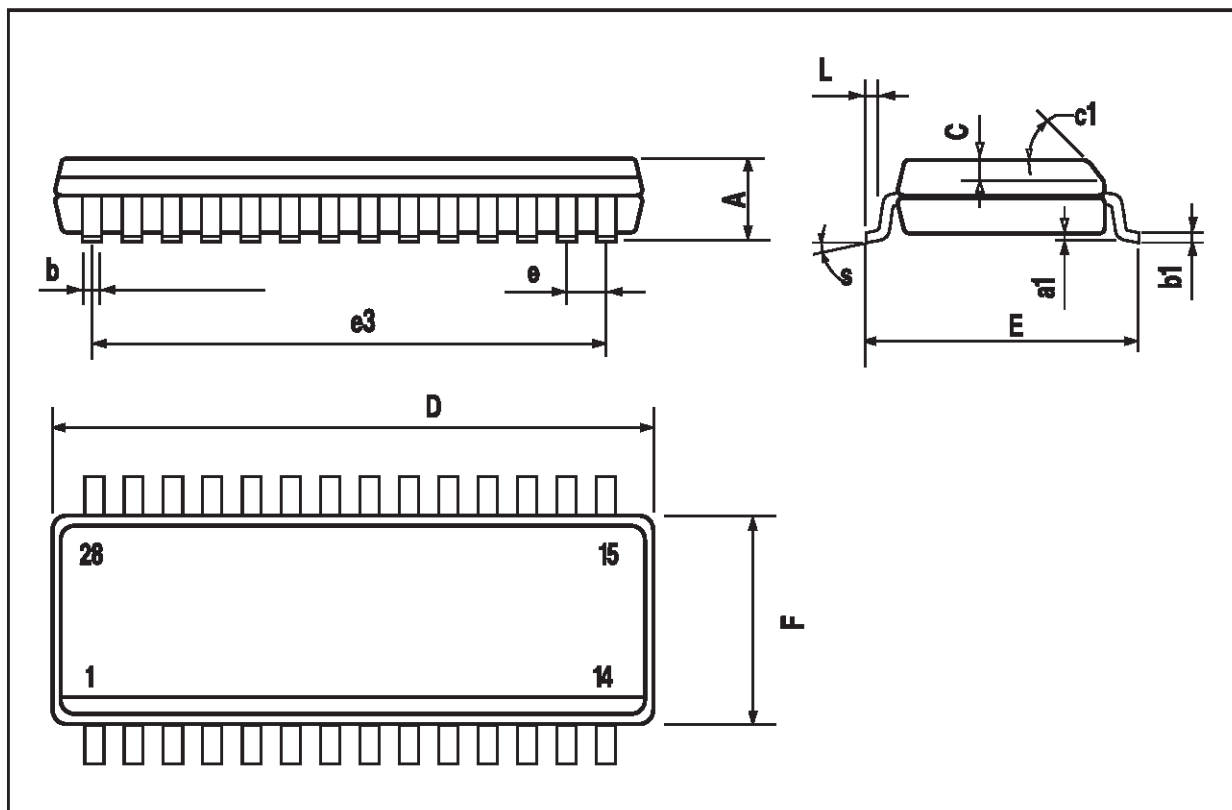
SDIP30 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.12	0.15	0.18
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	0.76	0.99	1.40	0.030	0.039	0.055
C	0.20	0.25	0.36	0.008	0.01	0.014
D	27.43	27.94	28.45	1.08	1.10	1.12
E	10.16	10.41	11.05	0.400	0.410	0.435
E1	8.38	8.64	9.40	0.330	0.340	0.370
e		1.778			0.070	
e1		10.16			0.400	
L	2.54	3.30	3.81	0.10	0.13	0.15
M	0°(min.), 15°(max.)					
S	0.31			0.012		



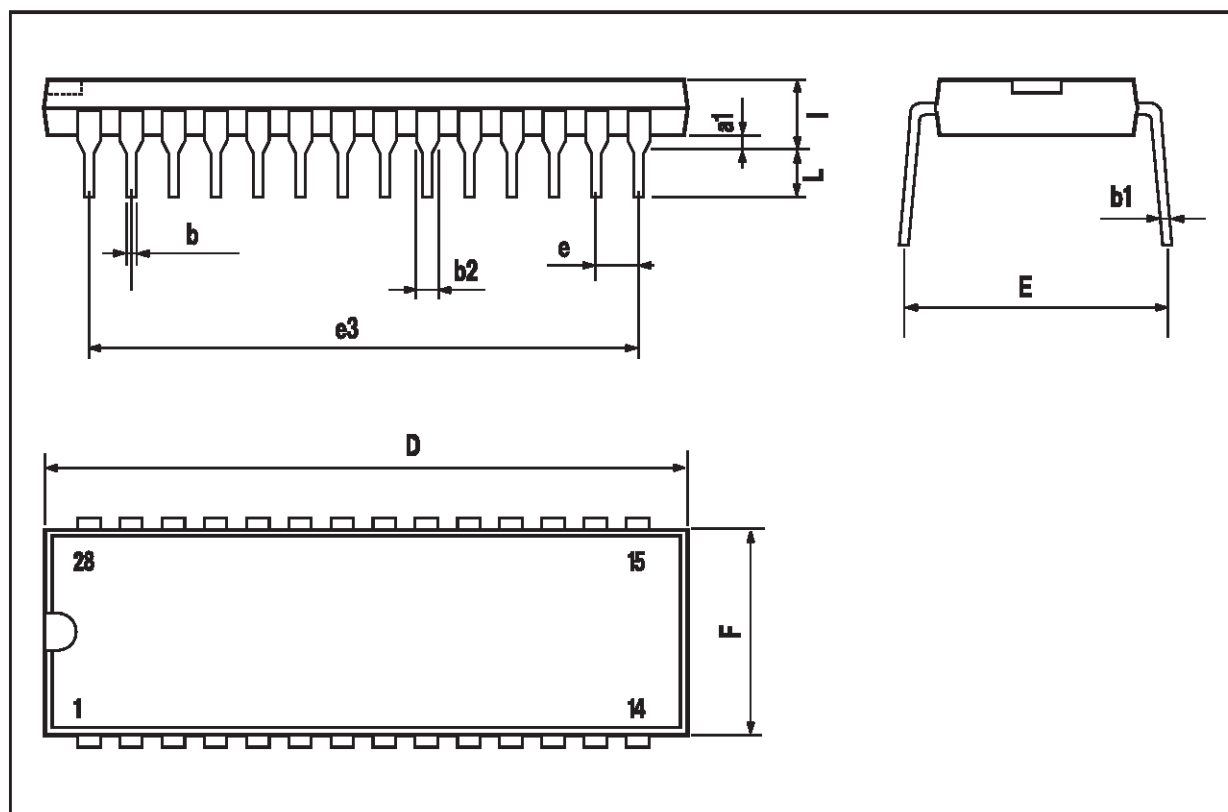
SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					



DIP28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1997 SGS-THOMSON Microelectronics – Printed in Italy – All Rights Reserved
SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.