DATA SHEET

TDA1383
DCC record/playback amplifier

Preliminary specification
File under Integrated Circuits, IC01

1995 Aug 30

Philips
Semiconductors

PHILIPS

DCC record/playback amplifier TDA1383

FEATURES

General

- Single 3 V power supply
- Low standby current consumption
- Internal voltage regulator for improved supply ripple rejection
- Double-speed DCC record and playback
- Can be applied with all generations of digital processing ICs
- All gains and settings are software controlled
- Reduced number of external components.

Record part

- Single point main data and AUX data record current setting
- Reduction of power consumption between current pulses
- Accurate temperature compensation of the record current by measuring the tape temperature
- Soft switching of record currents
- Timing compatible with TDA1319T and TDA1381H.

Playback part

- Low noise amplifiers
- Pre-equalization and anti-aliasing filters
- Automatic gain control of DCC preamplifiers
- Optional recording of auxiliary data during DCC playback
- Auxiliary data detect after record e.g. to detect end of tape or ‘head clogging’
- Two amplifiers for ACC equalization
- Control signal for ferro/chrome switches
- Mute for ACC playback
- Music search function during ACC (re)wind (to be confirmed).

GENERAL DESCRIPTION

The TDA1383 is a single-chip record and playback amplifier for a Digital Compact Cassette (DCC) tapedeck, including Analog Compact Cassette (ACC) playback functions. The device is designed to be used with the Philips DCC head, type RP410R1/15. All modes of operation and settings can be controlled by a single serial input. Application of the TDA1383 provides a small, versatile, low power and inexpensive DCC front-end.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1383H	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

QUICK REFERENCE DATA

T_{amb} = 25 °C; V_{DD1} = V_{DD2} = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1 record part		2.7	3.3	5.5	V
V_{DD1}	supply voltage 1 record part and playback part	note 1	tbf	3.3	5.5	V
V_{DD2}	supply voltage 2 playback part		2.7	3.3	5.5	V
$I_{DD1} + I_{DD2}$	supply current	DCC record mode; I_D = 100 mA	–	45	60	mA
		DCC playback mode; I_{sense} = 3 mA	–	52	68	mA
		ACC playback mode; I_{sense} = 3 mA	–	29	38	mA
I_{stb}	total standby supply current	no clock; note 1	–	–	50	µA
I_D	record current main data channels 0 to 7	see Table 1	10	–	125	mA
I_{AUX}	record/erase current auxiliary data channel		10	–	153	mA
$P_{d(av)}$	average power dissipation	DCC record mode; I_D = 100 mA	–	130	–	mW
		DCC playback mode; I_{sense} = 3 mA	–	150	–	mW
		ACC playback mode; I_{sense} = 3 mA	–	85	–	mW
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. V_{DD2} is not connected to V_{DD1} (internal voltage regulator on).

Table 1 Maximum record current as a function of V_{DD1} and record head resistance

V_{DD1}	R_{rec} = 10 Ω	R_{rec} = 6.5 Ω	R_{rec} = 4 Ω
2.7 V	75	90	110
3.3 V	90	110	125
>4 V	125	125	125

BLOCK DIAGRAM

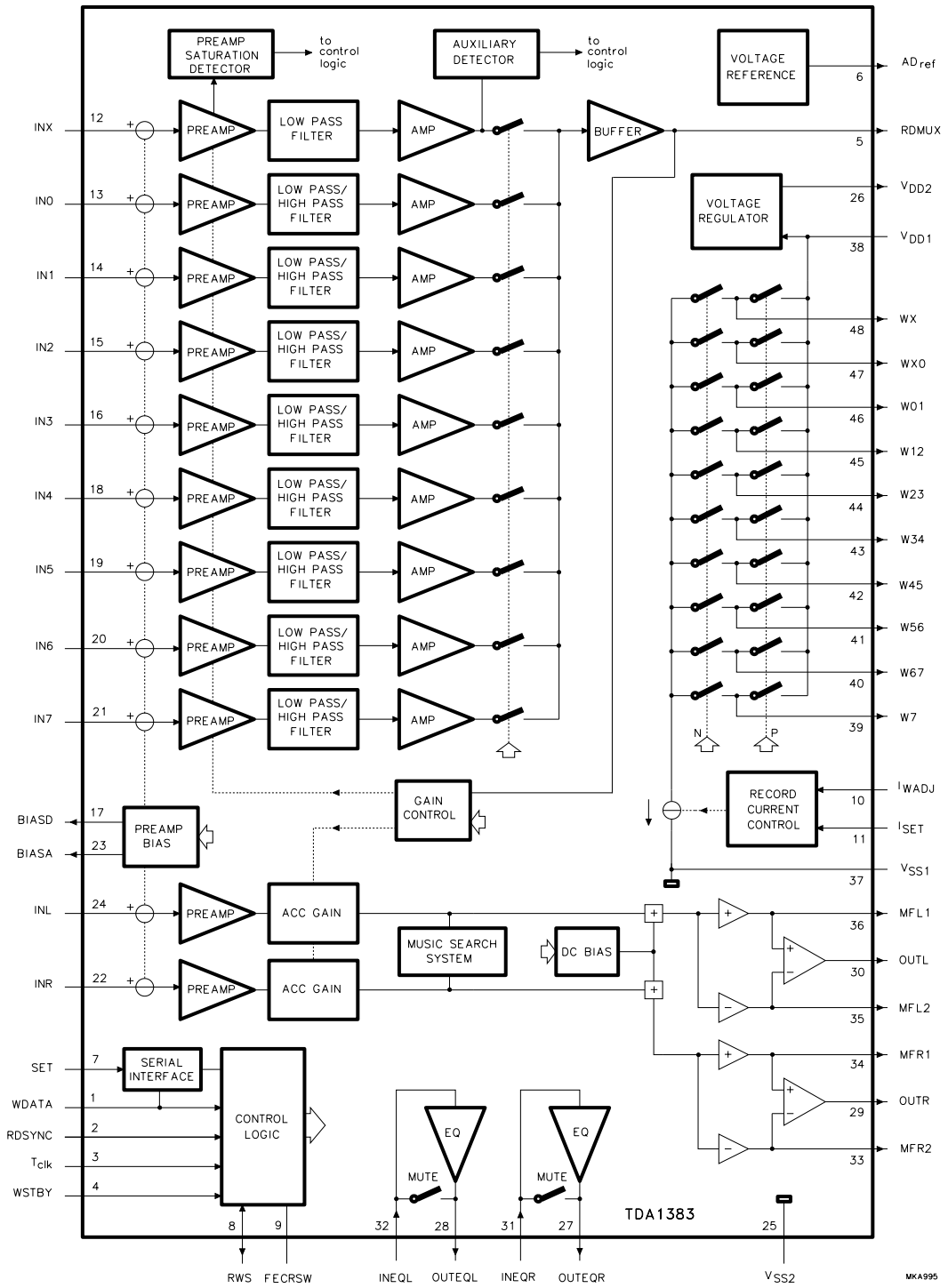


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WDATA	1	record data input/control data input
RDSYNC	2	playback sync input
T_{CLK}	3	tape clock input
WSTBY	4	record standby control input
RDMUX	5	multiplexed DCC data output
AD_{ref}	6	AD reference voltage output
SET	7	control data input
RWS	8	music search output/AUX detector output/saturation detector output/external clock input
FECRSW	9	ferro-chrome switch control signal
I_{WADJ}	10	record current adjust input
I_{SET}	11	record current set input
INX	12	auxiliary channel input
IN0	13	channel 0 input
IN1	14	channel 1 input
IN2	15	channel 2 input
IN3	16	channel 3 input
BIASD	17	DCC bias voltage output
IN4	18	channel 4 input
IN5	19	channel 5 input
IN6	20	channel 6 input
IN7	21	channel 7 input
INR	22	ACC right channel input
BIASA	23	ACC bias voltage output
INL	24	ACC left channel input
V_{SS2}	25	ground for playback part
V_{DD2}	26	supply voltage for playback part/voltage regulator output
OUTEQR	27	right channel equalization amplifier output
OUTEQL	28	left channel equalization amplifier output
OUTR	29	right channel ACC output
OUTL	30	left channel ACC output
INEQR	31	right channel equalization amplifier input
INEQL	32	left channel equalization amplifier input
MFR2	33	right channel feedback amplifier output 2
MFR1	34	right channel feedback amplifier output 1
MFL2	35	left channel feedback amplifier output 2
MFL1	36	left channel feedback amplifier output 1
V_{SS1}	37	ground for record part (substrate)
V_{DD1}	38	supply voltage for record part
W7	39	channel 7 record current output
W67	40	channel 6/7 record current output

SYMBOL	PIN	DESCRIPTION
W56	41	channel 5/6 record current output
W45	42	channel 4/5 record current output
W34	43	channel 3/4 record current output
W23	44	channel 2/3 record current output
W12	45	channel 1/2 record current output
W01	46	channel 0/1 record current output
WX0	47	channel X/0 record current output
WX	48	channel X record current output

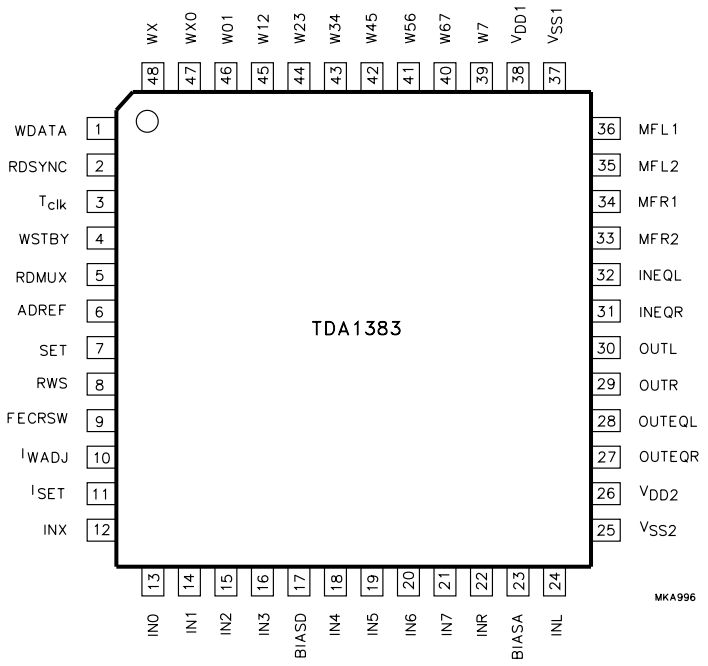


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A brief functional description of each block (see Fig.1) is given. The record part of the IC includes the record current control circuit, the current source and output switches. The DCC playback part includes nine channels, each consisting of a preamplifier, filters and an amplifier, automatic gain control and sense current (bias) circuits. Differential amplifiers with presettable gain and bias are used for ACC feedback to the head.

Modes of operation

All modes and (analog) settings are digitally controlled via the serial interface. Table 2. shows an overview of the modes of operation and the corresponding values of the control bits. For a number of bits it is allowed to deviate from this table (see description of the control bits). In the record modes additional control bits must be set, see Table 11 and Fig.6.

Table 2 Modes of operation

MODE	CONTROL BITS																		
	D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**S3**	**S2**	**S1**	**S0**	**G2**	**G1**	**G0**	**B4**	**B3**	**B2**	**B1**	**B0**
DCC playback	0	0	0	0	0	1	0	DCC sense voltage see Table 11				DCC gain see Table 12			0	(2)	–	–	–
DCC search	0	0	1	0	0	1	0								0	(2)	–	–	–
DCC playback and AUX data record	0	0	0	0	0	1	0								0	(2)	(2)	–	–
DCC playback and AUX data detection	0	1	1	0	0	1	0								0	(2)	(2)	–	–
DCC record	0	0	0	0	1	1	0	–	–	–	–	–	–	–	1	–	(2)	–	–
ACC playback	0	0	(3)	1	0	1	1	ACC sense voltage see Table 11				0	DCC gain see Table 12		DC bias voltage at ACC outputs see Table 10				
ACC search	0	1	–	0	0	1	1					–							
Standby(1)	0	0	0	0	1	1	0	–	–	–	–	–	–	–	1	–	–	–	–

Notes

1. TDAPLB and TAUPLB must be set HIGH (see Table 13).
2. 0 = normal-speed; 1 = double-speed.
3. 0 = LOW level at FECRSW output; 1 = HIGH level at FECRSW output.

Serial interface

Settings of the IC can be programmed either via the SET input pin or the WDATA input pin. When sending data via the WDATA pin, the SET pin must be held LOW, the data is then provided in the SET time-slot of the serial data word (one bit per cycle of 32 clock periods, see Fig.6). Four different control bytes are recognised (see Table 3).

The settings can be sent asynchronously at a bit-rate of $^1/_{32}f_{Tclk}$ (96 kbits/s in case of normal speed). The data transfer must be preceeded by a start bit (LOW) and end with a stop bit (HIGH), as shown in Fig.3. The SET data detector starts at the falling edge of the start bit. Each control bit is detected in the middle. After power-up at least ten stop bits (320 clock periods) must be sent in order to initialize the serial interface.

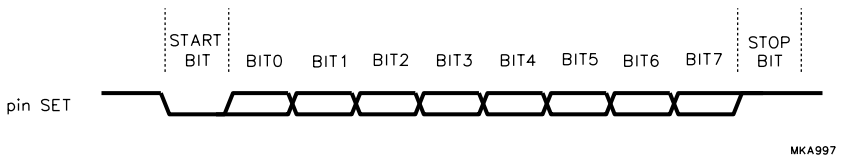


Fig.3 Timing diagram of the SET byte.

Table 3 Control bytes

CONTROL BYTE	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Byte 1	0	0	D0	D1	D2	D3	D4	D5
Byte 2	1	0	D6	–	S0	S1	S2	S3
Byte 3	0	1	–	–	–	G1	G1	G2
Byte 4	1	1	–	B0	B1	B3	B3	B4

Description of the control bits

Tables 4 to 12 describe the functions of the various control bits.

The magneto-resistive playback head (MRH) is directly connected to the IC. Bits D3 to D1 control the internal AC coupling to the MRH and DC biasing of capacitors connected between the internal amplifiers (see Fig.9). The cut-off frequencies are related to the clock frequency at T_{clk} or RWS (bit D3). Higher clock frequencies will result in higher cut-off frequencies.

Table 4 Control bit D0

D0	MODE
0	DCC playback/record
1	ACC playback

Table 5 Control bits D2 and D1

D2	D1	FUNCTION
0	0	preamp input floating, second stages normal (for testing only)
0	1	cut-off frequencies normal
1	0	cut-off frequencies high
1	1	cut-off frequencies very high (standby, fast settling)

Table 6 Control bit D3

D3	FUNCTION
0	cut-off frequencies coupled to the frequency at T_{clk} (pin 3)
1	cut-off frequencies coupled to the frequency at RWS (pin 8)

Table 7 Control bit D4

D4	DCC MODE (D0 = 0)	ACC MODE (D0 = 1)
0	AGC on	FECRSW = LOW level (pin 9)
1	AGC off, gain setting at G2, G1 and G0	FECRSW = HIGH level (pin 9)

Table 8 Detector modes and outputs

D5[1]	D6	FUNCTION IN ACC MODE (D0 = 1)	FUNCTION IN DCC MODE (D0 = 0)	PIN RWS (see Fig.9)
0	0	music search detector off	AUX detector off	control frequency input
0	1	test preamp saturation level	test preamp saturation level	saturation level detector output (HIGH when saturated)
1	0	music search detector on	AUX detector on	filtered MSS and AUX detector output
1	1	music search detector on	AUX detector on	(direct MSS and AUX detector output, for testing only)

Note

1. D3 and D5 should not be at logic 1 at the same time.

Table 9 Control bits B4 to B2

BIT	VALUE	FUNCTION IN DCC MODE (D0 = 0)	FUNCTION IN ACC MODE (D0 = 1)
B4[1]	0	playback mode on	see Table 10
	1	playback mode off	
B3	0	filters set for playback at normal-speed	
	1	filters set for playback at double-speed	
B2	0	recording at normal-speed	
	1	recording at double-speed	

Note

1. The bit B4 determines the sign of feedback bias voltage. If B4 = 0 then MFL1 and MFR1 are negative with respect to MFL2 and MFR2. If B4 = 1 then MFL1 and MFR1 are positive with respect to MFL2 and MFR2.

Table 10 Feedback conductor bias voltage settings in the ACC mode (D0 = 1, no MRH connected)

BIAS VOLTAGE BIT				TYPICAL DC BIAS VOLTAGE (mV)
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	30
0	0	1	0	60
0	0	1	1	90
0	1	0	0	120
0	1	0	1	150
0	1	1	0	180
0	1	1	1	210
1	0	0	0	240
1	0	0	1	270
1	0	1	0	300
1	0	1	1	330
1	1	0	0	360
1	1	0	1	390
1	1	1	0	420
1	1	1	1	450

Table 11 Sense voltage settings with DCC heads of 50 Ω and ACC heads of 200 Ω connected

SENSE VOLTAGE BITS(1)				TYPICAL DCC SENSE VOLTAGE (D0 = 0; B4 = 0)(2)	TYPICAL ACC SENSE VOLTAGE (D0 = 1)(2)
S3	S2	S1	S0		
0	0	0	0	50	80
0	0	0	1	80	160
0	0	1	0	110	230
0	0	1	1	140	310
0	1	0	0	170	390
0	1	0	1	200	470
0	1	1	0	230	550
0	1	1	1	260	630
1	0	0	0	290	700
1	0	0	1	320	780
1	0	1	0	350	860
1	0	1	1	380	940
1	1	0	0	410	1020
1	1	0	1	440	1090
1	1	1	0	470	1170
1	1	1	1	500	1250

Notes

1. Bits S3 to S0 control the sense voltage at the preamp input pins in both DCC and ACC mode. The sense current can be calculated from the sense voltage and the MRH resistance.
2. Depends on V_{DD1} and V_{DD2}, if no saturation occurs.

Table 12 Gain settings

GAIN SET BITS(1)			DCC MODE; AGC OFF (D0 = 0; D4 = 1)		ACC MODE (D0 = 1; D3 = 1)	
G2	G1	G0	DCC GAIN AT 50 kHz TYPICAL (dB) (PIN 5)		ACC GAIN AT 1 kHz TYPICAL (dB) (PINS 29 AND 30)	
			MAIN DATA (dB)	AUX DATA (dB)		
0	0	0	70	52.5	50.5	equalizer operational amplifier active
0	0	1	71.7	54.2	54.5	
0	1	0	72.3	55.8	58.5	
0	1	1	75	57.5	62.5	
1	0	0	76.6	59.1	50.5	equalizer operational amplifier mute
1	0	1	78.3	60.8	54.5	
1	1	0	79.9	62.4	58.5	
1	1	1	81.6	64.1	62.5	

Note

1. In the ACC mode G2 controls the mute switch over the equalizer operational amplifier (switch closed when G2 = 1).

DCC record

The TDA1383 record part is designed to drive the elements of a nine-channel integrated record head.

RECORD CURRENT CONTROL

The record current at the outputs is regulated by the current control circuit. The principle of this circuit is shown in Fig.4.

The value of the main data record current I_D can be set by applying a voltage to pin 10. This voltage can be derived from the reference voltage output at pin 6.

During AUX data record (outputs WX and WX0 active) the output current (I_X) is increased by a factor A_W. During the erase mode of the auxiliary channel (TERAUX = HIGH, see Table 2), the output current I_D is increased by a factor A_E.

RECORD MODES

Recording is controlled by the 32-bit wide serial data word which is clocked in at WDATA (pin 1). The current pulses are made available at the outputs WX to W7.

The timing sequence of the current pulses is shown in Fig.6. The operating mode of the record part can be set by the first three bits of the WDATA word. The signals TCH0 to TCH7 and TCHAUX determine the direction of the record current. When TCH_i is HIGH, the current flows as indicated in Fig.5. Otherwise current flows in the opposite direction. The principle of connection of the record head to the IC is also illustrated in Fig.5. The various modes of operation are given in Table 13. The standby mode can also be forced by setting the WSTBY input (pin 4) HIGH.

RECORD CURRENT OUTPUTS

Each channel is selected in sequence. Depending on the data bit (TCH0 to TCHAUX), the current is directed forward or reverse through the heads. The outputs that are not selected are kept floating to prevent any incorrect current flow. Current flow through a channel of the recording head is achieved by closing one of the switches P and the switch N of an adjacent channel (see Fig.1).

Table 13 DCC record modes

MODE		RECORD CURRENT		CONTROL BIT		
MAIN DATA CHANNELS	**AUX CHANNEL**	**MAIN DATA CHANNELS**	**AUX CHANNEL**	**TDAPLB(2) (DATA CHANNEL PLAYBACK)**	**TAUPLB(2) (AUX CHANNEL PLAYBACK)**	**TERAUX (AUX CHANNEL ERASE)**
record part STANDBY		off	off	1(1)	1	X(1)
record	playback	I_D	off	0(1)	1	X
record	record	I_D	$A_W \times I_D$	0	0	0
record	erase	I_D	$A_E \times I_D$	0	0	1
playback	record	off	$A_W \times I_D$	1	0	0
playback	erase	off	$A_E \times I_D$	1	0	1

Notes

1. 0 = LOW, 1 = HIGH and X = don't care.
2. When both TDAPLB and TAUPLB are HIGH, the record part of the IC is set to the standby mode. AW and AE are multiplication factors (see current control).

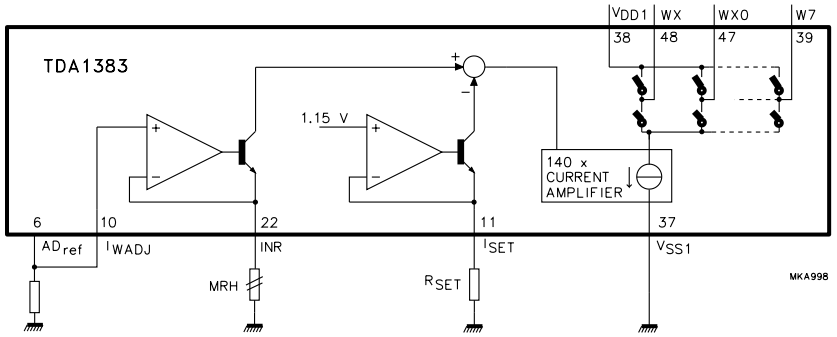


Fig.4 Principle of the record current control circuit.

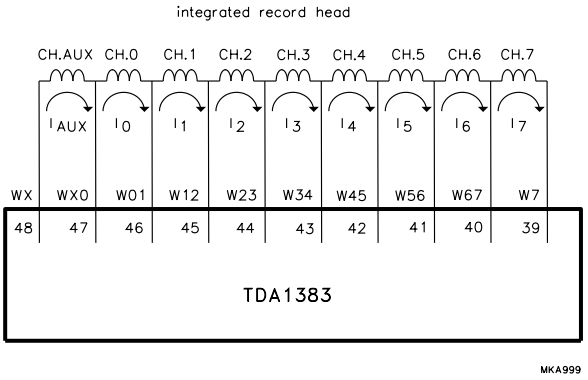
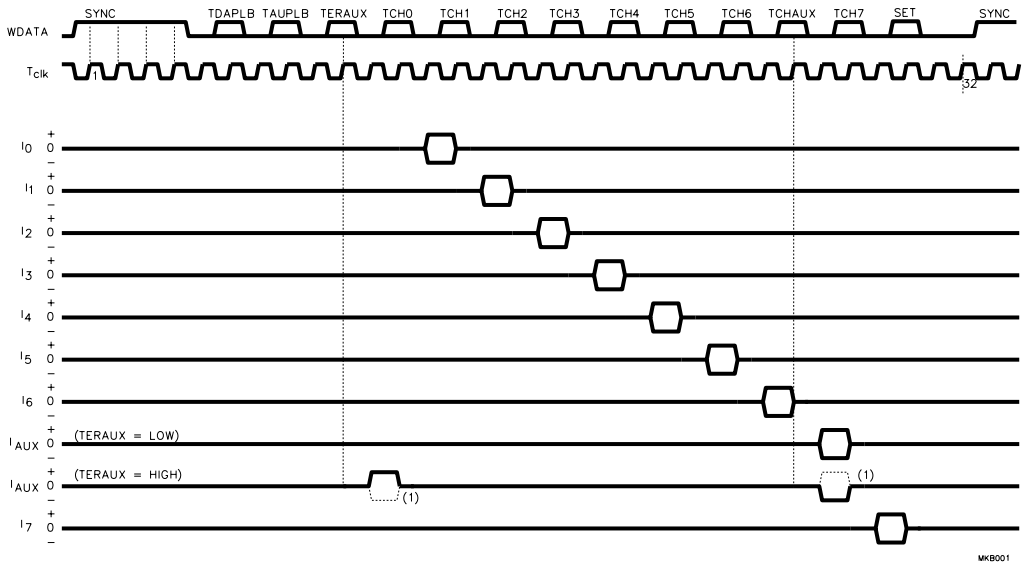


Fig.5 Definition of record currents.



(1) Erase pulses are inverted every other cycle of 32 clock pulses.

Fig.6 Timing diagram of record current pulses.

RECORD STANDBY MODE

The record circuit is set to the standby mode when TDAPLB = 1 and TAUPLB = 1 (see Table 13), or when a HIGH level is applied to WSTBY (pin 4). TDAPLB and TAUPLB will be overruled by a HIGH level on WSTBY. After a HIGH-to-LOW transition at WSTBY, the circuit will remain in the standby mode, until TDAPLB = 0 or TAUPLB = 0.

RECORD CURRENT TEMPERATURE COMPENSATION

During recording a fixed current is directed through the right channel ACC playback head. The resulting voltage over the head is temperature dependent and is used for compensation of the record current. This method ensures optimum record current at any tape temperature (see Fig.4).

DCC playback

PREAMPLIFIERS, FILTERS, MULTIPLEXERS AND OUTPUT BUFFER

The TDA1383 has nine low-noise preamplifiers, which are connected to a nine-channel magneto-resistive head (MRH). The heads must be DC-coupled to the IC. The preamplifiers will provide the necessary biasing conditions. Eight of the nine channels are for the DCC main data, the other is for the auxiliary (AUX) data. The eight main data channels have pre-equalization for frequencies from 1 to 50 kHz (1st-order highpass, –3 dB at 75 kHz), and a lowpass filter for anti-aliasing (2nd-order active, –3 dB at 120 kHz). The auxiliary data channel has a flat frequency response (from 100 Hz to 100 kHz).

A multiplexing circuit switches the nine digital channels sequentially to the output RDMUX. The AUX data is sampled during two clock periods, the eight main data channels are sampled during one clock period. The effective sample frequency is one tenth of the clock frequency at T_{clk} (see Fig.8).

DOUBLE-SPEED

The IC can be set to double speed DCC playback by setting bit B3 to logic 1 and applying a 6.144 MHz clock frequency. In this case all poles of the pre-equalization and anti-aliasing filters will be multiplied by a factor of two.

AUTOMATIC GAIN CONTROL

The DCC part is equipped with an automatic gain control circuit (AGC) which decreases the gain of the preamplifiers when the level at RDMUX exceeds a preset value. In this way an optimum voltage swing at the RDMUX output is obtained (for the ADC input of SAA2051, SAA2032, SAA2023 or SAA3323). There is a fixed relationship between decay time and recovery time of the preamplifier gain ($t_{recovery}$ is approximately equal to ten times t_{decay}). The AGC is active only in the DCC mode and can be switched off by setting D4 to logic 1. In this condition a fixed gain can be set via the serial input (see Table 12).

SENSE CURRENT

Separate, adjustable low-noise voltage sources are available at the inputs to provide the sense currents through the MRH. The voltage levels are controlled by the sense voltage bits, see Table 11. The principle of the sense voltage sources is shown in Fig.9. The value of the sense current is determined by the applied sense voltage and the MRH resistance. When the current through the MRH is too high, the input transistor will be saturated. This is detected by the saturation detector, which produces a HIGH output if V_c drops below V_b. Saturation is detected at the inputs INX and IN7. The detector output (available at pin 8) will become HIGH if one of the inputs INX or IN7 is saturated.

AUXILIARY DATA DETECTOR

A detector is available to detect the AUX signal envelope immediately after writing AUX data. This feature can be used to detect end of tape or head clogging. The output is available on pin 8 and will become HIGH if the AUX amplitude on RDMUX is above the specified level.

AUXILIARY DATA RECORD DURING DCC PLAYBACK

Provides possibility to write or erase auxiliary data.

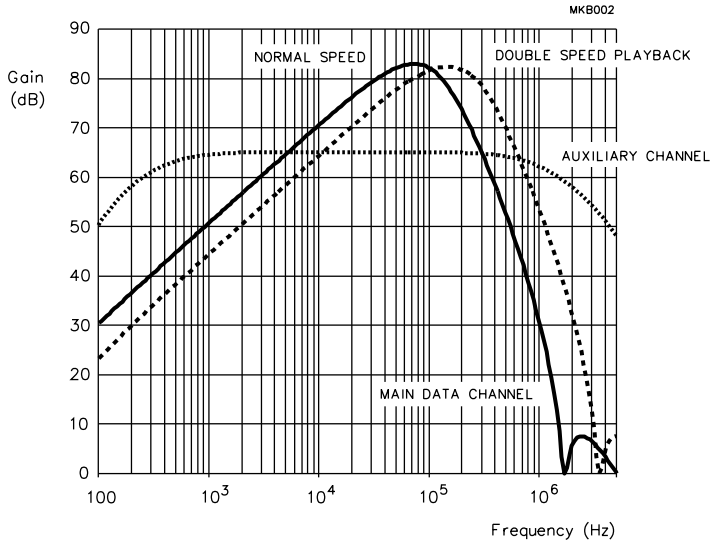


Fig.7 Typical gain of the main data and auxiliary data channel (AGC off, gain set to maximum).

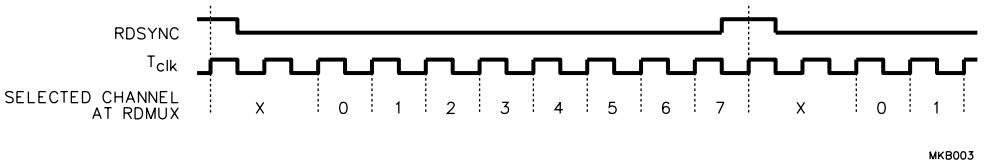


Fig.8 Timing diagram of read signals.

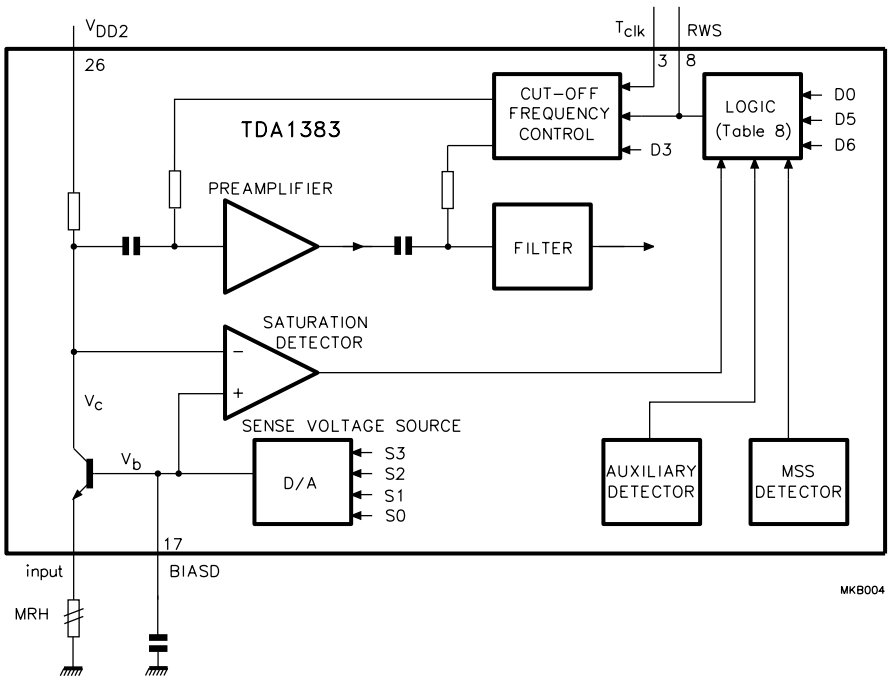


Fig.9 Principle of the sense voltage sources and the RWS output.

ACC playback

PREAMPLIFIER

The ACC playback MRH's are also directly connected to the inputs INL and INR. The preamplifier provides an adjustable sense voltage in order to bias the heads, in the same way as for the DCC inputs. Saturation is also checked on both input stages. Input signals are amplified in two stages. The gain can be set with bits G1 and G0 (see Table 12). The left and right outputs are available at pins 30 and 29.

FEEDBACK AMPLIFIERS

Separate ACC output stages are capable of driving a conductor in the MRH. This conductor will provide magnetic feedback to the head, in order to improve the linearity of the analog audio response. The left and right feedback signals are available at the outputs MFL1, MFL2 and MFR1, MFR2. The feedback amplifiers are also used for DC biasing of the feedback conductors of the MRH. A presettable DC level is added to the amplified signals before the output drivers. The DC bias voltage over the feedback conductor can be set by the control bits B4 to B0 (Table 10). This will result in a DC bias current through the head.

EQUALIZATION AMPLIFIERS

Two uncommitted operational amplifiers are available for pre-equalization of the left and right ACC signals. These amplifiers operate only during ACC playback. The non-inverting input is internally connected to a DC voltage approximately equal to 1.25 V. The equalization amplifier outputs can be muted via the serial interface, bit G2. Muting is achieved by closing an internal switch between output and inverting input. It is advised to connect the output to the input if the amplifier is not used in the application.

Fe/Cr SWITCH CONTROL SIGNAL

A control signal is available for setting the de-emphasis time constant switch from ferro to chrome (Fe/Cr) type in an application circuit. The signal is available at pin 9 and is HIGH when control bit D4 is set to logic 1.

MUSIC SEARCH SYSTEM (MSS)

This IC is equiped with a music detector which can be enabled via the serial interface (bit D5 = 1). This circuit can be used to find empty spaces between recordings during high-speed search. The ACC outputs (pins 29, 30 and 33 to 36) are muted when the music detector is active. The output of the MSS (pin 8) will go HIGH if a signal is detected. **Remark**; To be confirmed.

RWS INPUT (PIN 8)

When bit D3 is set to logic 1 pin 8 will become input for the signal whose frequency controls the cross-over frequencies of the internal AC couplings between the head and the preamplifier (used in ACC mode only).

General

INTERNAL STABILIZATION

The internal voltage regulator stabilises the supply voltage V_{DD2} of the playback part, including amplifiers, filters and voltage references. The circuit requires a small voltage drop between input and output for optimum operation.

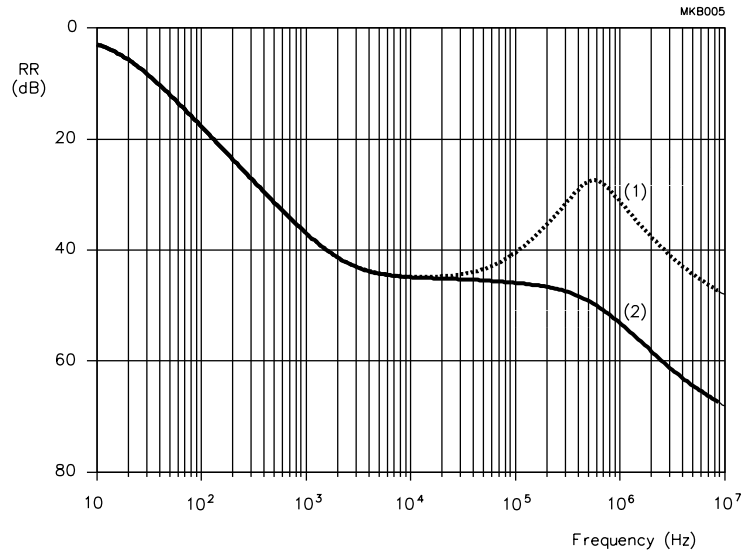
The regulator can be switched off by connecting V_{DD2} to V_{DD1}. Figure 10 shows the typical ripple rejection of the regulator. C26 is a decoupling capacitor between pin 26 and pin 25.

VOLTAGE REFERENCES

The DC output voltage AD_{ref} is derived from an internal bandgap reference voltage source. AD_{ref} (referenced to V_{SS}) can be used as reference voltage for analog-to-digital conversion of the RDMUX output. When the AGC is active the signal at RDMUX will not exceed the DC level of AD_{ref}. AD_{ref} can also be used for the adjustment of the record current (see Fig.4).

STANDBY MODE

When the IC is in the standby mode (see Tables 2 and 13), all circuits are switched off to minimize the power consumption, all record current outputs are floating, and the voltage reference output is switched off. During power-up WSTBY must be high in order to prevent unwanted record current pulses.



(1) C26 = 1 µF.
(2) C26 = 10 µF.

Fig.10 Ripple rejection of the voltage regulator (typ.).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to V_{SS1} and V_{SS2} (pins 25 and 37 externally tied together), currents positive into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD1}	supply voltage 1 record part		–0.3	+5.5	V
V_{DD2}	supply voltage 2 playback part		–0.3	+5.5	V
V_i	input voltage	V_{DD} + 0.3 < 5.5 V	–0.3	V_{DD} + 0.3	V
$I_{26,38(max)}$	maximum input current supply (pins 26 and 38)		–200	+200	mA
$I_{39\text{-}48(max)}$	maximum input current record output (pins 39 to 48)		–200	+200	mA
$I_{33\text{-}36(max)}$	maximum input current ACC feedback output (pins 33 to 36)		–80	+80	mA
$I_{n(max)}$	maximum input current remaining pins		–10	+10	mA
P_{tot}	total power dissipation		–	600	mW
T_{amb}	operating ambient temperature		–30	+85	°C
T_{stg}	storage temperature		–55	+150	°C
V_{es}	electrostatic handling	note 1	–3000	+3000	V
		note 2	–300	+300	V

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 25 Ω series resistor and a 2.5 μH series inductor.

QUALITY SPECIFICATION

In accordance with SNW-FQ-661 part E. The numbers of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9398 510 63011.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	65	K/W

CHARACTERISTICS

Voltages referenced to V_{SS} (pins 25 and 37, tied together externally); currents positive into the IC; supply voltage $V_{DD2} = V_{DD1} = 3.3$ V (pins 26 and 38); internal voltage regulator off; test circuit in accordance with Fig.12; $T_{amb} = +25$ °C; $f_{Tclk} = 3.072$ MHz; settings in accordance with Table 2; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD1}	supply voltage 1 record part, FB part and logic part		2.7	3.3	5.5	V
V_{DD1}	supply voltage 1 record part	voltage regulator used	tbf	3.3	5.5	V
V_{DD2}	supply voltage 2 playback part		2.7	3.3	5.5	V
V_{DD1}–V_{DD2}	voltage drop over regulator	voltage regulator used; $V_{DD1} = 3.3$ V	0.45	0.6	0.75	V
$I_{DD1} + I_{DD2}$	supply current	DCC record mode; $I_D = 100$ mA	–	45	60	mA
		DCC playback mode; $I_{sense} = 3$ mA	–	52	68	mA
		ACC playback mode; $I_{sense} = 3$ mA	–	33	45	mA
I_{stb}	total standby current	voltage regulator on; no clock	–	–	50	µA
$P_{d(av)}$	average power dissipation	DCC record mode; $I_D = 100$ mA	–	150	–	mW
		DCC playback mode; $I_{sense} = 3$ mA	–	170	–	mW
		ACC playback mode; $I_{sense} = 3$ mA	–	110	–	mW
AD_{ref}	reference voltage output	D0 = 0	1.9	2.0	2.15	V
DIGITAL INPUTS (PINS 1 TO 4, 7 AND 8)						
V_{IH}	HIGH level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD1}$	V
I_{LI}	input leakage current		–10	0	+10	µA
t_{su}	set-up time WDATA, RDSYNC	see Fig.11	20	–	–	ns
t_{hd}	hold time WDATA, RDSYNC	see Fig.11	20	–	–	ns
t_r	rise time of tape clock	see Fig.11	–	–	20	ns
t_f	fall time of tape clock	see Fig.11	–	–	20	ns
DIGITAL OUTPUT (PIN 8)						
V_{OH}	HIGH level output voltage	$I_o = -1$ mA	$V_{DD1} - 0.5$	–	V_{DD1}	V
V_{OL}	LOW level output voltage	$I_o = 1$ mA	0	–	0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCC record part						
I_D	recording current main data channels 0 to 7	see Table 1	10	–	125	mA
I_{AUX}	recording current auxiliary data channel		10	–	153	mA
A_W	relative AUX data record current increase with respect to I_D	I_D = 100 mA	1.0	1.2	1.4	dB
A_E	relative AUX erase current increase with respect to I_D	I_D = 100 mA	–	3.5	–	dB
ΔI_D	deviation among main data channel currents	I_D = 100 mA; note 1	–	–	0.5	dB
t_{rec}	rise time of record current pulse	I_D = 100 mA; 10% to 90%; f_{Tclk} = 6 MHz	–	36	–	ns
DCC playback part (note 2)						
V_N	preamplifier input referred noise voltage	f_i = 50 kHz; R_{source} = 50 Ω; I_{sense} = 3 mA	–	1.8	–	nV/√Hz
ΔV_N	3 × standard deviation of input referred noise voltage	f_i = 50 kHz; R_{source} = 50 Ω; I_{sense} = 3 mA	–	0.4	–	nV/√Hz
THD	preamplifier total harmonic distortion at TESTMUX (pin 9)	V_i = 0.2 mV (RMS); f_i = 9.6 kHz	–	tbf	–40	dB
G_{AUX}	auxiliary data gain at RDMUX	f_i = 9.6 kHz	62	64	66	dB
G_{50}	main data gain at RDMUX	f_i = 50 kHz	78	81	84	dB
ΔG_{10}	relative gain at 10 kHz	f_i = 10 kHz	–14	–12	–10	dB
ΔG_{300}	relative gain at 300 kHz	f_i = 300 kHz	–	–14	–	dB
G_{ds100}	main data gain at double-speed playback	f_i = 100 kHz	75	78	81	dB
ΔG_{ds20}	relative gain at 20 kHz at double-speed playback	f_i = 20 kHz	–12	–10	–8	dB
$V_{o(rms)}$	maximum output voltage at RDMUX (RMS value)	f_i = 9.6 kHz	0.5	–	–	V
$V_{DC(RDMUX)}$	DC voltage level at RDMUX		1.05	1.15	1.25	V
$\Delta V_{DC(os)}$	DC offset voltage between sampled outputs		–	–	200	mV
V_L	lower AGC detection level at RDMUX		–	0.5	–	V
V_H	upper AGC detection level at RDMUX		–	1.8	–	V
V_{hys}	hysteresis in AGC voltage detection level		–	0.15	0.25	V
AGC_{cr}	AGC range	D4 = 0	9	11	13	dB
α_{cs}	channel separation		30	–	–	dB
V_{sense}	sense voltage (INX to IN7)	R_{head} = 50 Ω	70	–	250	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{sense}	sense current (INX to IN7)	V_{sense} = maximum; no saturation	–	–	5	mA
$V_{AUXdet(M)}$	AUX detector voltage level at input INX (peak voltage)	note 3	tbf	75	tbf	mV
ACC playback part (note 4)						
V_N	preamplifier input referred noise voltage	f_i = 10 kHz; R_{head} = 200 Ω; I_{sense} = 3 mA	–	3.5	–	nV/√Hz
ΔV_N	3 × standard deviation of input referred noise voltage	f_i = 10 kHz; R_{head} = 200 Ω; I_{sense} = 3 mA	–	1	–	nV/√Hz
G_{ACC}	ACC gain at pins 29 and 30	f_i = 50 to 20 kHz	60	62.5	65	dB
$V_{o(rms)}$	maximum output voltage (RMS value) (pins 29 and 30)	f_i = 1 kHz; THD < –40 dB; RL ≥ 5 kΩ; maximum gain setting = 300	500	–	–	mV
$I_{o(rms)}$	maximum output current at FB outputs (RMS value)	f_i = 1 kHz; THD < –35 dB; $V_{DC(FB)}$ = 0; maximum gain setting = 300	25	–	–	mA
$V_{DC(FB)}$	DC bias voltage at FB outputs	no head connected; see Table 10	–450	–	+450	mV
$V_{os(FB)}$	DC offset voltage at FB outputs	$V_{DC(FB)}$ = 0	–	–	25	mV
α_{cs}	channel separation	f_i = 10 kHz	40	–	–	dB
V_{sense}	input sense voltage at INL and INR	R_{head} = 200 Ω	0.08	–	0.9	V
$I_{sense(max)}$	maximum input sense current at INL and INR		–	–	4.5	mA
V_{MSS}	music search system detector level	referenced to 500 mV (RMS) at pins 29 and 30; notes 5 and 6	–	40	–	dB
A_{mute}	equalizer output attenuation during mute	f_i = 1 kHz	30	35	–	dB
$V_{oEQ(rms)}$	maximum output voltage at pins 27 and 28 (RMS value)	f_i = 1 kHz; THD < –40 dB; R_L ≥ 2.5 kΩ	0.5	–	–	V

Notes

1. Defined as 20log ($I_{D(max)}/I_{D(min)}$) for channels 0 to 7.
2. DCC mode; AGC off; gain set to maximum (D0 = 0; D4 = 1; G2 = G1 = G0 = 1).
3. Pin 8 will become HIGH if AUX data with frequency above 1 kHz is above the specified level for longer than 10 ms.
4. ACC playback mode; D0 = 1; ACC gain set to maximum (G1 = G0 = 1); f_i = 48 kHz at pin 8; bit D3 = 1; unless otherwise specified.
5. D3 = 0; D5 = 1; D6 = 0; pin 8 will become HIGH when both channels are below this level for more than 10 ms.
6. All references to the music search system has the status ‘to be confirmed’.

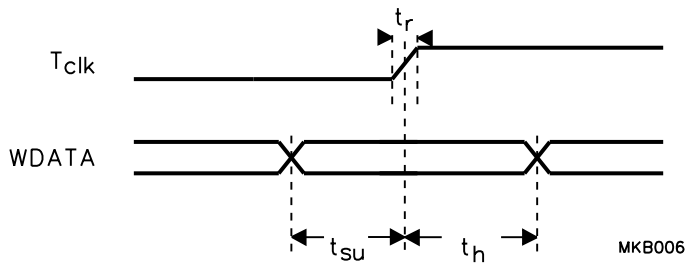


Fig.11 Timing relationship between the edges of T_{clk} and WDATA.

TEST AND APPLICATION INFORMATION

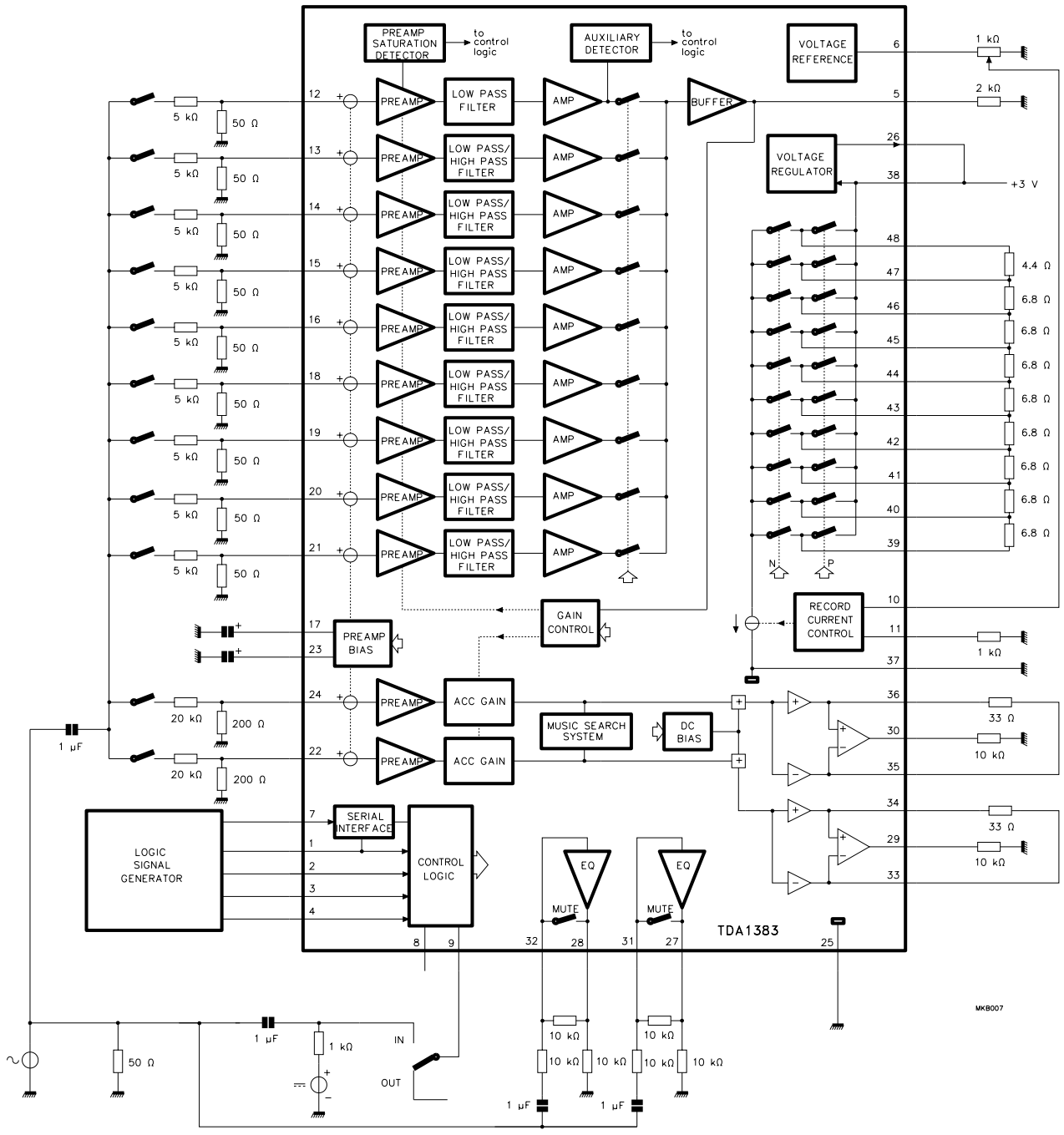


Fig.12 Test circuit.

The TDA1383 can be set to the test mode by setting control bit D6 to logic 1. In the test mode the FECRSW output (pin 9) is connected to a test multiplexer which allows the low-pass filter output of each DCC channel to be monitored (see Fig.13). The test multiplexer runs in phase with the channel output multiplexer.

When a DC level is applied to pin 9, the emitter follower can be turned off, allowing input to the high-pass filter. The DC level to be applied must be 0.7 V higher than the measured DC level of the selected channel.

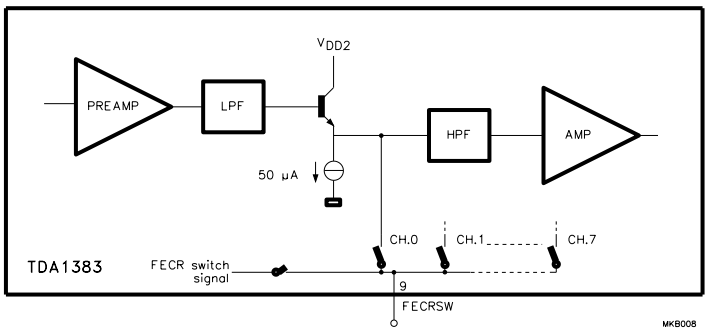
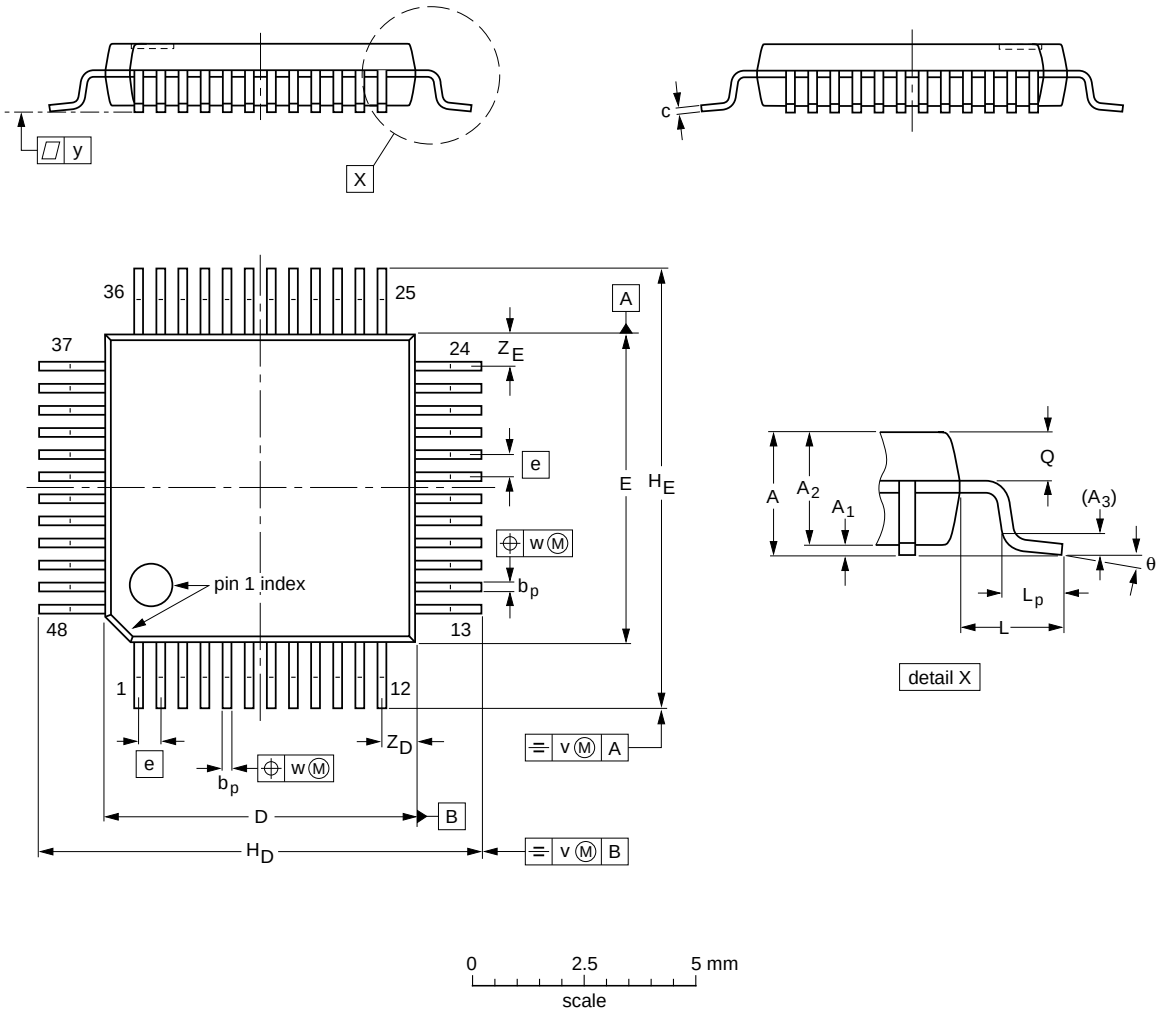


Fig.13 Principle of the TESTMUX input/output.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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