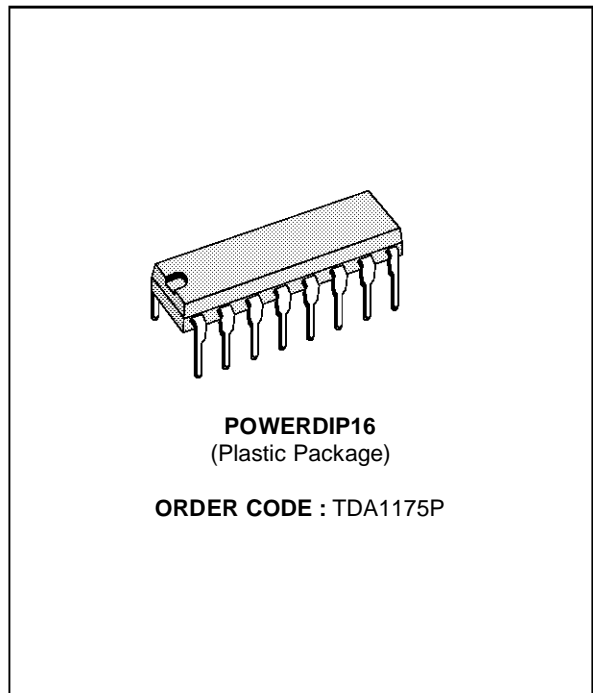


LOW-NOISE VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS
- ESD PROTECTED

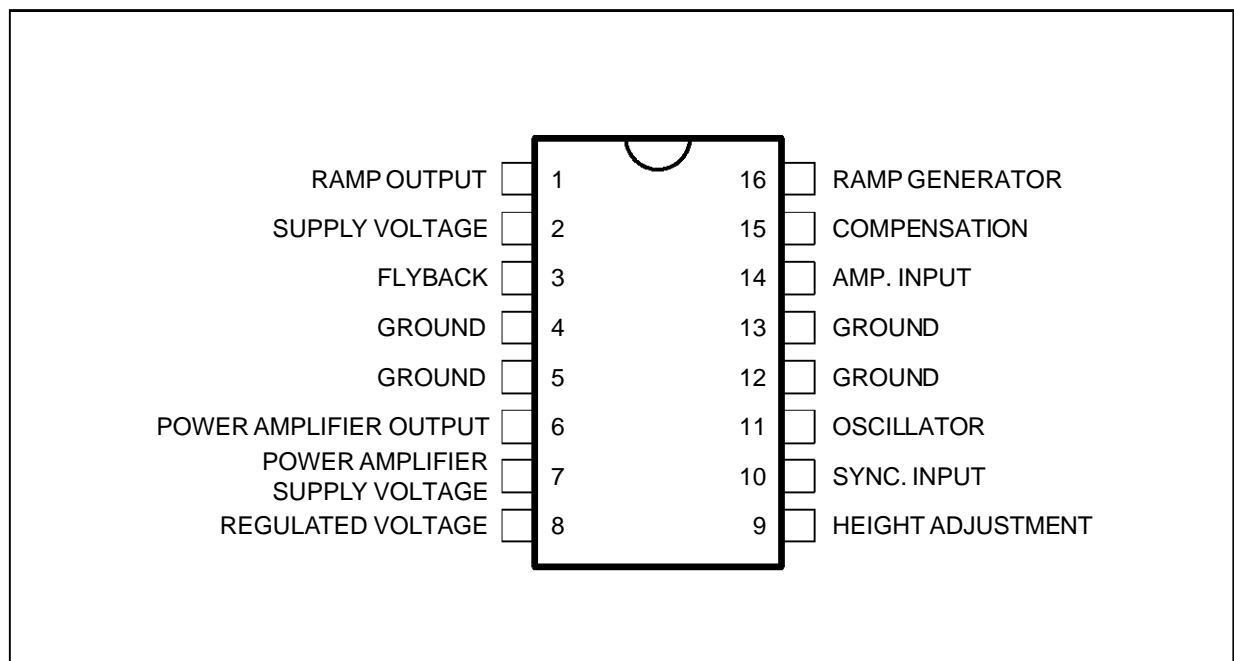


DESCRIPTION

The TDA1175P is a monolithic integrated circuit in POWERDIP16 plastic package. It is intended for use in black and white and colour TV receivers. Low-noise makes this device particularly suitable for use in monitors.

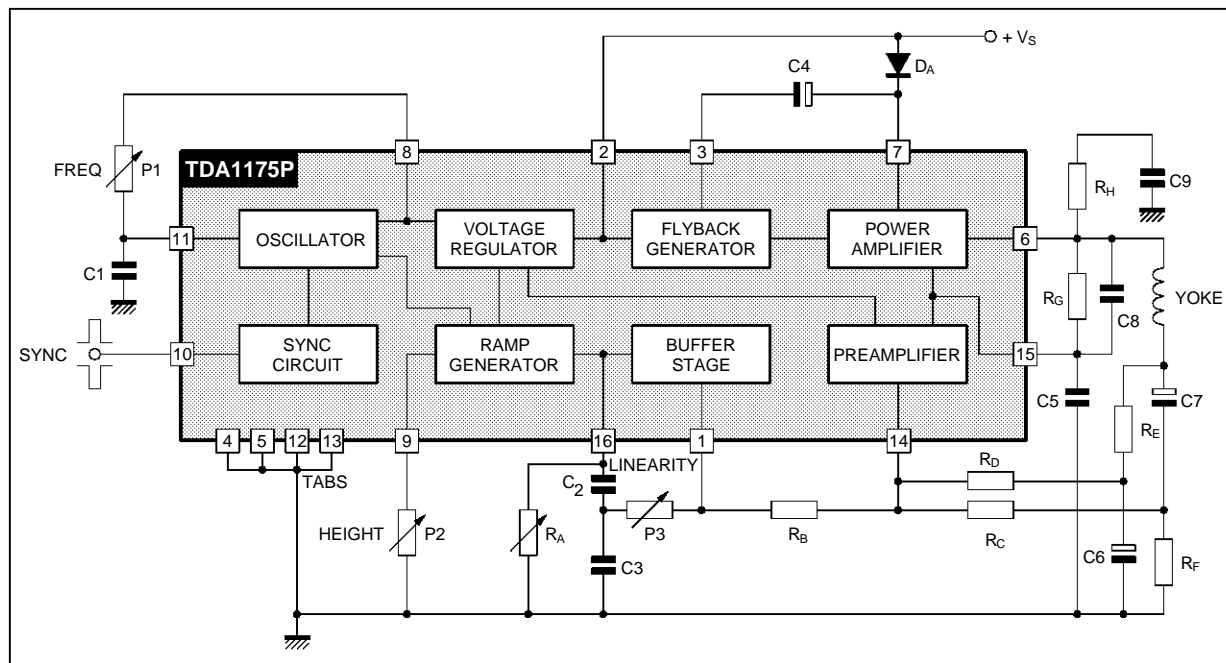
The functions incorporated are : synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

PIN CONNECTIONS



1175P-01 LEPS

BLOCK DIAGRAM



1175P-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage at Pin 2	35	V
V_6, V_7	Flyback Peak Voltage	60	V
V_{14}	Power Amplifier Input Voltage	+ 10 - 0.5	V
I_o	Output Peak Current (non repetitive) at $t = 2ms$	2	A
I_o	Output Peak Current at $f = 50Hz, t \leq 10\mu s$	2.5	A
I_o	Output Peak Current at $f = 50Hz, t > 10\mu s$	1.5	A
I_3	Pin 3 DC Current at $V_6 < V_2$	100	mA
I_3	Pin 3 Peak to Peak Flyback Current for $f = 50Hz, t_{fly} \leq 1.5ms$	1.8	A
I_{10}	Pin 10 Current	± 20	mA
P_{tot}	Power Dissipation : at $T_{tab} = 90^\circ C$ at $T_{amb} = 70^\circ C$ (free air) (1)	4.3 1	W
T_{stg}, T_j	Storage and Junction Temperature	- 40, + 150	$^\circ C$

1175P-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th(j-tab)}$	Thermal Resistance Junction-pin	Max. 12	$^\circ C/W$
$R_{th(j-amb)}$	Thermal Resistance Junction-ambient	Max. 80	$^\circ C/W^{(1)}$

(1) Obtained with tabs soldered to printed circuit with minimized copper area.

1175P-02.TBL

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS (Refer to the test circuits, $V_S = 35\text{V}$)							
I_2	Pin 2 Quiescent Current	$I_3 = 0$		7	14	mA	1b
I_7	Pin 7 Quiescent Current	$I_6 = 0$		8	17	mA	1b
$-I_{11}$	Oscillator Bias Current	$V_{11} = 1\text{V}$		0.1	1	μA	1a
$-I_{14}$	Amplifier Input Bias Current	$V_{14} = 1\text{V}$		1	10	μA	1b
$-I_{16}$	Ramp Generator Bias Current	$V_{16} = 0$		0.02	0.3	μA	1a
$-I_{16}$	Ramp Generator Current	$I_9 = 20\mu\text{A}$, $V_{16} = 0$	18.5	20	21.5	μA	1b
$\frac{\Delta I_{16}}{I_{16}}$	Ramp Generator Non-linearity	$\Delta V_{16} = 0$ to 12V , $I_9 = 20\mu\text{A}$		0.2	1	%	1b
V_S	Supply Voltage Range		10		35	V	
V_1	Pin 1 Saturation Voltage to Ground	$I_1 = 1\text{mA}$		1	1.4	V	
V_3	Pin 3 Saturation Voltage to Ground	$I_3 = 10\text{mA}$		1.5	2.5	V	1a
V_6	Quiescent output Voltage	$V_S = 10\text{V}$, $R_1 = 1\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ $V_S = 35\text{V}$, $R_1 = 3\text{k}\Omega$, $R_2 = 1\text{k}\Omega$	4.1 8.2	4.4 8.8	4.7 9.4	V V	1a 1a
V_{6L}	Output Saturation Voltage to Ground	$-I_6 = 0.1\text{A}$ $-I_6 = 0.8\text{A}$		0.9 1.8	1.2 2.2	V v	1c 1c
V_{6H}	Output Saturation Voltage to Supply	$I_6 = 0.1\text{A}$ $I_6 = 0.8\text{A}$		1.4 2.8	2.1 3.1	V V	1d 1d
V_8	Regulated Voltage at Pin 8		6.5	6.7	6.9	V	1b
V_9	Regulated Voltage at Pin 9	$I_9 = 20\mu\text{A}$	6.6	6.8	7	V	1b
$\frac{ \Delta V_8 }{\Delta V_S}$, $\frac{ \Delta V_9 }{\Delta V_S}$	Regulated Voltage Drift with Supply Voltage	$\Delta V_S = 10$ to 35V		1	2	mV/V	1b
V_{14}	Amplifier Input Reference Voltage	$V_{10} \leq 0.4\text{V}$	2.20	2.27	2.35	V	

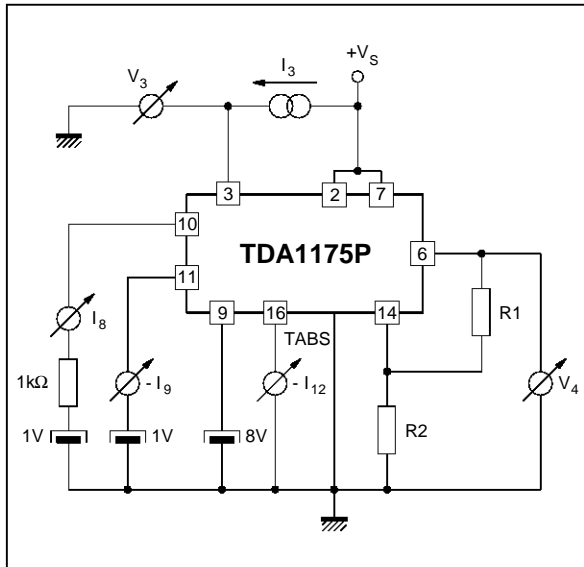
AC CHARACTERISTICS (Refer to the AC test circuit, $V_S = 22\text{V}$, $f = 50\text{Hz}$)

I_S	Supply Current	$I_Y = 1\text{A}_{PP}$		140		mA	2
I_{10}	Sync. Input Current (positive or negative)		0.5		2	mA	2
V_6	Flyback Voltage	$I_Y = 1\text{A}_{PP}$		45		V	2
t_{fly}	Flyback Time	$I_Y = 1\text{A}_{PP}$		0.7		ms	2
V_{ON}	Peak to Peak Output Noise	Pin 11 Connected to GND		18	30	mVpp	2
f_o	Free Running Frequency	$(P1 + R1) = 300\text{k}\Omega$ $C9 = 0.1\mu\text{F}$	36	43.5		Hz	2
f_{OPER}	Operating Frequency Range		10		120	Hz	2
Δf	Synchronization Range	$I_{10} = 0.5\text{mA}$, $C9 = 0.1\mu\text{F}$ $(P1+R1) = 300\text{k}\Omega$	14			Hz	2
$\frac{\Delta f}{\Delta V_S}$	Frequency Drift with Supply Voltage	$V_S = 10$ to 35V		0.005		Hz/V	2
$\frac{ \Delta f }{\Delta T_{ab}}$	Frequency Drift with tab Temperature	$T_{tab} = 40$ to 120°C		0.01		Hz/ $^{\circ}\text{C}$	2

1175P-03.TBL

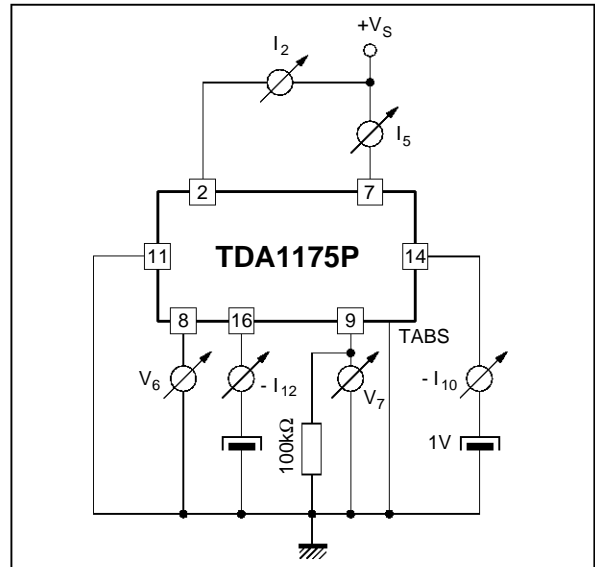
Figure 1 : DC Test Circuits

Figure 1a



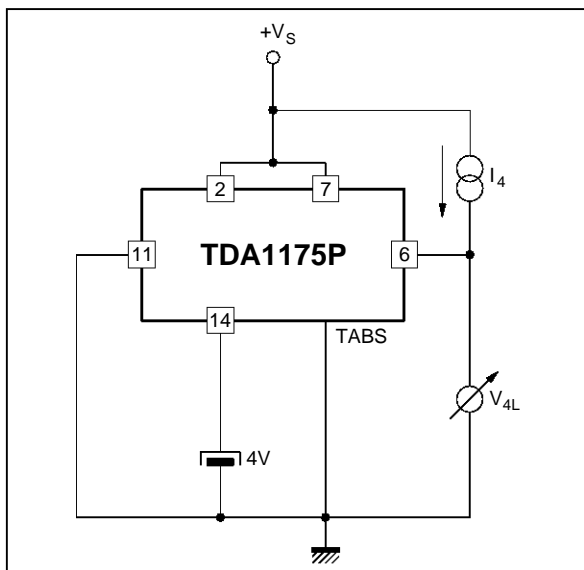
1175P-03.EPS

Figure 1b



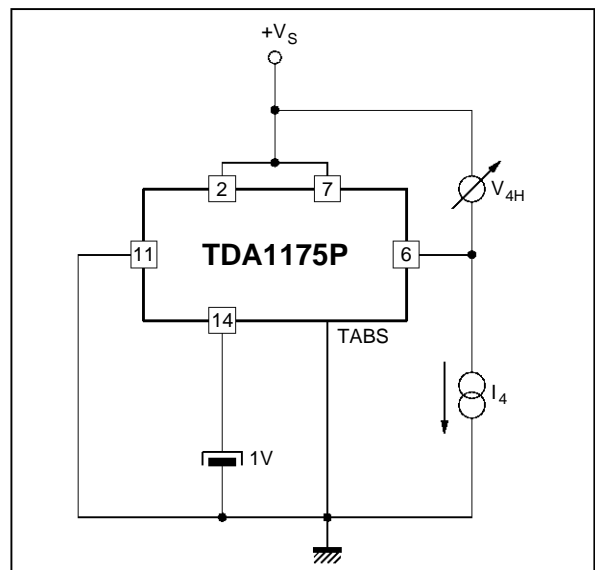
1175P-04.EPS

Figure 1c



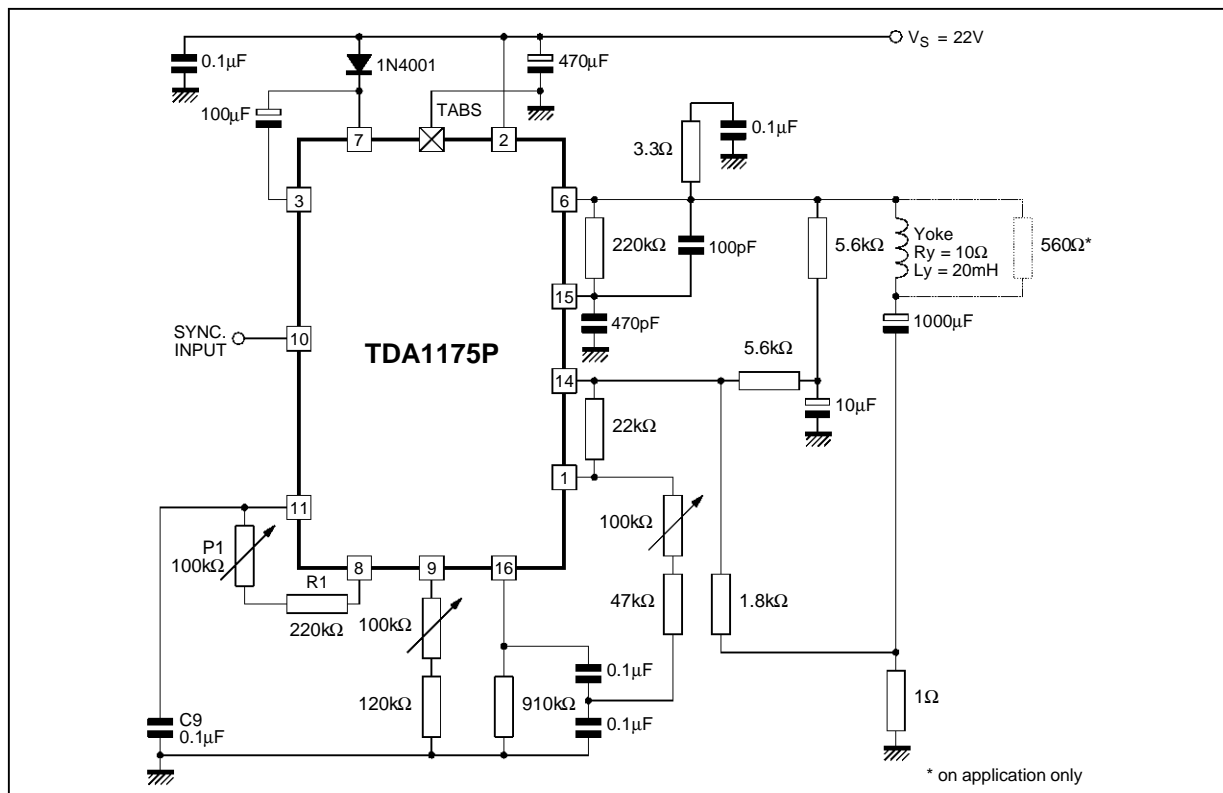
1175P-05.EPS

Figure 1d



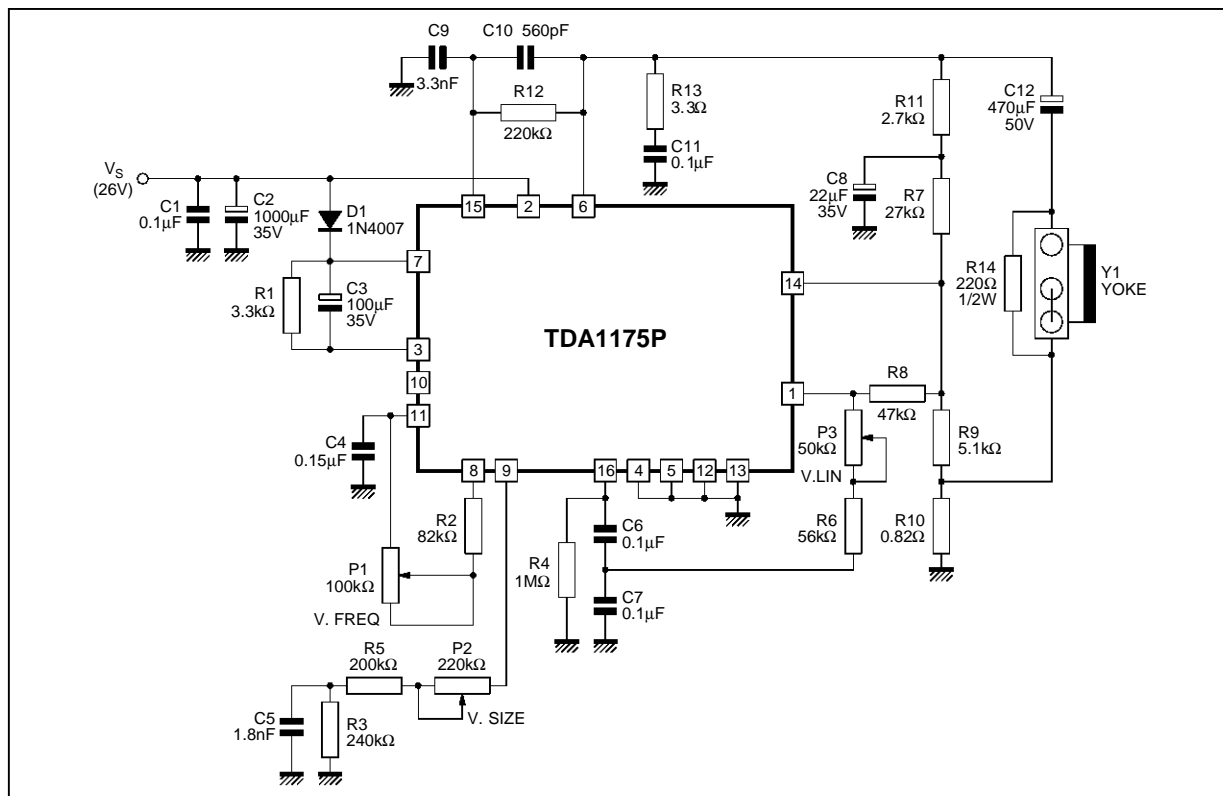
1175P-06.EPS

Figure 2 : AC Test and Application Circuit for Large Screen B/W TV Set $10\Omega/20mH/1A_{PP}$



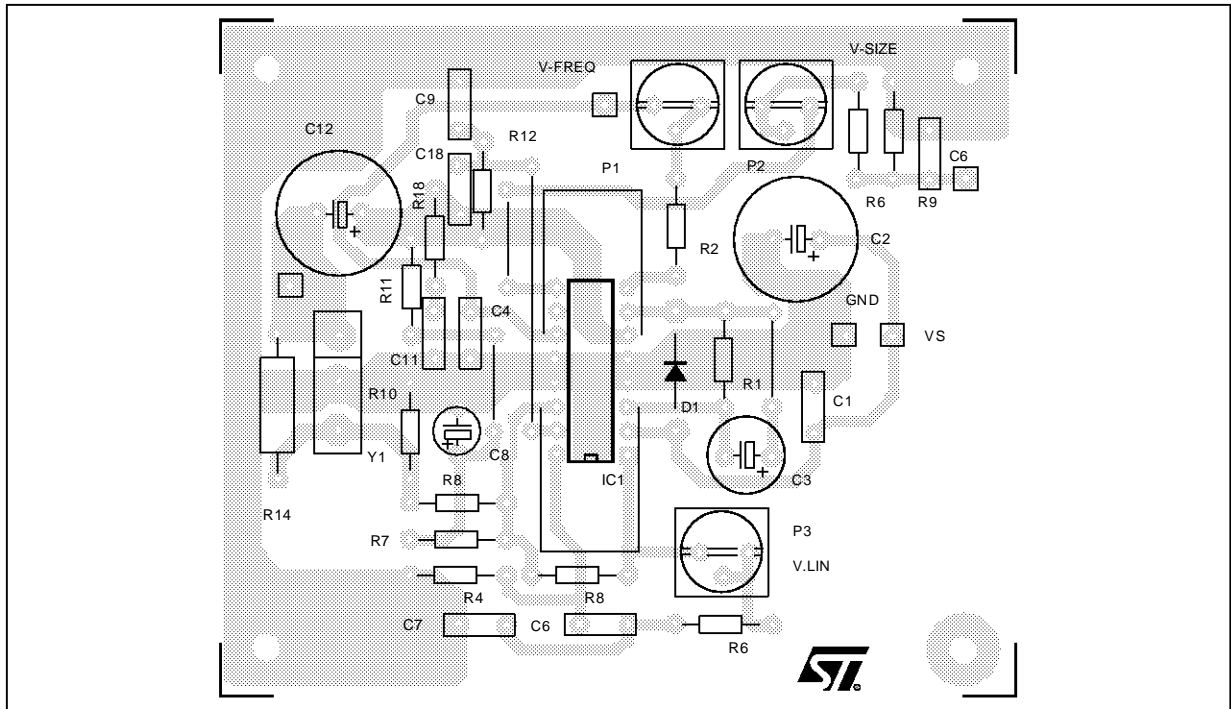
1175P-07.EPS

Figure 3 : Typical Application Circuit for VGA Monitor ($R_Y = 10\Omega$, $L_Y = 20mH$, $I_Y = 0.8A_{PP}$)



1175P-08.EPS

Figure 4 : P.C. Board and Components Layout of the Circuit of Figure 3 (1:1 scale)



1175P-09.EPS

BILL OF MATERIAL

Item	Qty	Reference	Part
1	4	C1, C6, C7, C11	0.1μF
2	1	C2	1000μF 35V
3	1	C3	100μF 35V
4	1	C4	0.15μF
5	1	C5	1.8nF
6	1	C8	22μF 35V
7	1	C9	3.3nF
8	1	C10	560pF
9	1	C12	470μF 50V
10	1	D1	1N4007
11	1	IC1	TDA1175P
12	1	P1	100kΩ POT
13	1	P2	220kΩ POT
14	1	P3	50kΩPOT
15	1	R1	3.3kΩ

Item	Qty	Reference	Part
16	1	R2	82kΩ
17	1	R3	240kΩ
18	1	R4	1MΩ
19	1	R5	200kΩ
20	1	R6	56kΩ
21	1	R7	27kΩ
22	1	R8	47kΩ
23	1	R9	5.1kΩ
24	1	R10	0.82Ω
25	1	R11	2.7kΩ
26	1	R12	220kΩ
27	1	R13	3.3Ω
28	1	R14	220Ω 1/2W
29	1	Y1	YOKE

1175P-04.TBL

MOUNTING INSTRUCTION

The $R_{th(j-a)}$ can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Figure 5) or to an external heatsink (Figure 6).

The diagram of Figure 7 shows the maximum dissippable power P_{tot} and the $R_{th(j-a)}$ as a function of the side "l" of two equal square copper areas

Figure 5 : Example of P.C. Board Copper Area

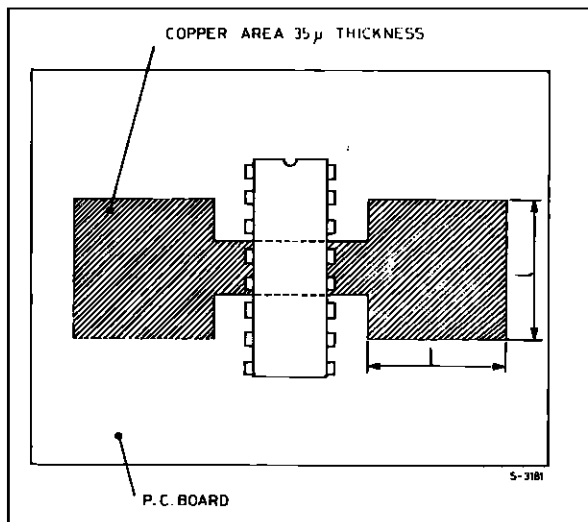
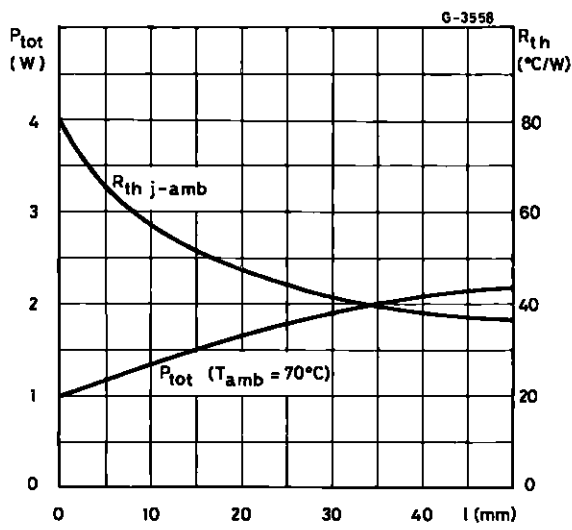


Figure 7 : Maximum Power Dissipation and Junction-ambient Thermal Resistance versus "l"



having a thickness of 35μ (1.4 mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 6 : External Heatsink Mounting Example

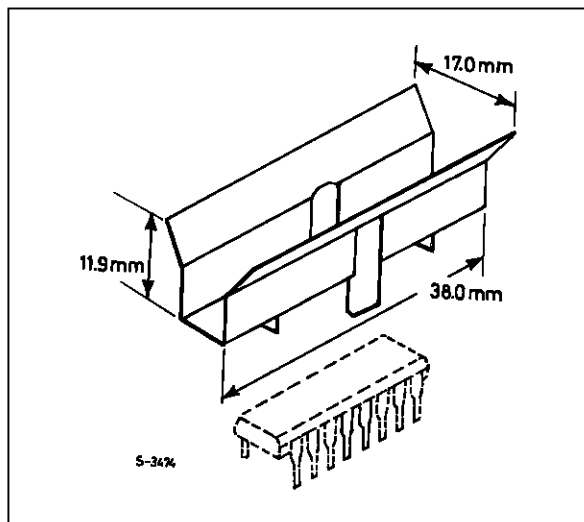
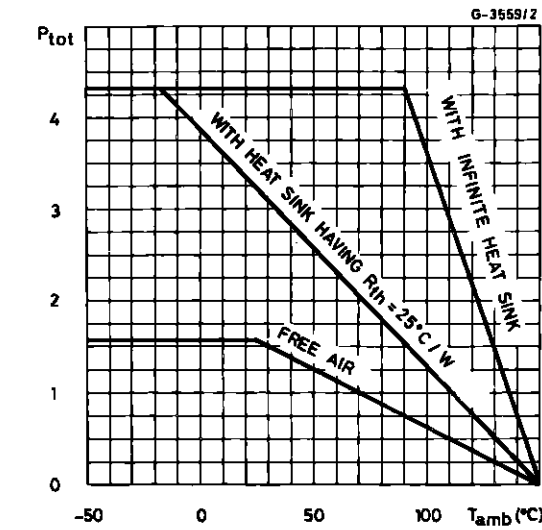
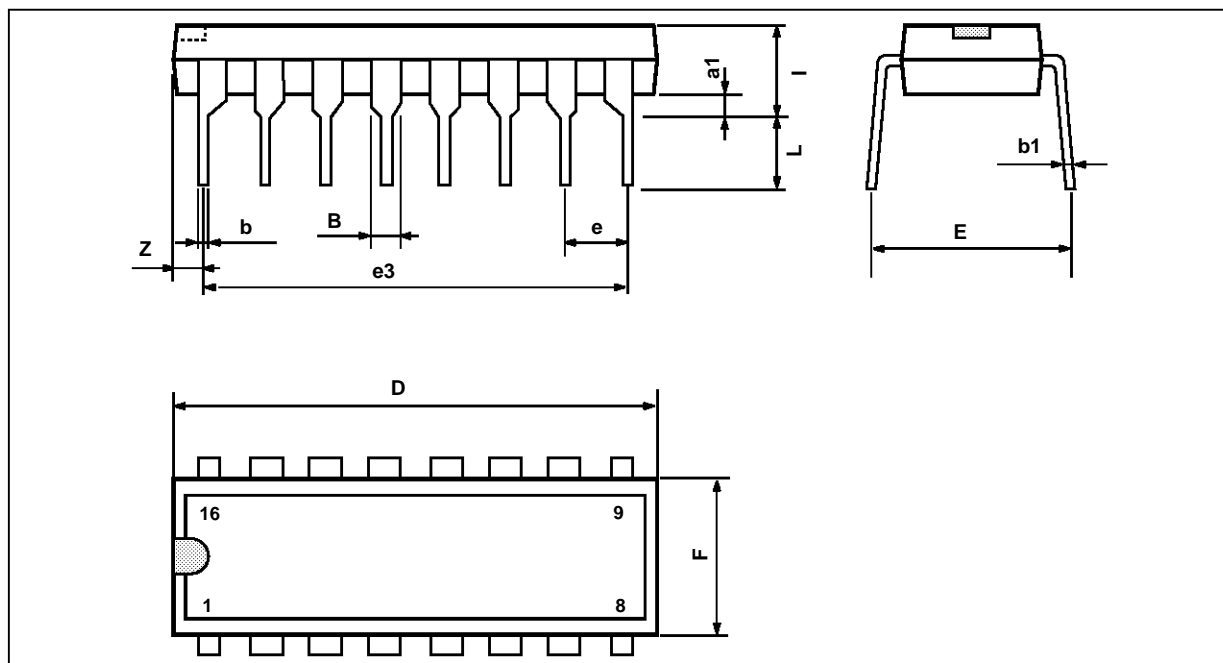


Figure 8 : Maximum Allowable Power Dissipation versus Ambient Temperature



PACKAGE MECHANICAL DATA
16 PINS - PLASTIC POWERDIP



PMDIP16W/EP5

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			20			0.787
E		8.8			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DIP16PW/TBL

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