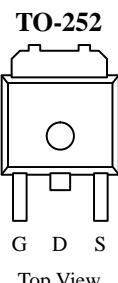


N-Channel Enhancement-Mode Transistor, Logic Level

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a
50	0.018 @ V _{GS} = 10 V	± 43
	0.020 @ V _{GS} = 4.5 V	± 43

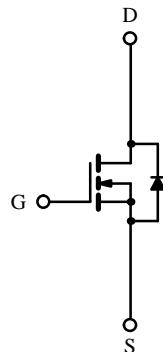
175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



Drain Connected to Tab

Top View

Order Number:
SUD45N05-20L



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	50	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current ^a	I _D	± 43	A
		± 30	
Pulsed Drain Current	I _{DM}	± 100	
Continuous Source Current (Diode Conduction) ^a	I _S	43	
Avalanche Current	I _{AR}	37	
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)	E _{AR}	93	mJ
Maximum Power Dissipation	P _D	75	W
		2.5 ^a	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient	R _{thJA}	60	°C/W
Free Air, FR4 Board Mount		110	
Maximum Junction-to-Case	R _{thJC}	2.0	

Notes

- a. Calculated Rating for T_C = 25°C, for comparison purposes only. This cannot be used as continuous rating (see Absolute Maximum Ratings and Typical Characteristics).
- b. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1410.

SUD45N05-20L

TEMIC
Semiconductors

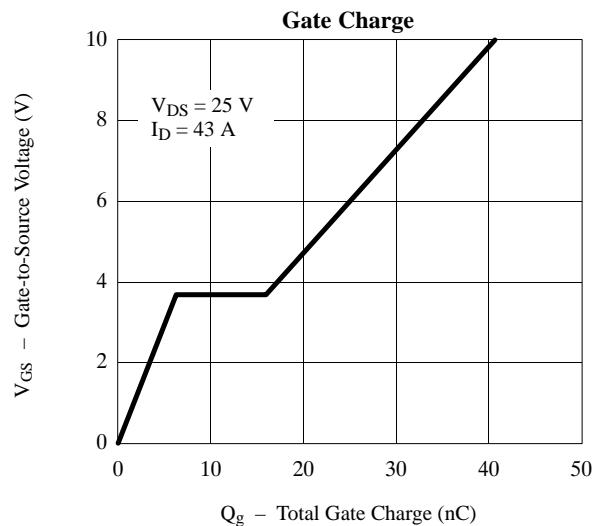
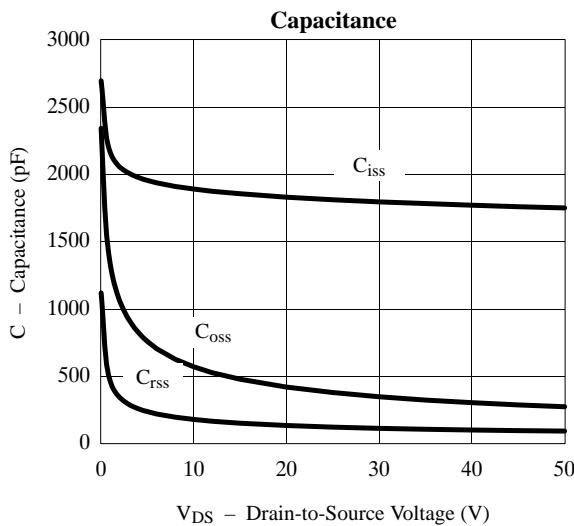
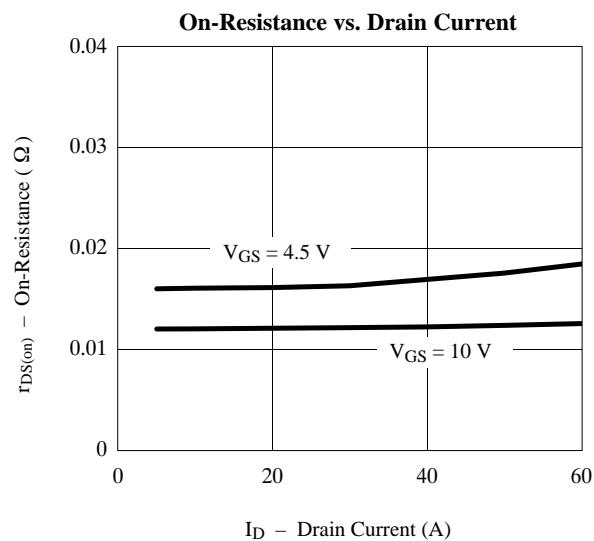
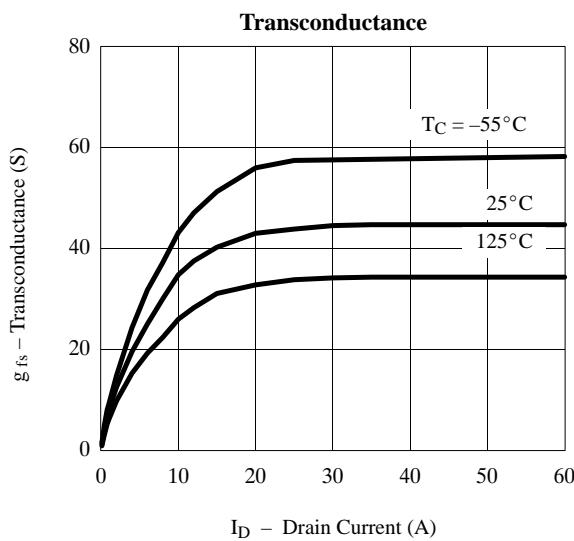
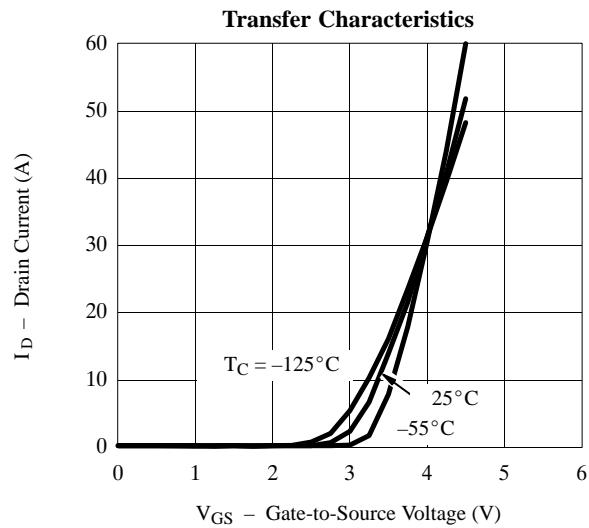
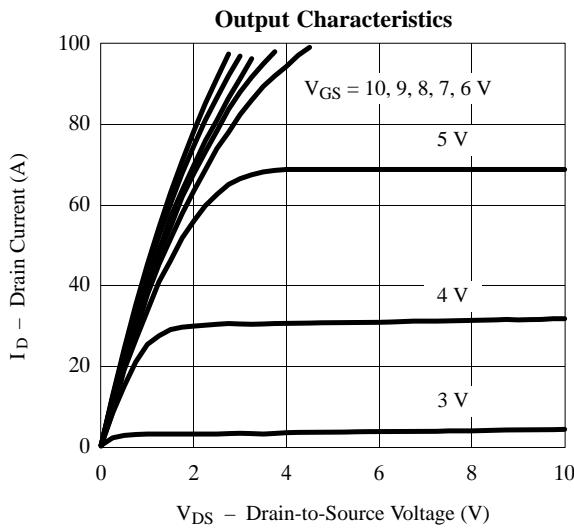
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	50			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0	2.0		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$		50		
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 175^\circ\text{C}$		150		
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	43			A
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.018		Ω
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125^\circ\text{C}$		0.036		
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125^\circ\text{C}$		0.040		
		$V_{GS} = 4.5 \text{ V}, I_D = 43 \text{ A}$		0.020		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 43 \text{ A}$	20			S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		1800	3600	pF
Output Capacitance	C_{oss}			370		
Reverse Transfer Capacitance	C_{rss}			130		
Total Gate Charge ^c	Q_g	$V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 43 \text{ A}$		43	60	nC
Gate-Source Charge ^c	Q_{gs}			7		
Gate-Drain Charge ^c	Q_{gd}			10		
Turn-On Delay Time ^c	$t_{d(\text{on})}$	$V_{DD} = 25 \text{ V}, R_L = 0.6 \Omega$ $I_D \cong 43 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$		10	20	ns
Rise Time ^c	t_r			10	20	
Turn-Off Delay Time ^c	$t_{d(\text{off})}$			32	60	
Fall Time ^c	t_f			7	15	
Source-Drain Diode Ratings and Characteristic ($T_C = 25^\circ\text{C}$)						
Pulsed Current	I_{SM}			43		A
Diode Forward Voltage ^b	V_{SD}	$I_F = 43 \text{ A}, V_{GS} = 0 \text{ V}$			1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 43 \text{ A}, \text{di}/\text{dt} = 100 \text{ A}/\mu\text{s}$		49	100	ns

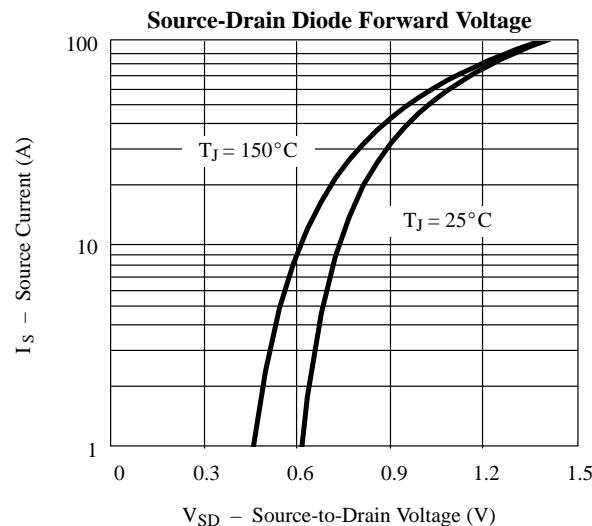
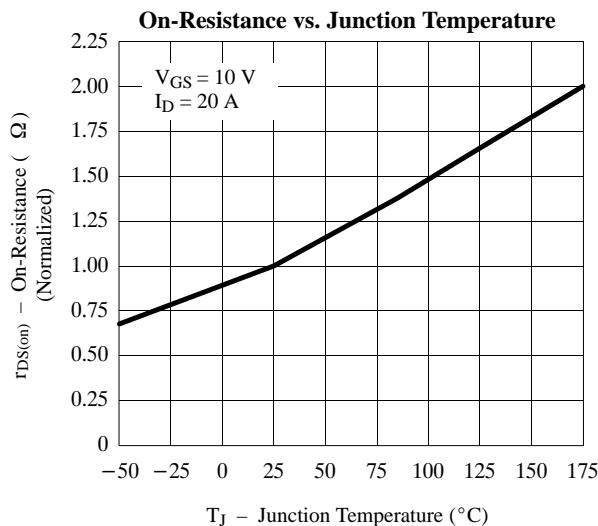
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)



Thermal Ratings

