

STP7NB40 STP7NB40FP

PRELIMINARY DATA

N - CHANNEL ENHANCEMENT MODE PowerMESHTM MOSFET

TYPE	V _{DSS}	R _{DS(on)}	ID
STP7NB40	400 V	< 0.9 Ω	7.0 A
STP7NB40FP	400 V	< 0.9 Ω	4.4 A

- TYPICAL $R_{DS(on)} = 0.75 \Omega$
- EXTREMELY HIGH dV/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

Using the latest high voltage MESH OVERLAYTM process, SGS-Thomson has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

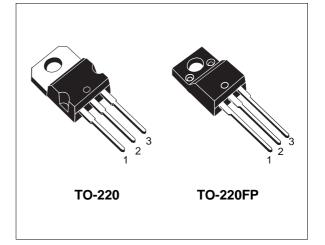
APPLICATIONS

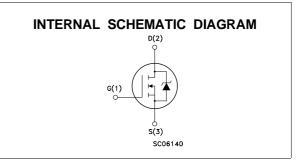
- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

ABSOLUTE N	IAXIMUM	RATINGS
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Symbol	Parameter		Value			
		STP7NB40	STP7NB40FP			
V _{DS}	Drain-source Voltage (V _{GS} = 0)		400	V		
Vdgr	Drain- gate Voltage (R_{GS} = 20 k Ω)		400	V		
VGS	Gate-source Voltage		± 30			
ID	Drain Current (continuous) at T _c = 25 °C	7	4.4	Α		
ID	Drain Current (continuous) at $T_c = 100$ °C	4.4	2.8	Α		
I _{DM} (●)	Drain Current (pulsed)	28	28	Α		
P _{tot}	Total Dissipation at $T_c = 25 \ ^{\circ}C$	100	35	W		
	Derating Factor	0.8	0.28	W/°C		
dv/dt(1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns		
VISO	Insulation Withstand Voltage (DC)	_	2000	V		
T _{stg}	Storage Temperature	-6	5 to 150	°C		
Tj	Max. Operating Junction Temperature		150	°C		
 Pulse wid 	th limited by safe operating area	(1) $I_{SD} \leq 7A$, di/dt $\leq 200 \text{ A/}\mu\text{s}$, V	$DD \le V_{(BR)DSS}, Tj \le T_{JMAX}$			

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice. January 1998





THERMAL DATA

			TO-220	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case	Max	1.25	3.57	°C/W
R _{thj-amb} R _{thc-sink} T _I	Thermal Resistance Junction-ambient Thermal Resistance Case-sink Maximum Lead Temperature For Soldering P	Max Typ urpose	62 0 30	.5	°C/W °C/W °C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	7	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	300	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25 \ ^{\circ}C$ unless otherwise specified) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A$ $V_{GS} = 0$	400			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating$ $T_c = 125 °C$			1 50	μΑ μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	$V_{GS} = \pm 30 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \ \mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V I_D = 3.5 A$		0.75	0.9	Ω
I _{D(on)}	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	7			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g _{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_{D} = 3.5 \text{ A}$	2.5	4.2		S
Ciss C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V f = 1 MHz V_{GS} = 0$		705 132 17	720 175 25	pF pF pF



ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Time Rise Time			11.5 7.5	16 11	ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 320 \text{ V}$ $I_D = 7 \text{ A}$ $V_{GS} = 10 \text{ V}$		21 7.3 8.5	30	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _f	0	$V_{DD} = 320 \text{ V}$ $I_D = 7 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 5)		9.5 9 16.5	15 14 25	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (●)	Source-drain Current Source-drain Current (pulsed)				7 28	A A
V _{SD} (*)	Forward On Voltage	$I_{SD} = 7 \text{ A}$ $V_{GS} = 0$			1.6	V
t _{rr}	Reverse Recovery Time	$I_{SD} = 7 \text{ A}$ di/dt = 100 A/µs V _{DD} = 100 V T _i = 150 °C		300		ns
Qrr	Reverse Recovery Charge	(see test circuit, figure 5)		2		μC
I _{RRM}	Reverse Recovery Current			13.7		A

(*) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %
 (•) Pulse width limited by safe operating area



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4/4