SPARClet™

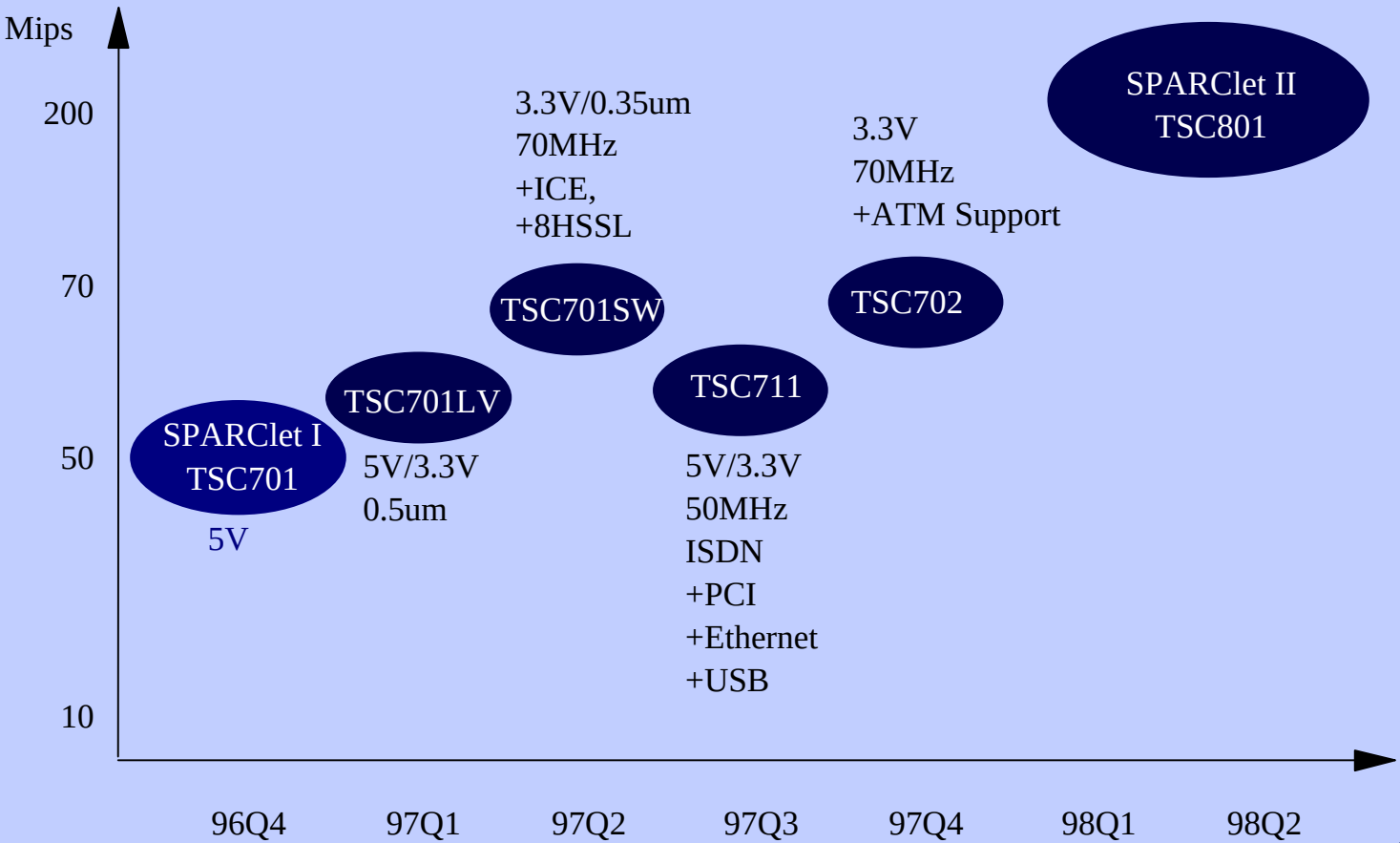
32-bit RISC+DSP Microcontrollers

TEMIC
Semiconductors

Architecture Introduction

- SPARClet™ is designed to help customers meet the enormous potential of the rapidly evolving 32 bit microprocessor + Digital Signal Processing (DSP) embedded telecommunication market.
- SPARClet™ has been developed with the dual goal of significantly lowering system and development costs while maintaining industry-leading performance standards across a broad range of applications.
- These goals have been met through the integration of DSP and control functions within a single, industry standard SPARC processor core, and via SPARClet's advanced Concurrent Processing capability.

SPARClet™ Road Map



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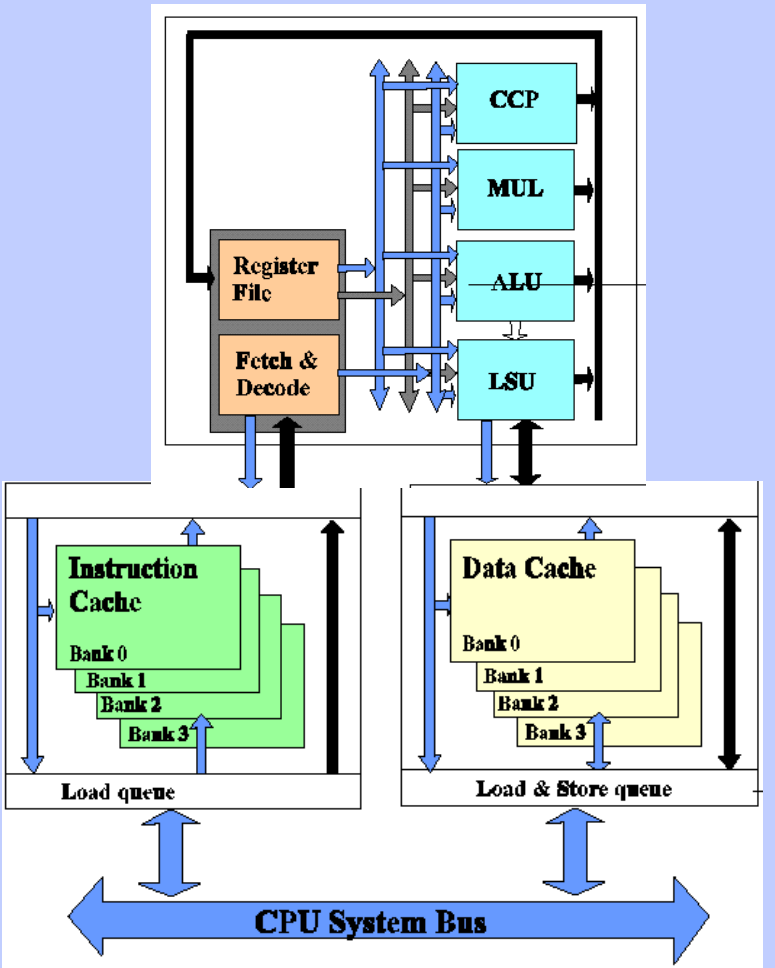
Architecture Principles (1/2)

Efficient Trap Model

on top of the "Precise" Trap Model which allows the SPARC V8 Compliancy, SPARClet™ implements "Interrupting" and "Differed" Models especially adapted for Real-Time Embedded applications. It furthermore includes a dedicated Alternate Register Window to enhance the Interrupt response time.

Massive parallel processing

all of the execution units work totally concurrently unless a data dependancy is observed. If independant, the results are written back in the Register File out of order.



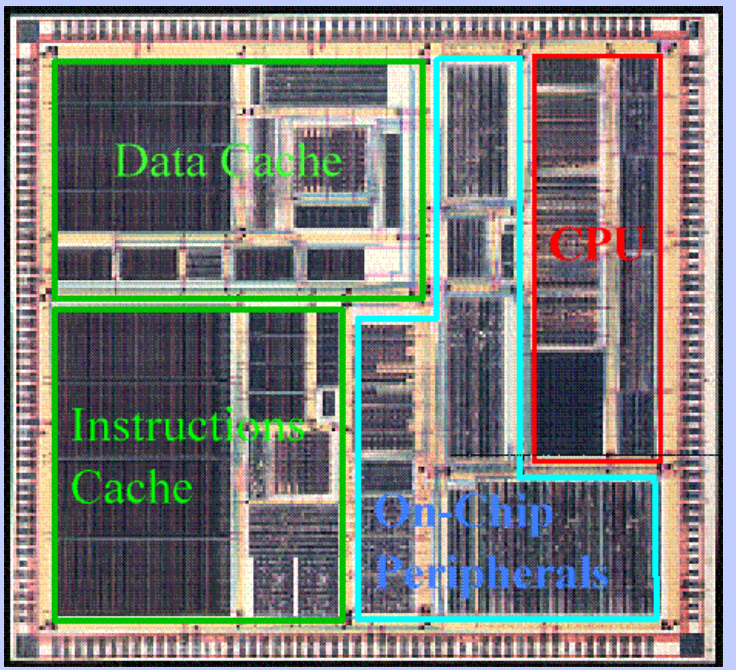
Architecture Principles (2/2)

Advanced Cache Memory management

in order to maximize the performance, the Data Cache contains a transaction re-ordering mechanism to extend the parallelism even to the external memory. In the other hand, anticipated requests on the System Bus limit the penalty in case of Instruction Cache miss.

Dataflow structure

the System Bus is of the "Split Cycle" type (splits the request and the completion, so freeing the bus in the meantime for other requests) and so provides an outstanding bus bandwidth.



TSC701 Communication Controller
Product Introduction

The TSC701 is a 32-bit Embedded SPARC Processor especially designed for the Communication Market. Built around TEMIC's SPARClet ™ architecture, the TSC701 provides a full one-chip system solution with a high performance core integrating DSP and High Speed HDLC Controllers and the necessary peripherals for this field of application.

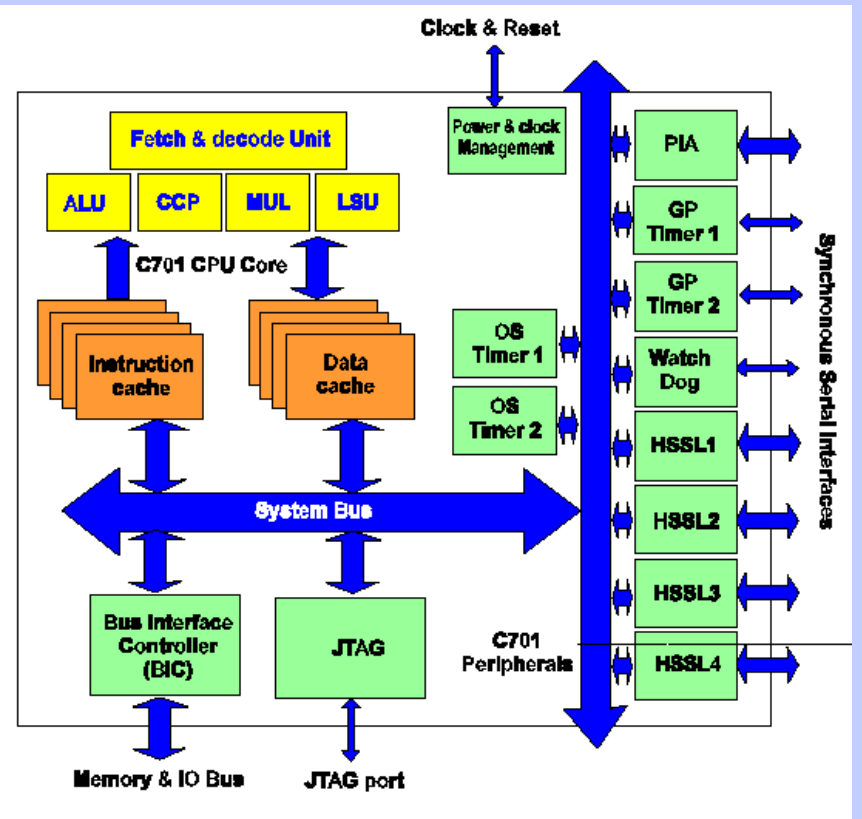
Performance

- 50 MIPS (@50MHz) SPARC V8 Compatible CPU
- High HDLC Processing Power: from 96 full duplex channels (worst case) up to 336 channels (best case configuration).
- Up to 8 Mbps Transmission Speed on each of the 4 HSSL (High Speed Serial Line).
- DSP capability: one cycle efficient 32x32-bit multiplier.

TSC701 Communication Controller Product Features

Key Features

- Communications Functions:
  - Communication Coprocessor (CCP)
  - 4 HSSL: asynchronous, synchronous (Point to Point and Multipoint) and PCM (T1, E1, T2... lines)
- DSP Capability:
  - Fully Parallel On-Chip 32x32-bit Multiplier
- Integrated Instruction Cache (16 KB) and Data Cache (8 KB)
- Multiprocessing Capability.



TSC701 Communication Controller
Product Applications

Typical application	*Main Benefits*
Cellular Phone Base Stations	- Integration of the DSP function - Multiprocessing
ISDN Routers	- Meet today's and tommorows's bit rates requirements
WAN Switching systems	- Up to 336 HDLC channels

TSC701 Communication Controller Design Tools (1/3)

In order to provide a comprehensive solution, a full range of software and debug tools have been developed around the TSC701.

Code Development Tools

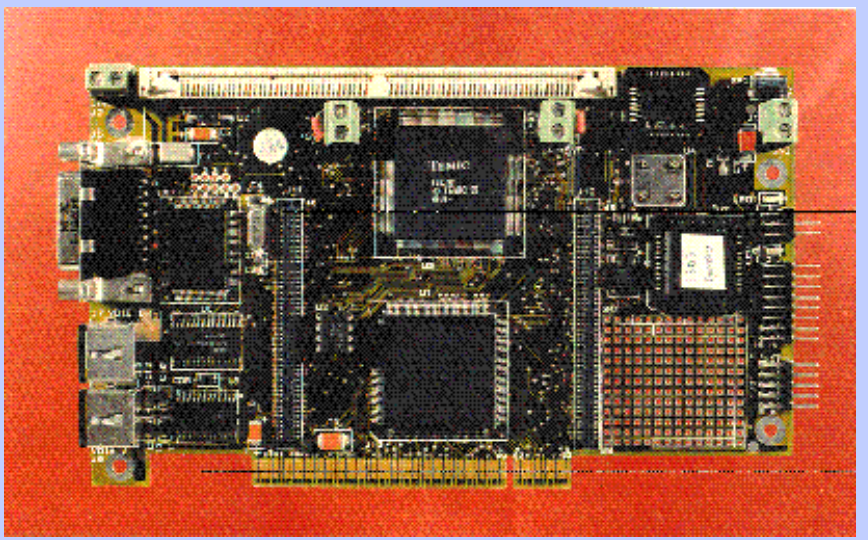
CYGNUS, one of the compiler's market leaders, provides the SPARClet™ CDK (CYGNUS Development Kit) package which includes a GNU based C/C++ compiler and the RGDB remote debugger. The CDK environment package is proposed for Sun OS, Solaris and Windows 3.1 platforms.

TSC701 Communication Controller Design Tools (2/3)

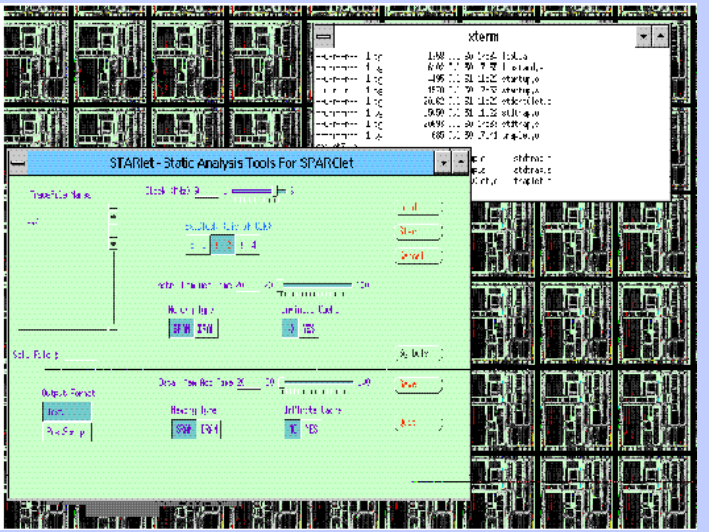
Starter & Application Kits

Those support kits available from TEMIC include:

- the TSC701 Demonstration Board (PCI, Ethernet) a debug monitor the necessary software libraries for:
  - the on-chip peripherals and coprocessors
  - the basic applicative functions (HDLC,Software DMA,...)
- the SPARClet™ CDK



TSC701 Communication Controller Design Tools (3/3)



Real-Time Operating System

- Chorus OS from **Chorus Systems**
- VxWorks/Tornado from **Wind River Systems**

Development and Debug Tools

- Architecture Simulator:the SASlet package provided by TEMIC
- Logic analyser: SPARClet™ dedicated tools including hardware probes and on-line disassembling are developed by **Tektronics**.
- ROM emulator: **XLNT** ROM emulation equipments.
- JTAG tool: JTAG tool from **Gopel**
- Real-Time Trace and Performance monitoring: CodeTest from **AMC**