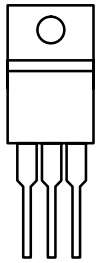
SMP40N10

N-Channel Enhancement-Mode Transistor

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.040	40

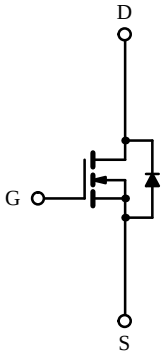
TO-220AB



G D S

Top View

DRAIN connected to TAB



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	40	A
	T_C = 100°C		25	
Pulsed Drain Current		I_{DM}	160	
Avalanche Current		I_{AR}	40	
Avalanche Energy	L = 0.3 mH	E_A	240	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	40	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		60	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.0	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

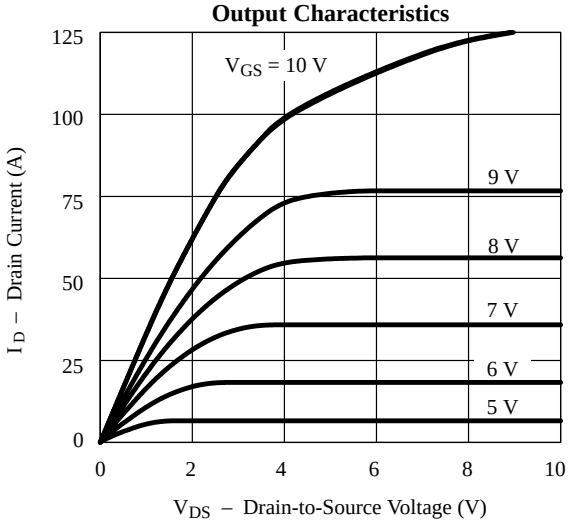
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0		4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A		0.030	0.040	Ω
		V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		0.055	0.072	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A	15	20		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		3000		pF
Output Capacitance	C_{oss}			750		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge[c]	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 40 A		62	80	nC
Gate-Source Charge[c]	Q_{gs}			20	30	
Gate-Drain Charge[c]	Q_{gd}			26	35	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.25 Ω I_D ≃ 40 A, V_{GEN} = 10 V, R_G = 5 Ω		17	30	ns
Rise Time[c]	t_r			80	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			40	60	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				40	A
Pulsed Current	I_{SM}				180	
Forward Voltage[b]	V_{SD}	I_F = 40 A, V_{GS} = 0 V			1.8	V
Reverse Recovery Time	t_{rr}			120	250	ns
Reverse Recovery Charge	Q_{rr}			0.3		µC

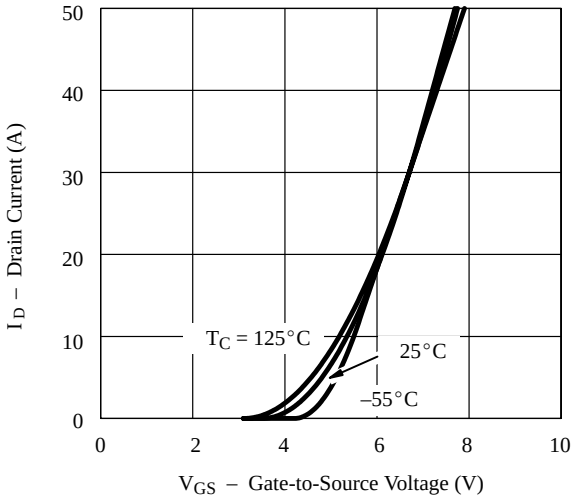
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

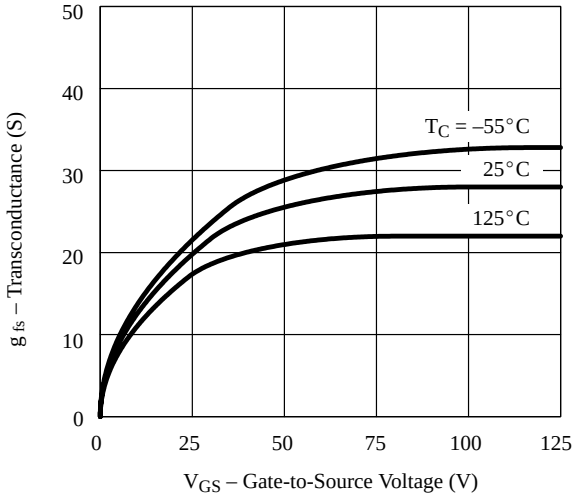
Output Characteristics



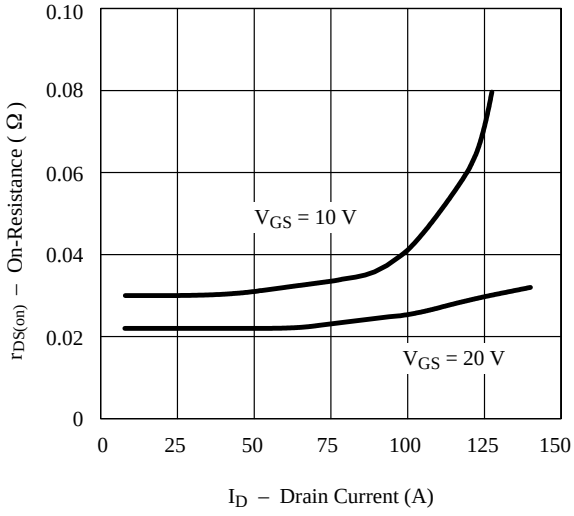
Transfer Characteristics



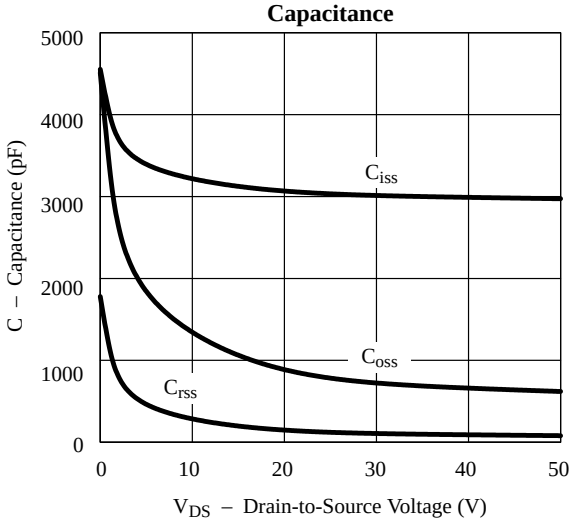
Transconductance



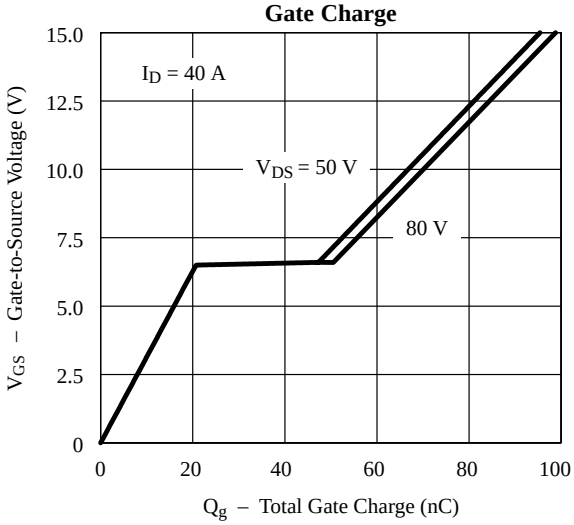
On-Resistance vs. Drain Current



Capacitance

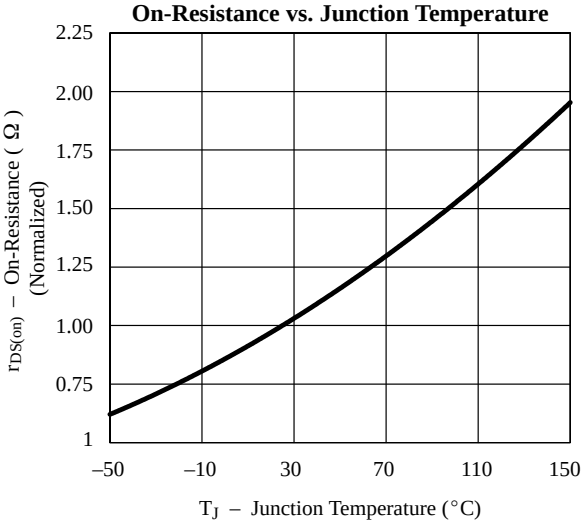


Gate Charge

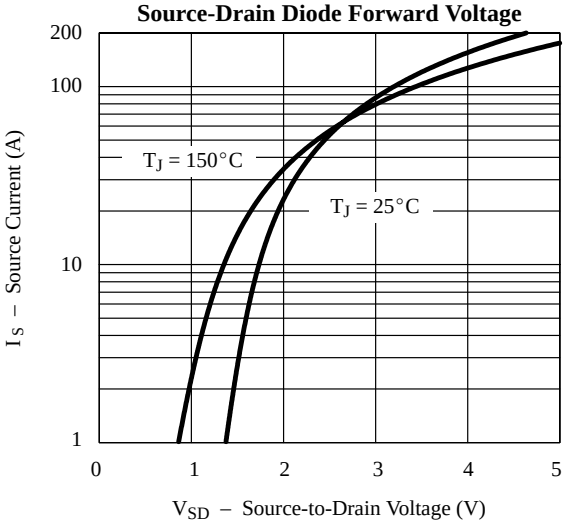


Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

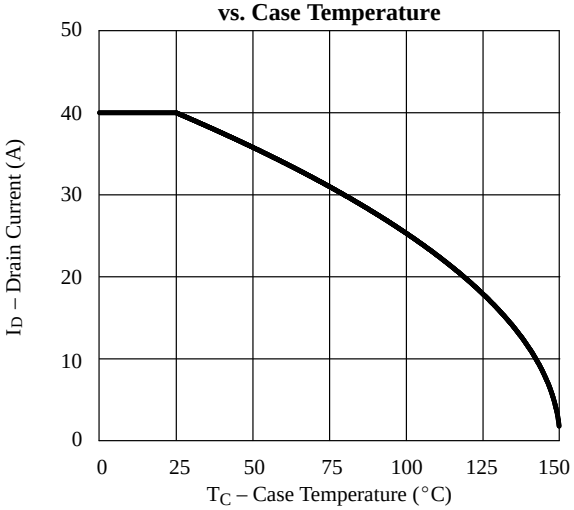


Source-Drain Diode Forward Voltage

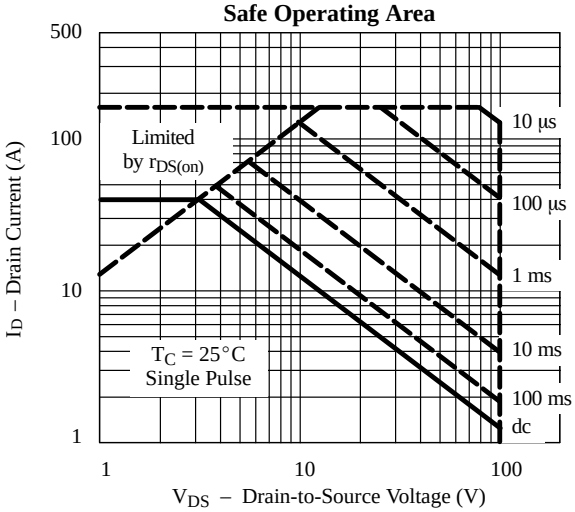


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case