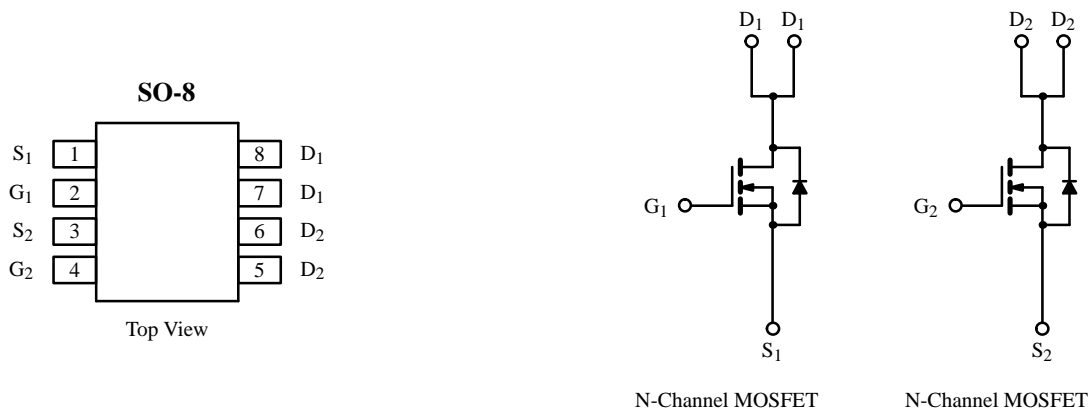


**Dual N-Channel Enhancement-Mode MOSFET**

**Product Summary**

V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
60	0.30 @ V <sub>GS</sub> = 10 V	± 2.0
	0.50 @ V <sub>GS</sub> = 5 V	± 0.6

For higher performance see Si9945DY



**Absolute Maximum Ratings (T<sub>A</sub> = 25° C Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	± 2.0
		T <sub>A</sub> = 70°C	± 1.6
Pulsed Drain Current	I <sub>DM</sub>	± 8	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	1.8	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	2
		T <sub>A</sub> = 70°C	1.3
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1224. A SPICE Model data sheet is available for this product (FaxBack document #5116).

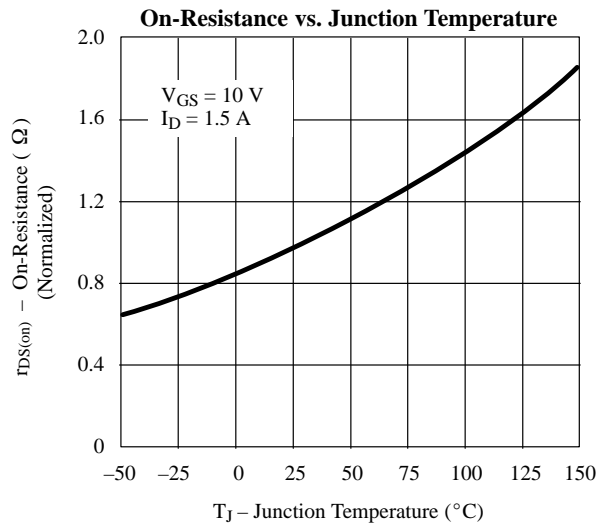
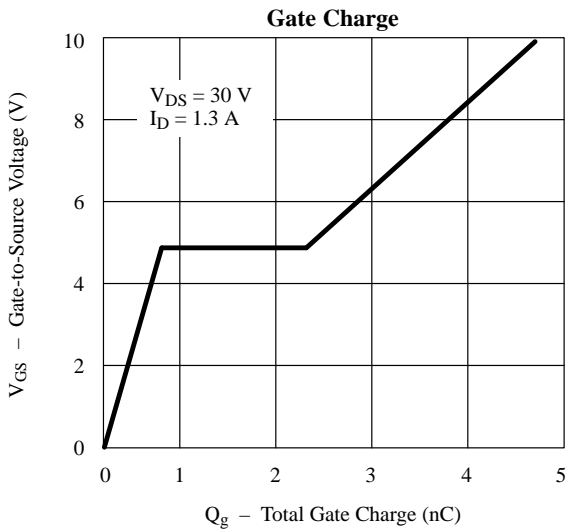
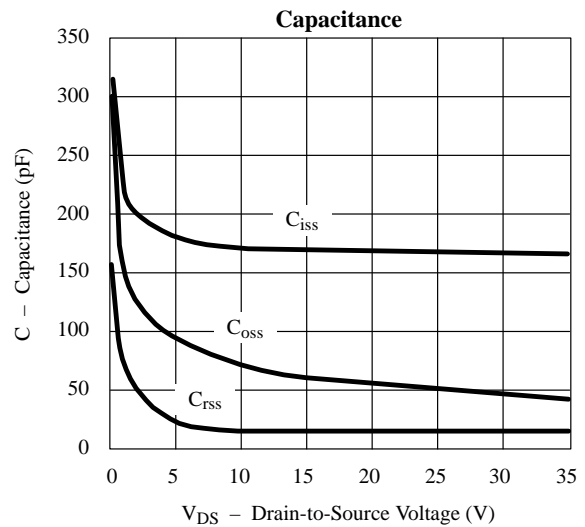
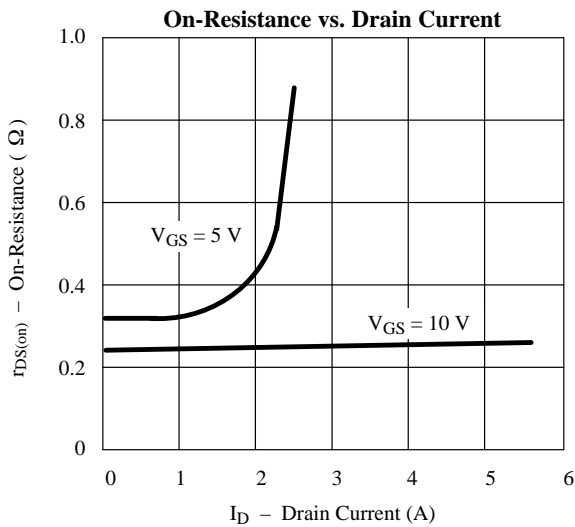
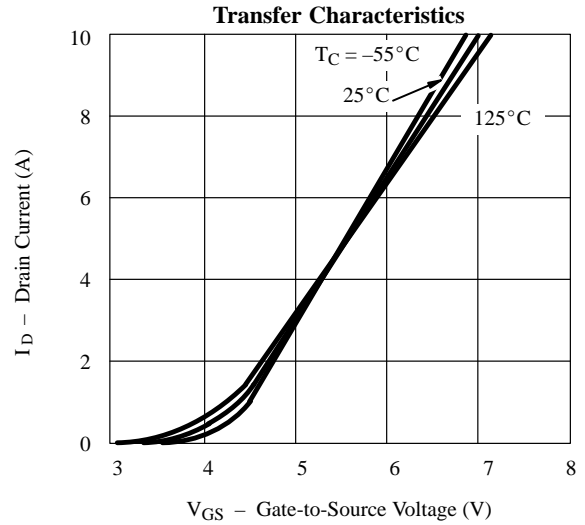
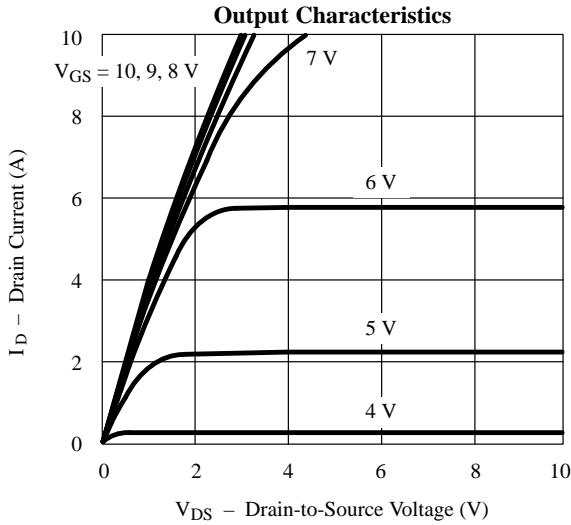
## Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			2	$\mu\text{A}$
		$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	8			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 1.5 \text{ A}$		0.23	0.30	$\Omega$
		$V_{GS} = 5 \text{ V}, I_D = 0.6 \text{ A}$		0.32	0.50	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 2.0 \text{ A}$		2.5		S
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_S = 1.25 \text{ A}, V_{GS} = 0 \text{ V}$		0.85	1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 1.3 \text{ A}$		5	15	nC
Gate-Source Charge	$Q_{gs}$			1		
Gate-Drain Charge	$Q_{gd}$			2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 50 \Omega$ $I_D \approx 0.6 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		7	40	ns
Rise Time	$t_r$			18	70	
Turn-Off Delay Time	$t_{d(off)}$			40	100	
Fall Time	$t_f$			23	70	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		70	100	

### Notes

- a. Guaranteed by design, not subject to production testing.  
 b. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .

**Typical Characteristics (25°C Unless Otherwise Noted)**



## Typical Characteristics (25°C Unless Otherwise Noted)

