DATA SHEET

DIGITAL dcc COMPACT CASSETTE

SAA2023
Drive processor for DCC systems

Preliminary specification
File under Integrated Circuits, IC01

May 1994

Philips Semiconductors

PHILIPS

Drive processor for DCC systems SAA2023

FEATURES

- Operating supply voltage: 4.5 to 5.5 V
- Low power dissipation: 260 mW at 5.0 V
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording
- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller ‘L3’ interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA2023 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

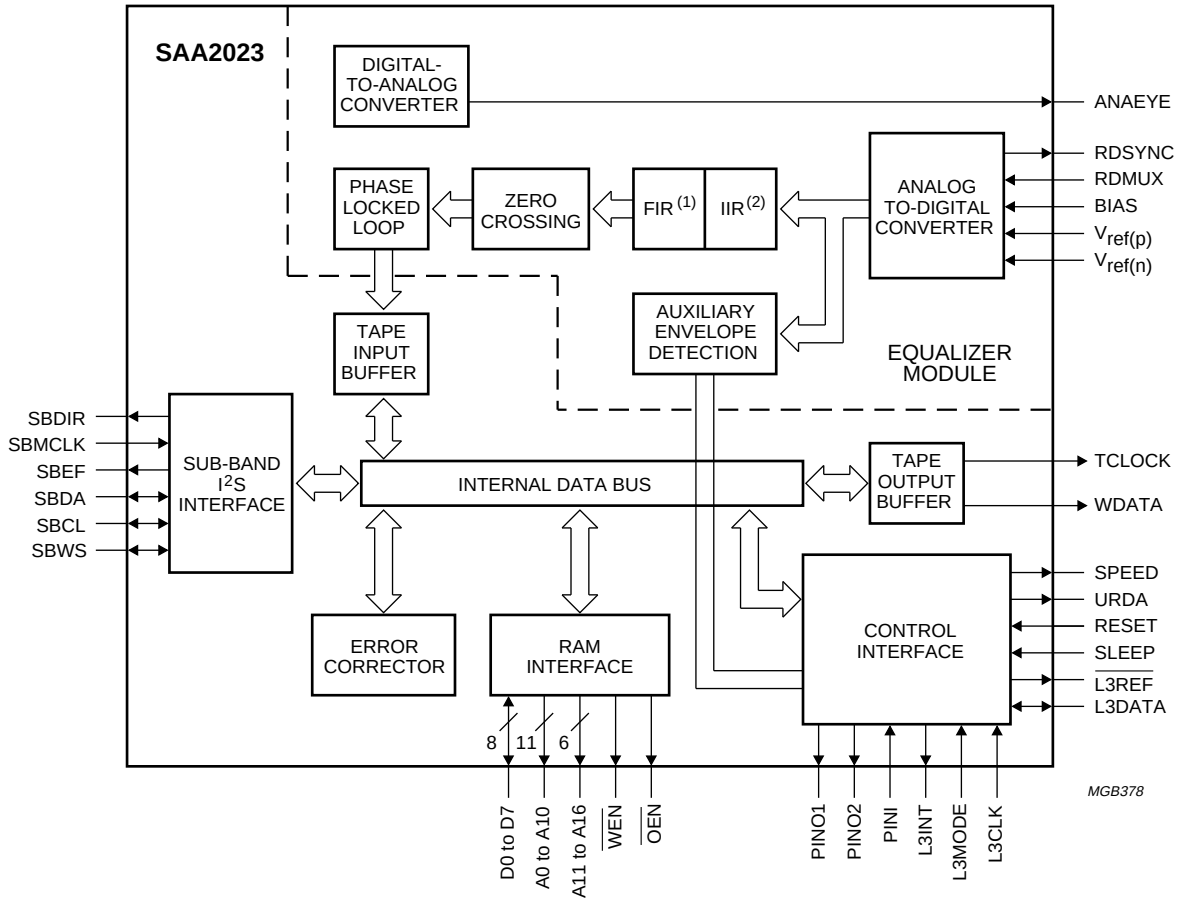
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2023H	80	TQFP80(1)	plastic	SOT315-1
SAA2023GP	80	QFP80(1)	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *“Quality Reference Pocketbook”* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.

(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{\text{L3REF}}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA2023	I
SLEEP	15	13	sleep mode selection of SAA2023	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{\text{OEN}}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{\text{RAS}}$	22	20	address SRAM; $\overline{\text{RAS}}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE(1)
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

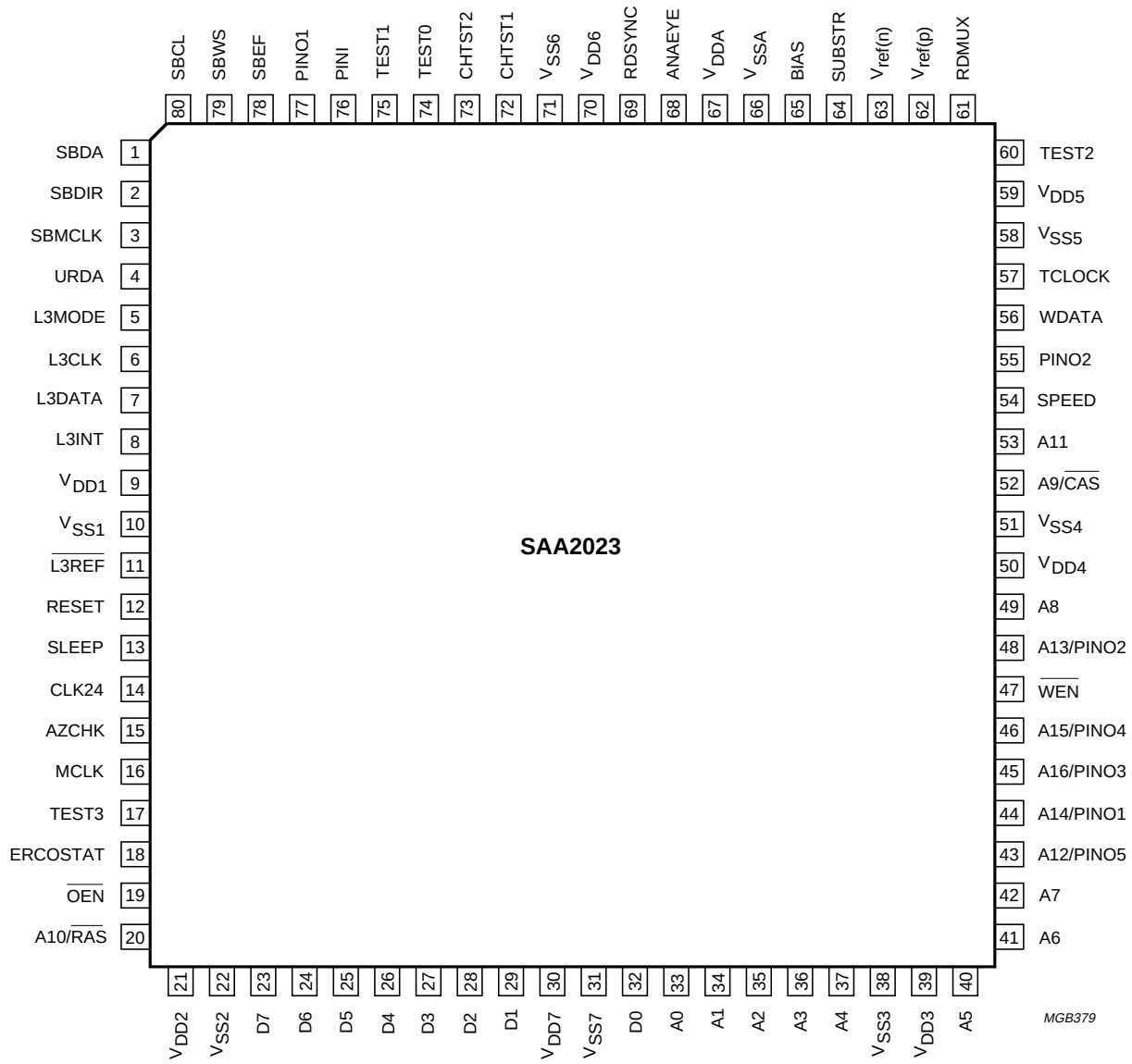


Fig.2 Pin configuration (SOT315-1; TQFP80).

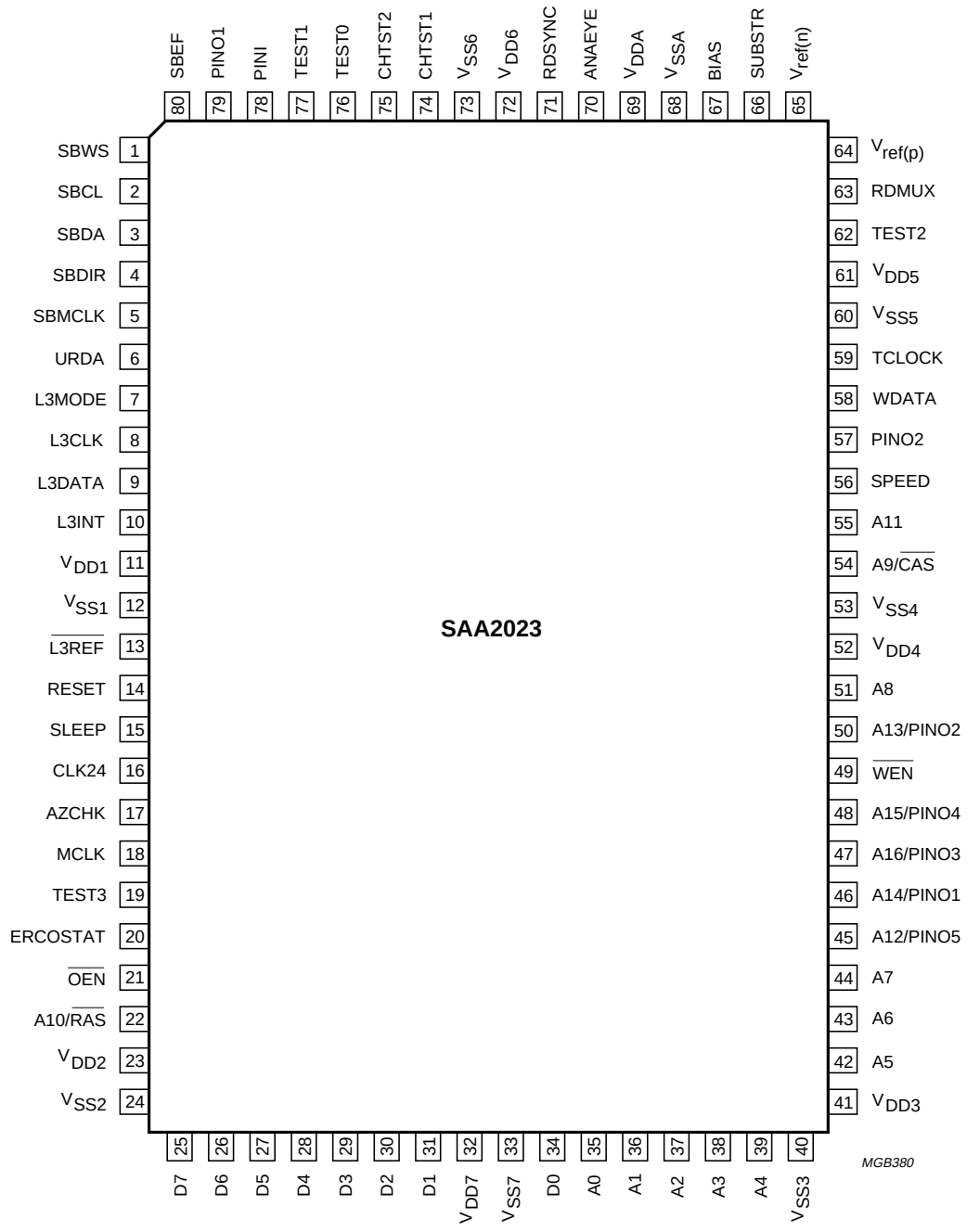


Fig.3 Pin configuration (SOT318-2; QFP80).

FUNCTIONAL DESCRIPTION

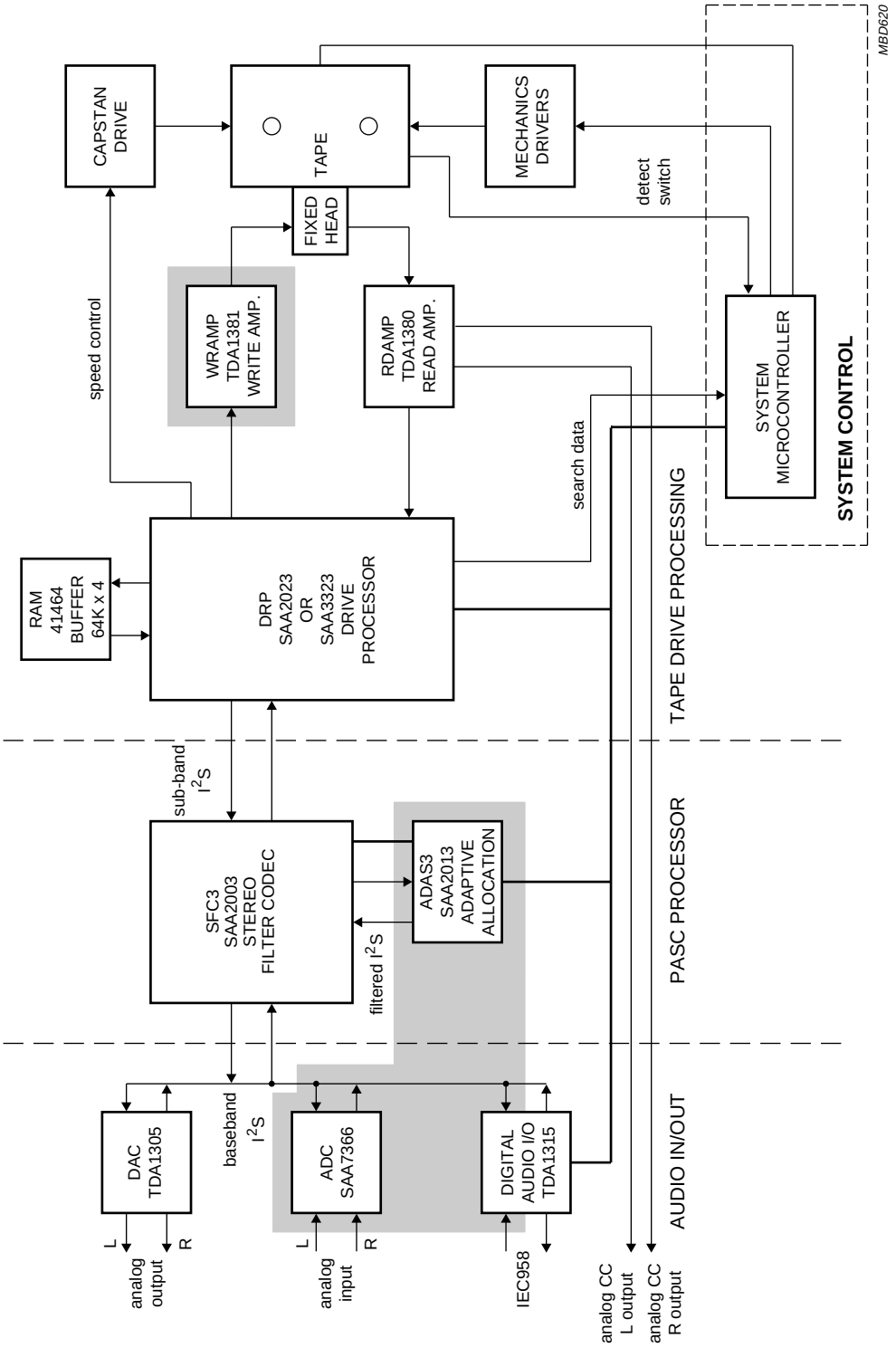


Fig.4 DCC system block diagram.

A simplified block diagram of the SAA2023 is shown in Fig.1.

DCC drive processing

The SAA2023 provides the following functions for the DCC drive processing.

PLAYBACK MODES

- Analog-to-digital conversion
- Tape channel equalization
- Tape channel data and clock recovery
- 10-to-8 demodulation
- Data placement in system RAM
- C1 and C2 error correction decoding
- Interfacing to sub-band serial PASC interface
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck.

RECORD MODES

- Interfacing to sub-band serial PASC interface
- C1 and C2 error correction encoding
- Formatting for tape transfer
- 8-to-10 modulation
- Interfacing to microcontroller for SYSINFO and AUX data
- Capstan control for tape deck, programmable by microcontroller.

SEARCH MODE

- Detection and interpretation of AUX envelope information
- AUX envelope counting
- Search speed estimation.

Tape Formatting and Error (TFE) correction module

The TFE module has 3 basic modes of operation as shown in Table 1.

Table 1 Basic modes of TFE module.

MODE	EXPLANATION
DPAP	audio and SYSINFO (main data) play; AUX play
DPAR	audio and SYSINFO (main data) play; AUX record
DRAR	audio and SYSINFO (main data) record; AUX record

TFE REGISTERS

The TFE module has 8 writable and 5 readable registers that are accessible via the L3 interface, one write register (CMD) and four read registers (STATUS0 to STATUS3) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 2.

Table 2 TFE register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
STATUS2	R
STATUS3	R
SET0	W
SET1	W
SET2	W
SET3[1]	W
SPDDTY	W
BYTCNT	W
RACCNT	W
SPEED	R

Note

1. The 4 LSBs of register ‘SET3’ set RAM type (RType) and RAM timing (RTim). See Table 3.

   For normal operation the 4 MSBs of register ‘SET3’ should be logic 0.

Table 3 RAM settings by register SET3.

RAM	REGISTER SET3
RTYPE 0	bit 0
RTYPE 1	bit 1
RTim 0	bit 2
RTim 1	bit 3

TFE DATA STREAMS

The TFE module has three read/write data streams that are accessible via the L3 interface and they are shown in Table 4.

Table 4 TFE data streams.

DATA STREAM NAME	READ/WRITE
SYSINFO	R/W
AUXINFO	R/W
Scratch pad RAM	R/W

TFE 'COMMANDS'

These are the commands that need to be sent to the TFE in order to access the indirectly accessible registers and the data streams, see Table 5.

Table 5 TFE commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
RDSPEED	0	0	0	0	0	0	0	0	read SPEED register
LDSET0	0	0	0	1	0	0	0	0	load new TFE settings register 0
LDSET1	0	0	0	1	0	0	0	1	load new TFE settings register 1
LDSET2	0	0	0	1	0	0	1	0	load new TFE settings register 2
LDSET3	0	0	0	1	0	0	1	1	load new TFE settings register 3
LDSPDDTY	0	0	0	1	0	1	0	1	load SPDDTY register
LDBYTCNT	0	0	0	1	0	1	1	1	load BYTCNT register
LDRACCNT	0	0	0	1	1	0	0	0	load RACCNT register
RDAUX	0	0	1	0	0	0	0	0	read AUXILIARY information
RDSYS	0	0	1	0	0	0	0	1	read SYSINFO
RDDRAC	Y	Z	1	0	0	0	1	0	read RAM data bytes (8 bits) from quarter YZ
RDWDRAC	Y	Z	1	0	0	0	1	1	read RAM data words (12 bits) from quarter YZ
WRAUX	0	0	1	1	0	0	0	0	write AUXILIARY information
WRSYS	0	0	1	1	0	0	0	1	write SYSINFO
WRDRAC	Y	Z	1	1	0	0	1	0	write RAM data bytes (8 bits) to quarter YZ
WRWDRAC	Y	Z	1	1	0	0	1	1	write RAM data words (12 bits) to quarter YZ

Digital equalizer module

The digital equalizer module has 2 basic modes of operation as shown in Table 6.

Table 6 Basic modes of equalizer module.

MODE	EXPLANATION
Play	main data and AUX channels are equalized
Search	only AUX channel is processed; AUX envelope information is processed

DIGITAL EQUALIZER REGISTERS

The digital equalizer module has 9 write only, 3 read only and 1 read/write register(s) that are accessible via the L3 interface, one write register (CMD) and 2 read registers (STATUS0 and STATUS1) which are directly addressable, the other registers are indirectly addressable via commands sent to the CMD register. The registers are named as shown in Table 7.

Table 7 Digital equalizer register names.

REGISTER NAME	READ/WRITE
CMD	W
STATUS0	R
STATUS1	R
COEFCNT	W
FCTRL	W
CHT1SEL	W
CHT2SEL	W
ANAEYE	W
AEC	R/W
SSPD	R
INTMASK	W
DEQ2SET	W
CLKSET	W

DATA STREAMS

The digital equalizer module has one write only and one read only data stream that are accessible via the L3 interface and they are shown in Table 8.

Table 8 Digital equalizer data streams.

DATA STREAM NAME	READ/WRITE
FIR coefficients to buffer bank	W
FIR coefficients from active bank	W

DIGITAL EQUALIZER "COMMANDS"

These are the commands that need to be sent to the digital equalizer in order to access the indirectly accessible registers and the data streams.

Table 9 Digital equalizer commands.

NAME	COMMAND BYTE								EXPLANATION
	7	6	5	4	3	2	1	0	
WRCOEF	0	0	1	1	0	0	0	0	write FIR coefficients to the digital equalizer buffer bank
RDCOEF	0	0	1	0	0	0	0	0	read FIR coefficients from the digital equalizer active bank
LDCOEFCNT	0	0	0	1	0	0	1	1	load FIR coefficient counter
LDFCTRL	0	0	0	1	0	1	0	0	load filter control register
LDT1SEL	0	0	0	1	0	1	1	0	load CHTST1 pin selection register
LDT2SEL	0	0	0	1	0	1	1	1	load CHTST2 pin selection register
LDTAEYE	0	0	0	1	1	0	0	0	load ANAEYE channel selection register
LDAEC	0	0	0	1	1	0	0	1	load AEC counter
RDAEC	0	0	1	0	0	0	1	0	read AEC counter
RDSSPD	0	0	1	0	0	1	0	0	read SEARCH speed register
LDINTMSK	0	0	0	1	0	0	1	0	load interrupt mask register
LDDEQ3SET	0	0	0	1	0	0	0	0	load digital equalizer settings register
LDCLKSET	0	0	0	1	0	0	0	1	load PLL clock extraction settings register

Table 10 Filter control register.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	µCS[1]	SH1	SH0	Reserved	
Default	0	0	0	0	1	0	1	1

Note

1. µCS is a microcontroller controlled coefficient bank switch. This causes the filter coefficients to be activated at a time that is safe for the digital equalizer, i.e. at the end of the FIR program and that the complete value of coefficient number 9 has been received.

Table 11 SH1 and SH2 (FIR output scaling).

SH		EFFECT ON FIR OUTPUT
1	**0**	
0	0	FIR mod 256
0	1	$\frac{FIR}{2}$ mod 256
1	0	$\frac{FIR}{4}$ mod 256
1	1	$\frac{FIR}{8}$ mod 256

Transfer of FIR coefficients

For the main data channels (tracks 0 to 7) there are 10 coefficients (taps) each of 8 bits, where all of the data channels make use of the same coefficients. The addresses for the main data coefficients 0 to 9 are 0 to 9_{dec} respectively.

There are ten coefficients (taps) each of 8 bits for the aux channel (CHAUX). The addresses for the auxiliary coefficients 0 to 9 are 16 to 25_{dec} respectively.

There are 2 banks of coefficients for both the aux and the main data channels, namely the ‘buffer’, and the ‘active’ banks. The microcontroller writes only to the ‘buffer’ banks, and reads only from the ‘active’ banks.

The microcontroller can poll the digital equalizer status bit BKSW to see when the switch occurs. BKSW starts life LOW, goes HIGH as a result of the bank switching and goes LOW as result of the complete value of a main data coefficient being received by the digital equalizer.

The microcontroller sets μCS HIGH before sending the new set of aux or main data coefficients, the digital equalizer resets it once the bank switch occurs.

The actual FIR coefficients that are used are a function of the tape head, read amplifier and type of tape (i.e. pre-recorded or own recorded) used, such information is outside of the scope of this data sheet.

Coefficient address counter (COEFCNT)

This 5 bit counter is used to point to the FIR coefficient to be transferred to or from the digital equalizer.

Table 12 Coefficient address counter.

BIT	7	6	5	4	3	2	1	0
Meaning	–	–	–	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	0	0	0	0	0

Pin explanations and interfacing to other hardware

RESET

This is an active HIGH input which resets the SAA2023 and brings it into its default mode, DPAP. This reset does not affect the contents of the FIR filter coefficients in the digital equalizer. This should be connected to the system reset, which can be driven by the microcontroller. The duration of the reset pulse should be at least 15 μs.

SLEEP

This pin is an active HIGH input which puts the SAA2023 in a low power consumption SLEEP mode. This pin should be connected to the DCC SLEEP signal, which can be driven by the microcontroller. The CLK24 clock may be stopped and the VREFP and VREFN inputs brought to ground while the SAA2023 is in ‘sleep’ mode to further reduce power consumption. When recovering from sleep mode, the SLEEP pin should be taken LOW and the SAA2023 reset.

CLK24

This is the 24.576 MHz clock input and should be connected directly to the SAA2003 (pin CLK24).

Sub-band serial PASC interface connections

The timing for the sub-band serial PASC interface is given in Figs 5 to 7.

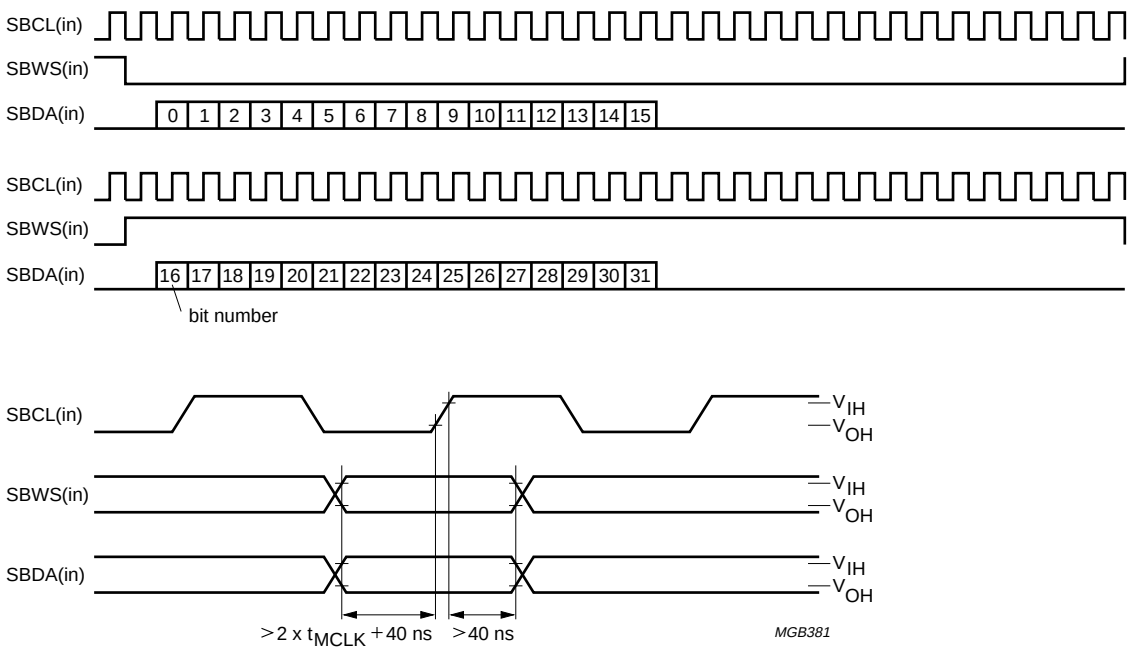


Fig.5 Sub-band serial PASC interface timing; DRAR mode.

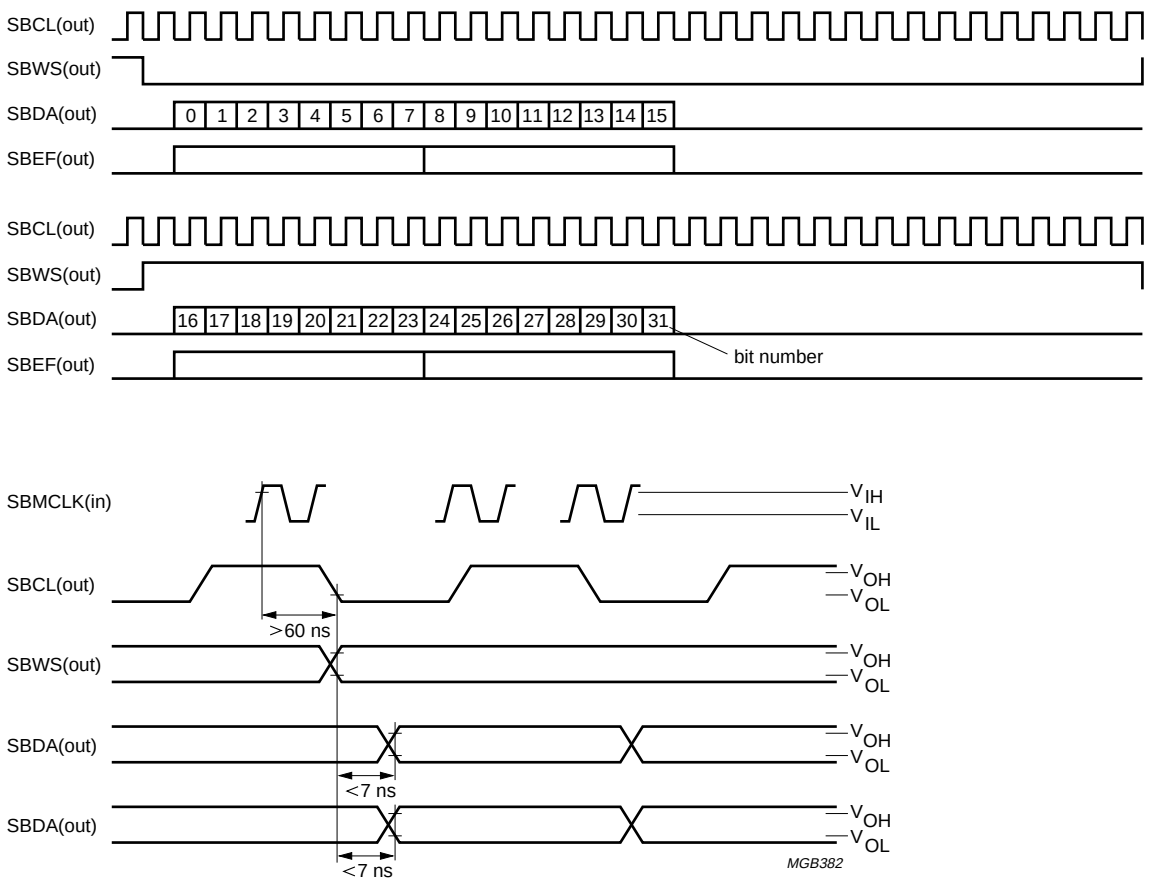


Fig.6 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 1.

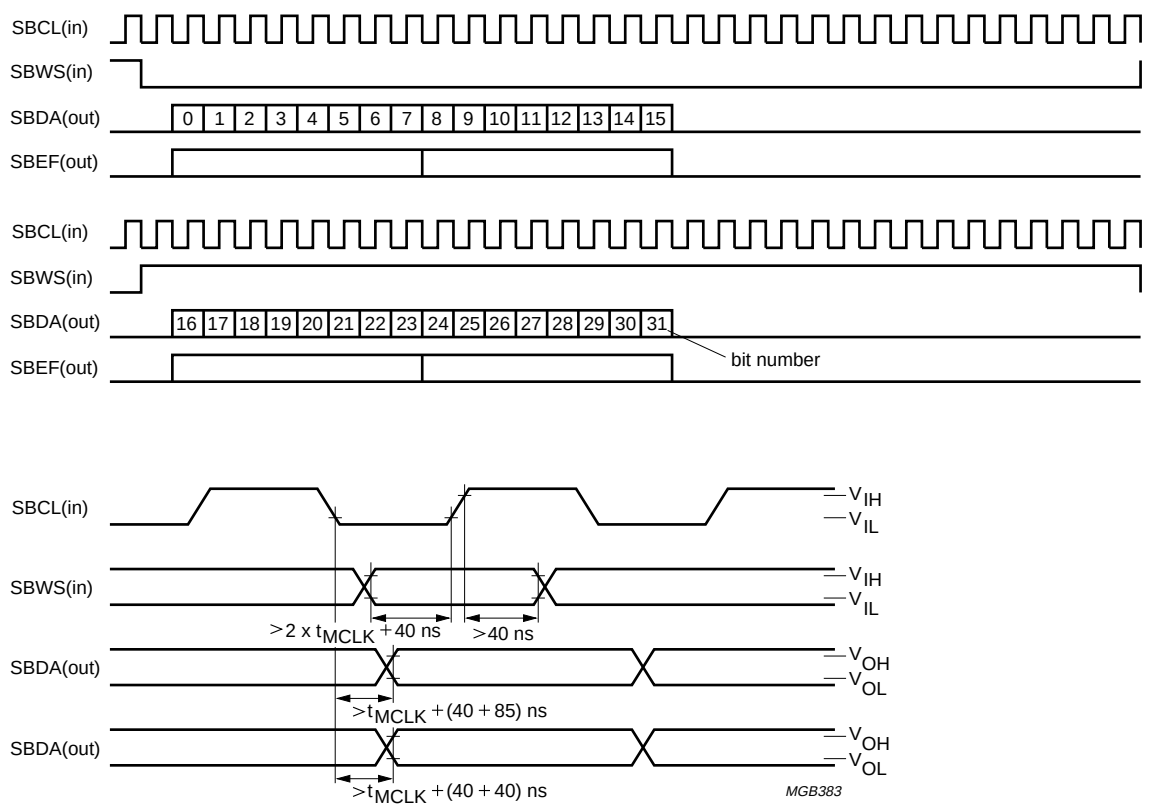


Fig.7 Sub-band serial PASC interface timing in play modes; DRPMAS = logic 0.

SBMCLK

This is the sub-band master clock input for the sub-band serial PASC interface. The frequency of this signal is nominally 6.144 MHz. When the SAA2023 is used with SAA2003 this pin is tied to ground, and the TFE settings bit ‘DRPMAS’ set to logic 1.

SBDIR

This output pin is the sub-band serial PASC bus direction signal, it indicates the direction of transfer on the sub-band serial PASC bus. This pin connects directly to the SBDIR pin on the SAA2003. The transfer directions are shown in Table 13.

Table 13 PASC bus transfer directions.

SBDIR	DIRECTION
1	SAA2023 to SAA2003 transfer (audio play)
0	SAA2003 to SAA2023 transfer (audio record)

SBCL

This input/output pin is the bit clock line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 768 kHz.

SBWS

This input/output pin is the word select line for the sub-band serial PASC interface to the SAA2003. When used with SAA2003 this pin is input only. It has a nominal frequency of 12 kHz.

SBDA

This input/output pin is the serial data line for the sub-band serial PASC interface to the SAA2003.

SBEF

This active HIGH output pin is the error-per-byte line for the sub-band serial PASC interface to the SAA2003.

URDA

This active HIGH output pin indicates that the main data (audio), the SYSINFO and the AUXILIARY data are NOT usable, regardless of the state of the corresponding reliability flags. The state of this pin is reflected in the URDA bit of STATUS byte 0, which can be read by the microcontroller. This pin should be connected directly to the URDA pin of the SAA2003. URDA goes active as a result of a reset, a mode change from mode DRAR to DPAP, or if the SAA2023 has had to re-synchronize with the incoming data from tape.

The position of the first sub-band serial PASC bytes in a tape frame is shown in Figs 8 and 9.

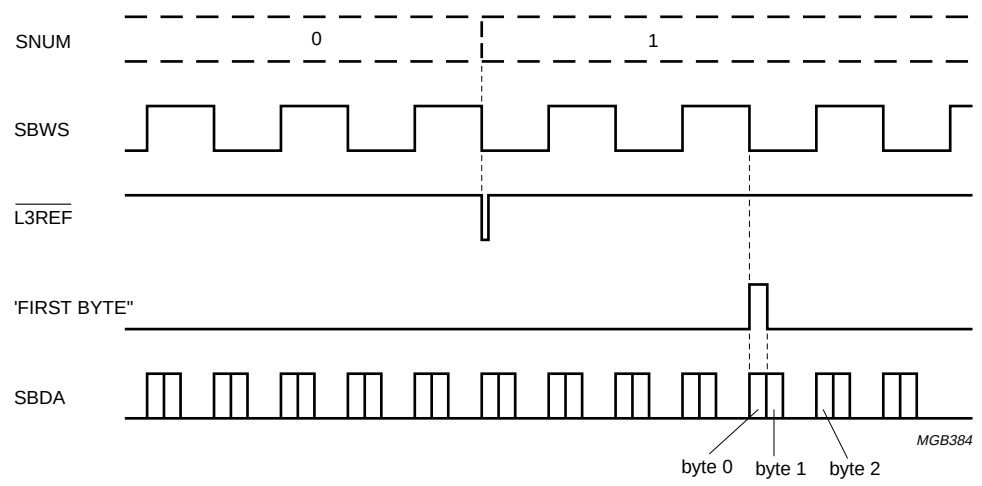


Fig.8 Position of first sub-band serial PASC bytes in a tape frame in DPAP/DPAR mode.

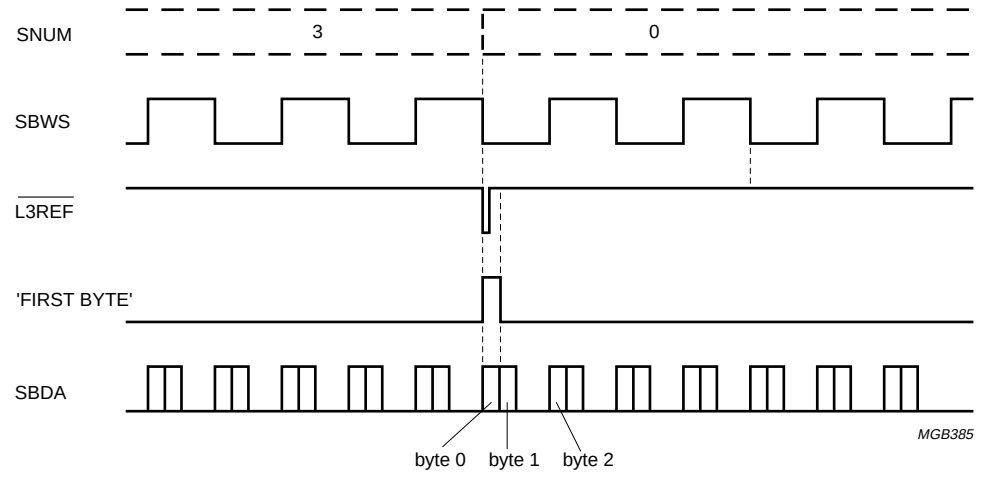


Fig.9 Position of first sub-band serial PASC bytes in a tape frame in DRAR mode.

RAM connections

The SAA2023 has been designed to operate with DRAMs and SRAMs. Suitable DRAMs are 64K × 4-bit or 256K × 4-bit configurations operating in page mode, with an access time of 80 to 100 ns. The timing for read, write and refresh cycles for DRAMs is shown in Figs 10 to 12. The timing for SRAMs is shown in Figs 13 to 19.

For fast SRAMs: (these values are subject to verification during characterization). The conditions (most critical at the required V_{DD}) are shown in Table 14.

Table 14 Fast SRAM conditions.

CONDITION(1)	TIME
Write pulse duration	$t_W \leq 140$ ns
Data set-up to rising $\overline{WEN}$	$t_{su} \leq 72$ ns
Write cycle time	$T_{cy} \leq 200$ ns
Read access time	$t_{ACC} \leq 240$ ns

Note

1. The SAA2023 should work in: RType = ‘01’; RTim = ‘00’ mode.

A9/$\overline{CAS}$

When SAA2023 is used with SRAM this output pin is Address line 9, and should be connected directly to the corresponding address pin on the SRAM. When SAA2023 is used with DRAM this output pin is the column address strobe (active LOW), it connects directly to the column address strobe pin of the DRAM.

A10/$\overline{RAS}$

When SAA2023 is used with SRAM this output pin is Address line 10, and should be connected to the corresponding address pin of the SRAM. When SAA2023 is used with DRAM this output pin is the row address strobe (active LOW), it connects directly to the row address strobe pin of the DRAM.

$\overline{OEN}$

This output pin is the output enable (active LOW) for the RAM, it connects directly to the output enable pin of the RAM.

$\overline{WEN}$

This output pin is the write enable (active LOW) for the RAM, it connects directly to the write enable pin of the RAM.

A0 TO A8

When SAA2023 is used with DRAM these output pins are the multiplexed column and row address lines. When the 64K × 4-bit DRAM is used, pins A0 to A7 should be connected to the DRAM address input pins, and pin A8 should be left unconnected. When using the 256K × 4-bit DRAM the address pins A0 to A8 should be connected to the address input pins of the DRAM.

When SAA2023 is used with SRAM these are the lower address pins and should be connected directly to the SRAM address pins.

A11

This output pin is the an address pin for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used this pin should not be connected.

A10 AND A12 TO A16

These output pins are the upper address pins for the SRAM and when SRAM is used they should be connected directly to the address pins of the SRAM. When DRAM is used or when the small SRAM is used all or some of these pins become available as Port expander outputs.

Table 15 Port expander outputs.

PIN NAME	PIN		PORT EXPANDER OUTPUT	CONDITIONS
	QFP80	TQFP80		
A14/PINO1	46	44	PINO1	RType = 00
A13/PINO2	50	48	PINO2	RType = 00
A16/PINO3	47	45	PINO3	RType = 00 or RType = 01
A15/PINO4	48	46	PINO4	RType = 00 or RType = 01
A12/PINO5	45	43	PINO5	RType = 00

D0 TO D3

When SAA2023 is used with SRAM these I/O pins form the lower nibble of the data bus connection to the RAM, and should be connected to the corresponding data I/O pins of the SRAM. When SAA2023 is used with DRAM these input/output pins are the data lines for the RAM, they should be connected directly to the DRAM data I/O pins.

D4 TO D7

These input/output pins are the upper nibble of the data bus for use with SRAM, and when SRAM is being used they should be connected directly to the corresponding SRAM I/O pins.

Fig.10 DRAM read cycle timing.