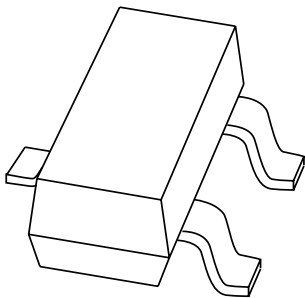


DATA SHEET



PDTA114TT PNP resistor-equipped transistor

Objective specification
Supersedes data of 1998 May 18

1999 Apr 13

PNP resistor-equipped transistor

PDTA114TT

FEATURES

- Built-in bias resistor R1 (typ. 10 kΩ)
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

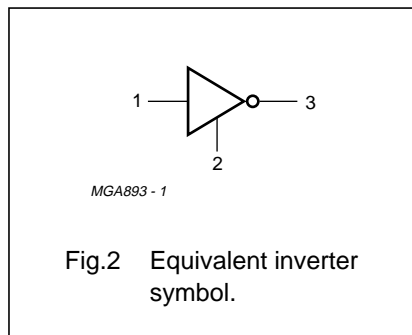
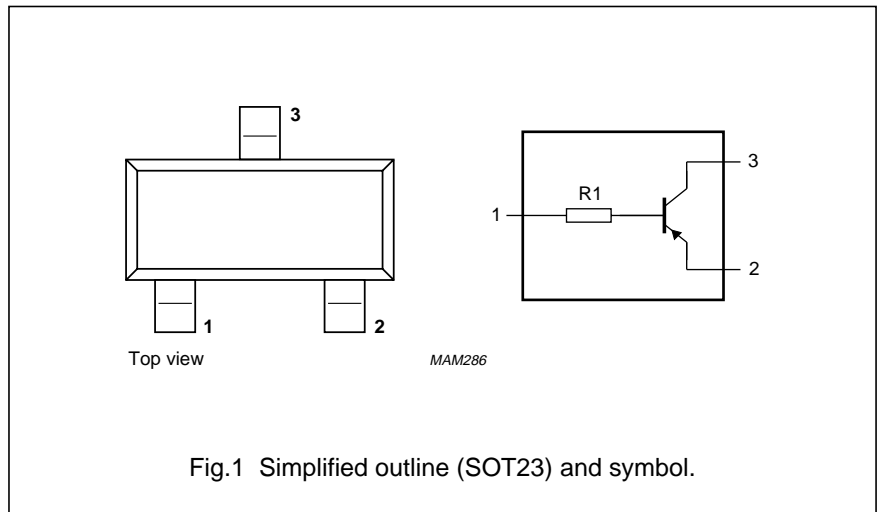
- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of an external resistor.

DESCRIPTION

PNP resistor-equipped transistor in a SOT23 plastic package.
NPN complement: PDTC114TT.

PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground (+)
3	collector/output



MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PDTA114TT	*11

Note

- * = p : Made in Hong Kong.
* = t : Made in Malaysia.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CB0}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

PNP resistor-equipped transistor

PDTA114TT

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	500	K/W

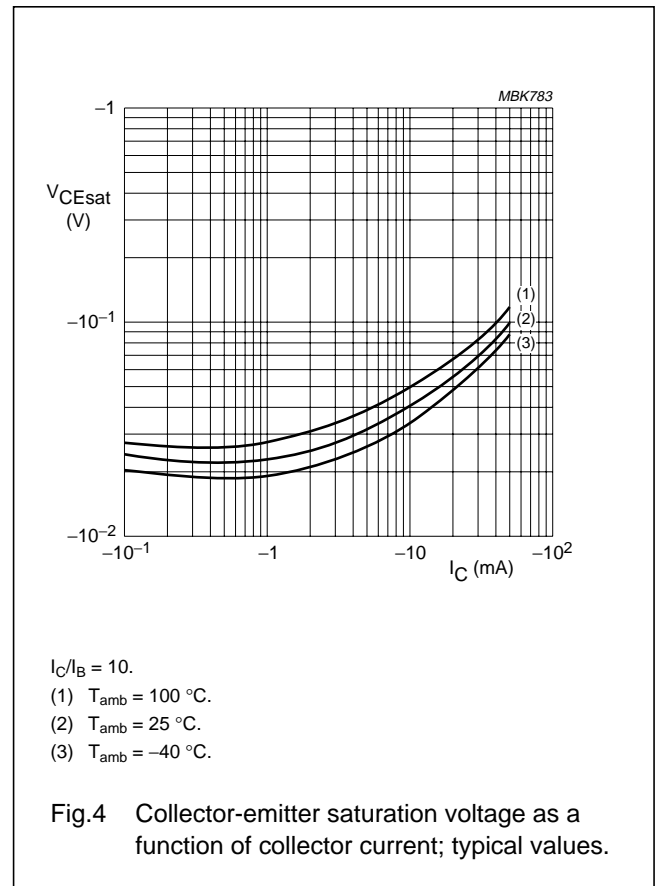
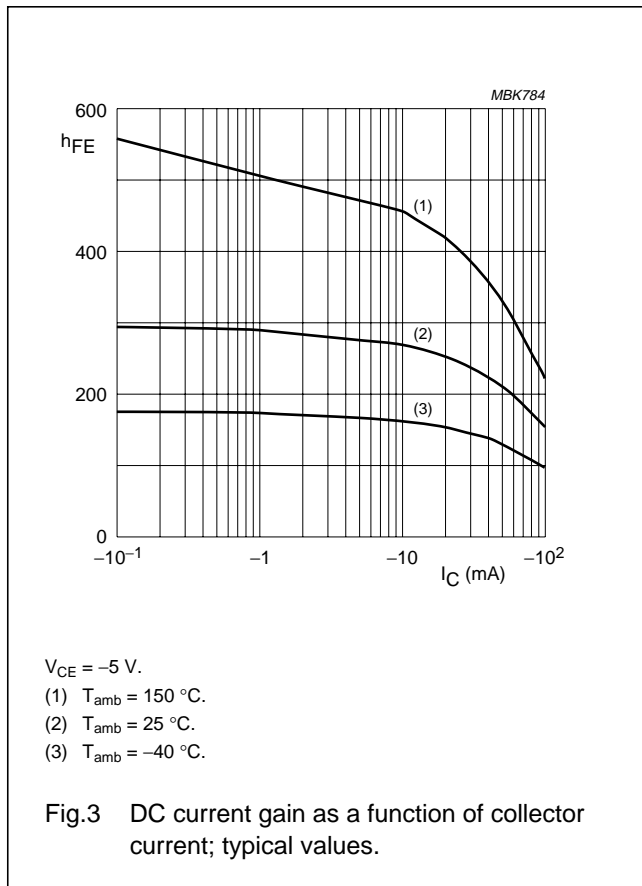
Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -50\text{ V}$	-	-	-100	nA
I_{CEO}	collector cut-off current	$I_B = 0; V_{CE} = -30\text{ V}$	-	-	-1	μA
		$I_B = 0; V_{CE} = -30\text{ V}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -4\text{ V}$	-	-	-100	nA
h_{FE}	DC current gain	$I_C = -1\text{ mA}; V_{CE} = -5\text{ V}$	200	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}$	-	-	-150	mV
R1	input resistor		7	10	13	$\text{k}\Omega$
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = -10\text{ V}; f = 1\text{ MHz}$	-	-	3	pF



PNP resistor-equipped transistor

PDTA114TT

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



PNP resistor-equipped transistor

PDTA114TT

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP resistor-equipped transistor

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NOTES

PNP resistor-equipped transistor

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NOTES

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