

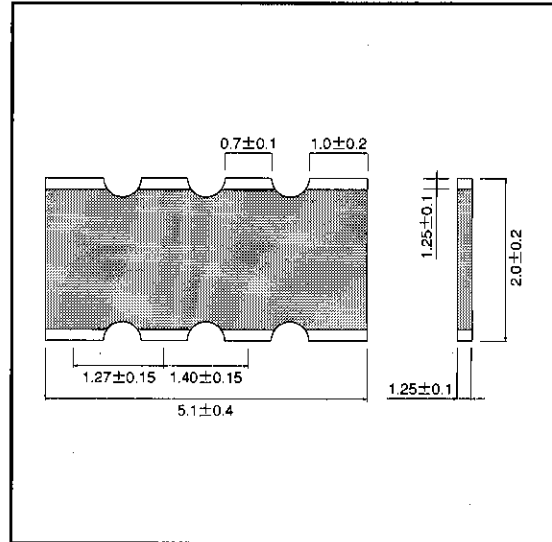
Multi-layer ceramic chip capacitors

MNA24 (2012×4 size chip network capacitor)

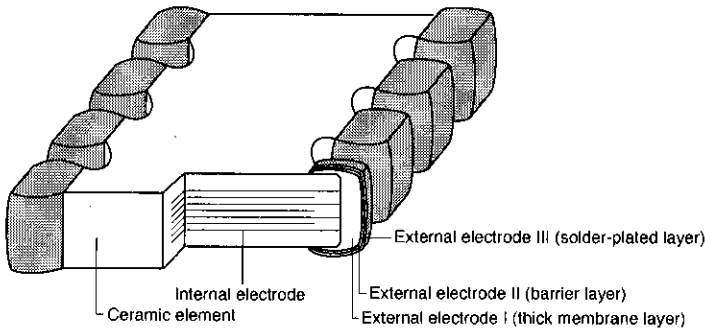
●Features

- 1)Area ratio is approximately 43% smaller than that of chip MCH21, enabling high-density mounting.
- 2)Mounting costs are reduced.
- 3)Use of convex electrodes prevents solder bridging during mounting, and makes it easy to perform a visual inspection of the mounted component. Also facilitates automatic inspection.
- 4)Solder-plated terminals offer superior wetting properties and resistance to soldering heat.
- 5)Each element is independent to ensure a wide range of circuit applications.
- 6)Can be packed on taping.

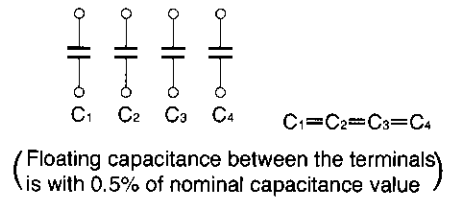
●External dimensions (Units: mm)



●Structure



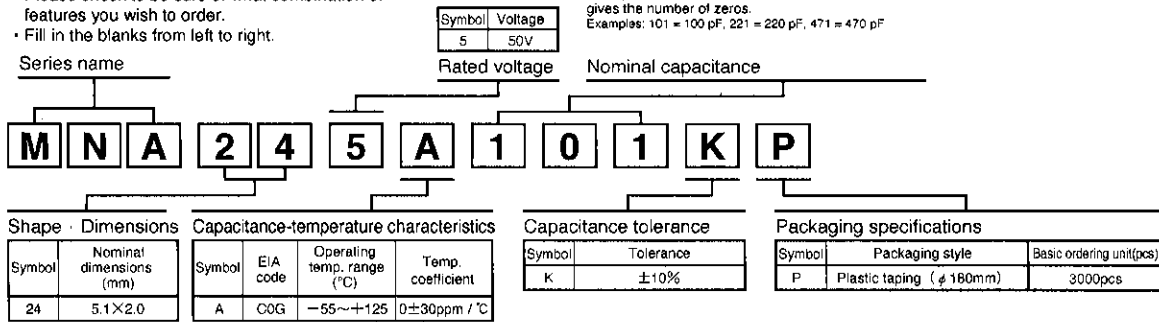
●Equivalent circuits



● Makeup of the part number

- When ordering, please specify the part number.
- Please check to be sure of what combination of features you wish to order.
- Fill in the blanks from left to right.

Three-digit number indicates the number of picofarads. The first two digits are the significant digits; the last digit gives the number of zeros. Examples: 101 = 100 pF, 221 = 220 pF, 471 = 470 pF





● Capacitance range

(Units : pF)

Part No.	Thickness (mm)	A (C0G) characteristics	
			50V
MNA24	1.25±0.1	100, 220, 470	
Tolerance (%)		K (±10)	

● Characteristics (for temperature compensated)

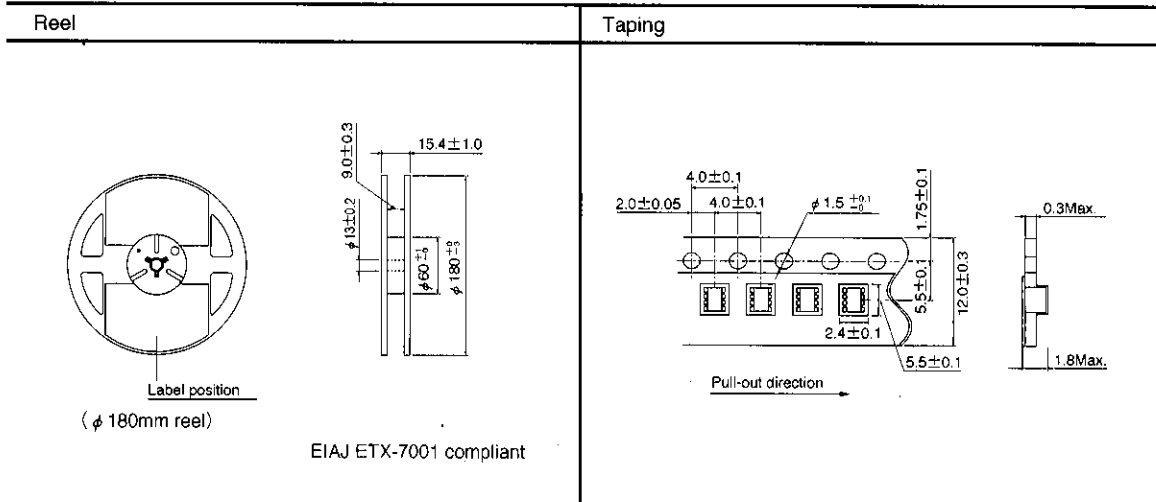
Temperature characteristics		A (COG)	Test methods/conditions (based on JIS C 5102)
Operating temperature range		-55°C ~ +125°C	
Nominal capacitance (C)		Must be within the specified tolerance range.	Measured at room temperature and standard humidity, Based on paragraph 7.8 and paragraph 9.
Dissipation factor (tan δ)		100(400+20C)% or less : Less than 30 pF 0.1% or less : 30 pF or larger	1000pF or less Measurement frequency: 1±0.1MHz Measurement voltage: 1±0.1Vrms. Over 1000pF Measurement frequency: 1±0.1kHz Measurement voltage: 1±0.1Vrms.
Insulation resistance (IR)		10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	Measurement is made after rated voltage Based on paragraph 7.6 is applied for 60±5s.
Withstanding voltage		The insulation must not be damaged.	Apply 300% of the rated voltage Based on paragraph 7.1 for 1 to 5s then measure.
Temperature characteristics		Within 0±30ppm / °C	The temperature coefficients in table 12, paragraph 7.12 are calculated at 20°C and high temperature.
Terminal adherence		No detachment or signs of detachment.	Based on JIS C 6429, Appendix 1. Apply 5N (0.51 kgf) for 10 ±1s in the direction  Indicated by the arrow.
Resistance to vibration	Appearance	There must be no mechanical damage.	Chip is mounted to a board in the manner shown on the right, subjected to vibration (type A in paragraph 8.2), and measured 24±2 hrs later. 
	Rate of capacitance change	Must be within initial tolerance.	
	Dissipation factor	Must satisfy initial specified value.	
Solderability		At least 3/4 of the surface of the two terminals must be covered with new solder.	Soldering temperature Based on paragraph 8.13: 235±5°C Soldering time: 2±0.5s
Resistance to solder heat	Appearance	There must be no mechanical damage.	Based on JIS C 6429, Appendix 3. Soldering temperature: 260±5°C Soldering time: 5±0.5s Preheating: 150±10°C for 1 to 2 min.
	Rate of capacitance change	±2.5% or less, or ±0.25 pF or less, whichever is larger	
	Dissipation factor	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
	Withstanding voltage	The insulation must not be damaged.	
Temperature cycling	Appearance	There must be no mechanical damage.	Based on paragraph 9.3. Number of cycles: 10 Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±2.5% or less, or ±0.25 pF or less, whichever is larger.	
	Dissipation factor	Must satisfy initial specified value.	
	Insulation resistance	10,000 MΩ or larger, or 500 ΩF or larger, whichever is smaller	
Humidity load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.9, Test temperature : 40±2°C Relative humidity: 90% - 95% Applied voltage: rated voltage Test time: 500 to 524 hrs. Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±7.5% or less, or ±0.75 pF or less, whichever is larger.	
	Dissipation factor	0.5% or less	
	Insulation resistance	500 MΩ or larger, or 25 ΩF or larger, whichever is smaller	
High-temperature load test	Appearance	There must be no mechanical damage.	Based on paragraph 9.10, Test temperature : Max. operating temp. Applied voltage: rated voltage x 200% Test time: 1,000 to 1,048 hrs. Capacitance measured after 24±2 hrs.
	Rate of capacitance change	±3.0% or less, or ±0.3 pF or less, whichever is larger.	
	Dissipation factor	0.3% or less	
	Insulation resistance	10,000 MΩ or larger, or 50 ΩF or larger, whichever is smaller	

Ceramic Capacitors

Multi-layer ceramic network chip capacitors

●Packaging

(Units: mm)



●Electrical characteristics

Rate of capacitance change vs. temperature characteristics

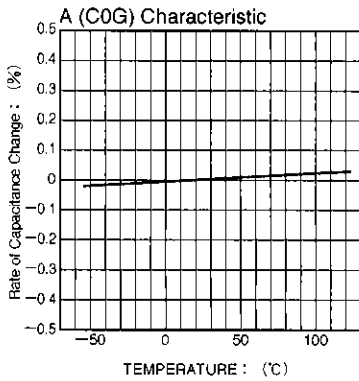


Fig.1

Rate of capacitance change vs. DC voltage characteristics

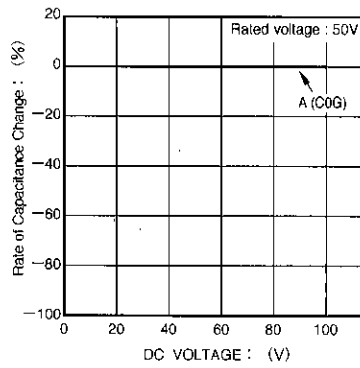


Fig.2

Impedance vs. frequency characteristics

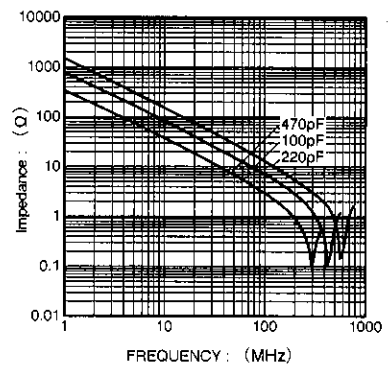


Fig.3

● Electrical characteristics

Temperature cycling test

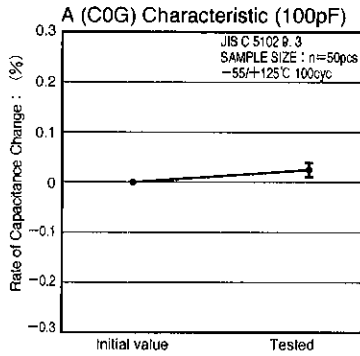


Fig. 4 Rate of capacitance change

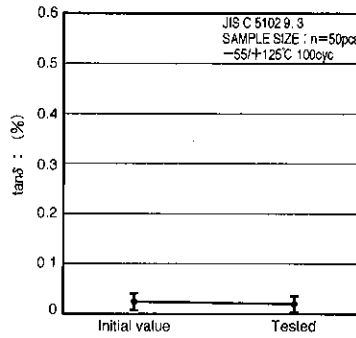


Fig. 5 Dissipation factor

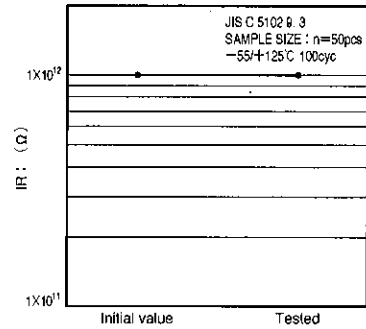


Fig. 6 Insulation resistance

High-temperature load test

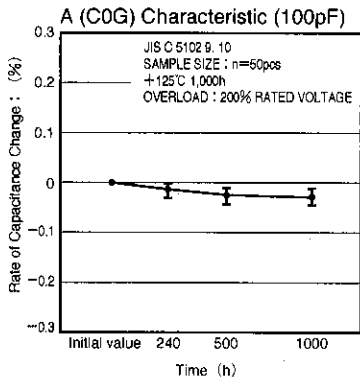


Fig. 7 Rate of capacitance change

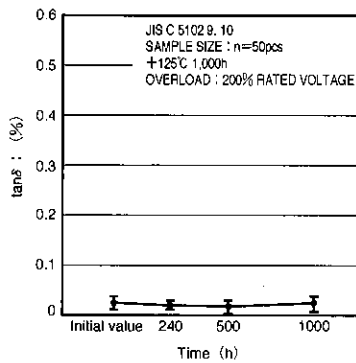


Fig. 8 Dissipation factor

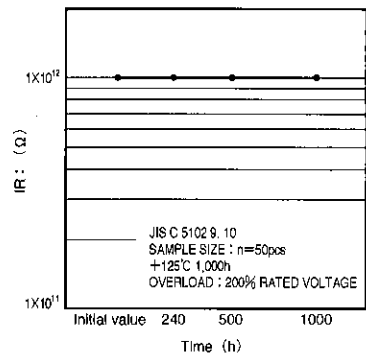


Fig. 9 Insulation resistance

Humidity load test

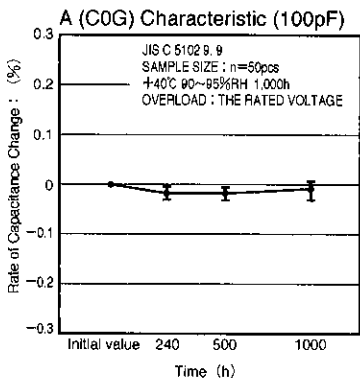


Fig. 10 Rate of capacitance change

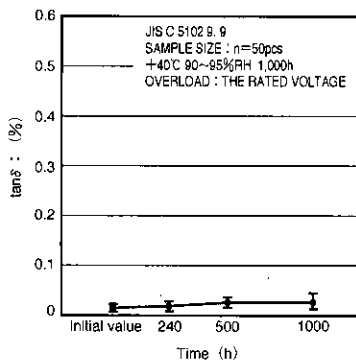


Fig. 11 Dissipation factor

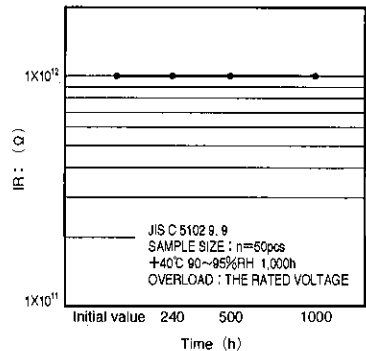


Fig. 12 Insulation resistance

Ceramic Capacitors
Multi-layer ceramic network chip capacitors

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