

# FLASH MEMORY CARD

## 3V-ONLY FLASH MINIATURE CARD

### MB98D81123(2MB)/81223(4MB)-15

#### 2M/4M-BYTE 3 V-ONLY FLASH MINIATURE CARD

The Fujitsu Flash Miniature cards conform to "Miniature Card Specification" published by MCIF; Miniature Card Implementers Forum.

The Fujitsu Flash Miniature cards are small form factor Flash memory cards targeted various markets; digital photography, audio recording, hand held PCs and other small portable equipments. Miniature cards' high performance, small size (38 mm × 33 mm × 3.5 mm), low cost and simple interface are ideal for portable applications that require high speed flash disk drives or eExecute In Place (XIP).

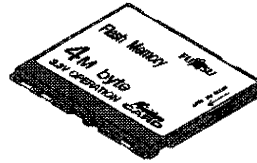
The Flash Miniature cards are 5 V-only operational and allow the users to use as ×8 or ×16 organization on low power at high speed.

- Small size: 33.0 mm (length) × 38.0 mm (width) × 3.5 mm (thickness)
- +3.3 V power supply program and erase
- Command control for Automated Program/Automated Erase operation
- Erase Suspend Read/Program Capability
- 128 KB Sector Erase (at ×16 mode)
- Any Combination of Sectors Erase and Full Chip Erase
- Detection of completion of program/erase operation with Data# Polling or Toggle bit.
- Ready/Busy Output with BUSY#
- Reset Function with RESET# pin
- Write protect function with WP switch
- Low VCC Write Inhibit
- AIS (Attribute Information Structure) is available from the address "0000H" of Lower Byte.

# MB98D81123/81223-15

## ■ PACKAGE

3 V - ONLY FLASH MINIATURE CARD



(CRD-60P-M02)

## ■ DESCRIPTION

### DIFFERENCES

|                       | MB98D81123 | MB98D81223 |
|-----------------------|------------|------------|
| Density               | 2 MB       | 4 MB       |
| Memory Device         | 8 M bit    | 8 M bit    |
| Quantity              | 2          | 4          |
| Read                  | 1 B unit   | ←          |
| Program               | 1 B unit   | ←          |
| Chip Erase            | 1 MB unit  | 1 MB unit  |
| Sector Erase          | 64 KB unit | ←          |
| Number of Sectors     | 32         | 64         |
| Erase Suspend Read    | Yes        | Yes        |
| Erase Suspend Program | Yes        | Yes        |
| Address               | A0 to A19  | A0 to A20  |
| RESET#                | Yes        | Yes        |
| BUSY#                 | Yes        | Yes        |

**MB98D81123/81223-15****■ PAD ASSIGNMENTS**

| Pad No | Symbol          | Pad No | Symbol          | Pad No | Symbol          | Pad No | Symbol            |
|--------|-----------------|--------|-----------------|--------|-----------------|--------|-------------------|
| 1      | A <sub>18</sub> | 16     | N.C.            | 31     | A <sub>19</sub> | 46     | CD#               |
| 2      | A <sub>16</sub> | 17     | N.C.            | 32     | A <sub>17</sub> | 47     | N.C.              |
| 3      | A <sub>14</sub> | 18     | OE#             | 33     | A <sub>15</sub> | 48     | BUSY#             |
| 4      | N.C.            | 19     | D <sub>15</sub> | 34     | A <sub>13</sub> | 49     | WE#               |
| 5      | CEH#            | 20     | D <sub>13</sub> | 35     | A <sub>12</sub> | 50     | D <sub>14</sub>   |
| 6      | A <sub>11</sub> | 21     | D <sub>12</sub> | 36     | RESET#          | 51     | RFU               |
| 7      | A <sub>9</sub>  | 22     | D <sub>10</sub> | 37     | A <sub>10</sub> | 52     | D <sub>11</sub>   |
| 8      | A <sub>8</sub>  | 23     | D <sub>9</sub>  | 38     | VS1#            | 53     | VS2#              |
| 9      | A <sub>6</sub>  | 24     | D <sub>0</sub>  | 39     | A <sub>7</sub>  | 54     | D <sub>8</sub>    |
| 10     | A <sub>5</sub>  | 25     | D <sub>2</sub>  | 40     | N.C.            | 55     | D <sub>1</sub>    |
| 11     | A <sub>3</sub>  | 26     | D <sub>4</sub>  | 41     | A <sub>4</sub>  | 56     | D <sub>3</sub>    |
| 12     | A <sub>2</sub>  | 27     | N.C.            | 42     | CEL#            | 57     | D <sub>5</sub>    |
| 13     | A <sub>0</sub>  | 28     | D <sub>7</sub>  | 43     | A <sub>1</sub>  | 58     | D <sub>6</sub>    |
| 14     | N.C.            | 29     | N.C.            | 44     | N.C.            | 59     | N.C.              |
| 15     | N.C.            | 30     | N.C.            | 45     | N.C.            | 60     | A <sub>20</sub> * |
| EX 1   | V <sub>CC</sub> | EX 2   | GND             | EX 3   | CINS#           |        |                   |

\* : A<sub>20</sub> is "N.C." for MB98D81123.

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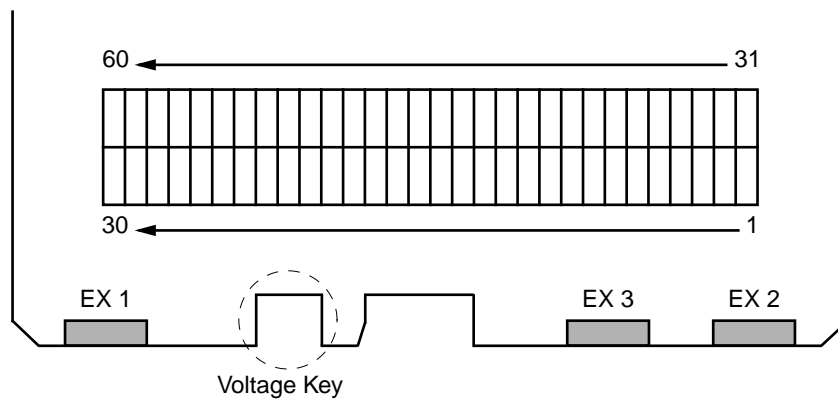
## ■ PAD DESCRIPTIONS

| Symbol                            | I/O | Pad Name                   | Symbol          | I/O | Pad Name       |
|-----------------------------------|-----|----------------------------|-----------------|-----|----------------|
| A <sub>0</sub> to A <sub>20</sub> | I   | Address Input              | BUSY#           | O   | Ready/Busy     |
| D <sub>0</sub> to D <sub>15</sub> | I/O | Data Input/Output          | CD#             | O   | Card Detect *  |
| CEL#                              | I   | Card Enable for Lower Byte | VS1#, VS2#      | O   | Voltage Sense  |
| CEH#                              | I   | Card Enable for Upper Byte | N.C.            | —   | Non Connection |
| OE#                               | I   | Output Enable              | V <sub>CC</sub> | —   | Power Supply   |
| WE#                               | I   | Write Enable               | GND             | —   | Ground         |
| RESET#                            | I   | Hardware Reset             | CINS#           | O   | Card Insertion |

\* : Take notice that those pads are connected internally.

## ■ PAD LOCATIONS

Fig. 1 — BOTTOM VIEW



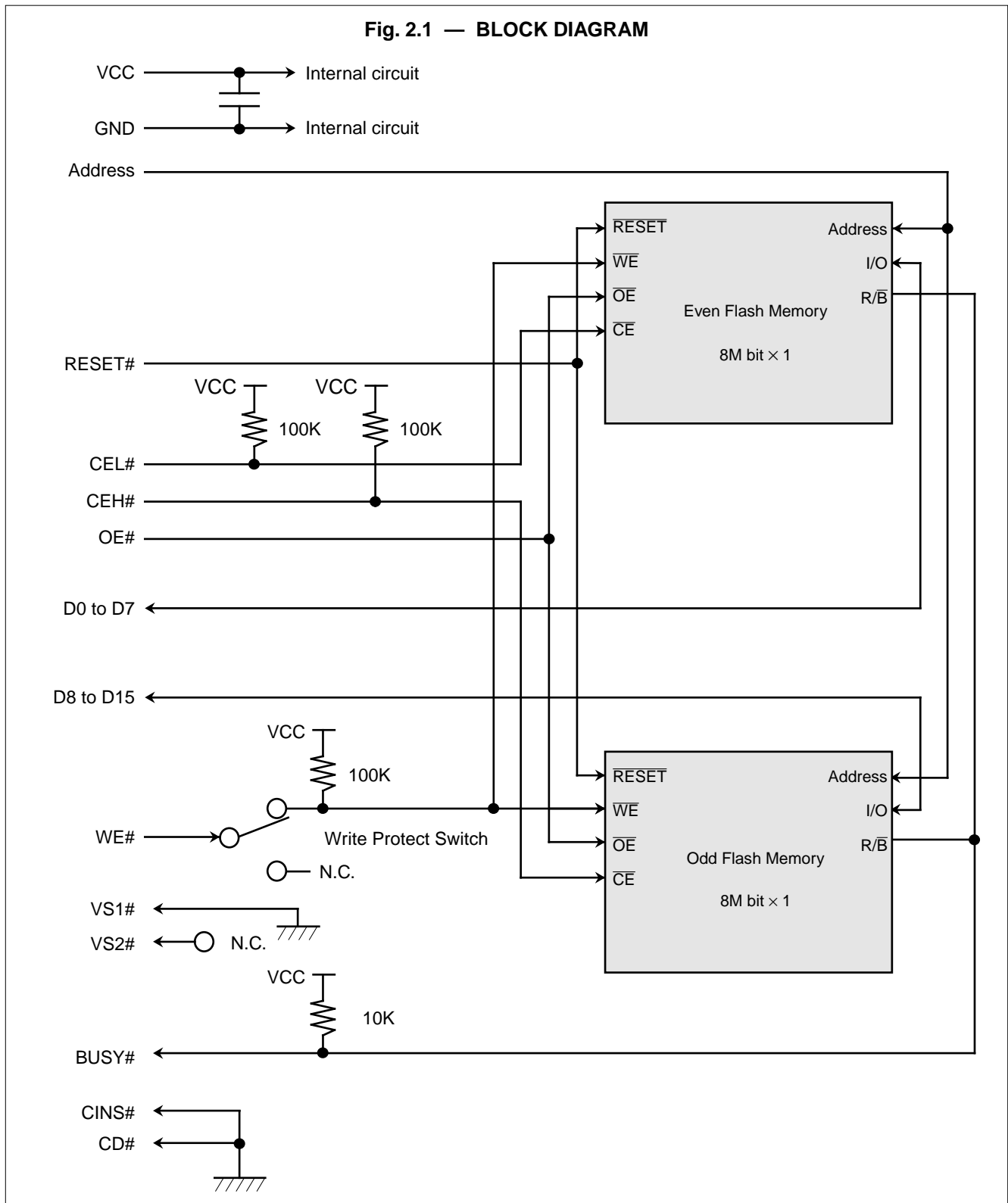
Voltage Key: See "UNIQUE FEATURES".

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## ■ BLOCK DIAGRAM

### MB98D81123

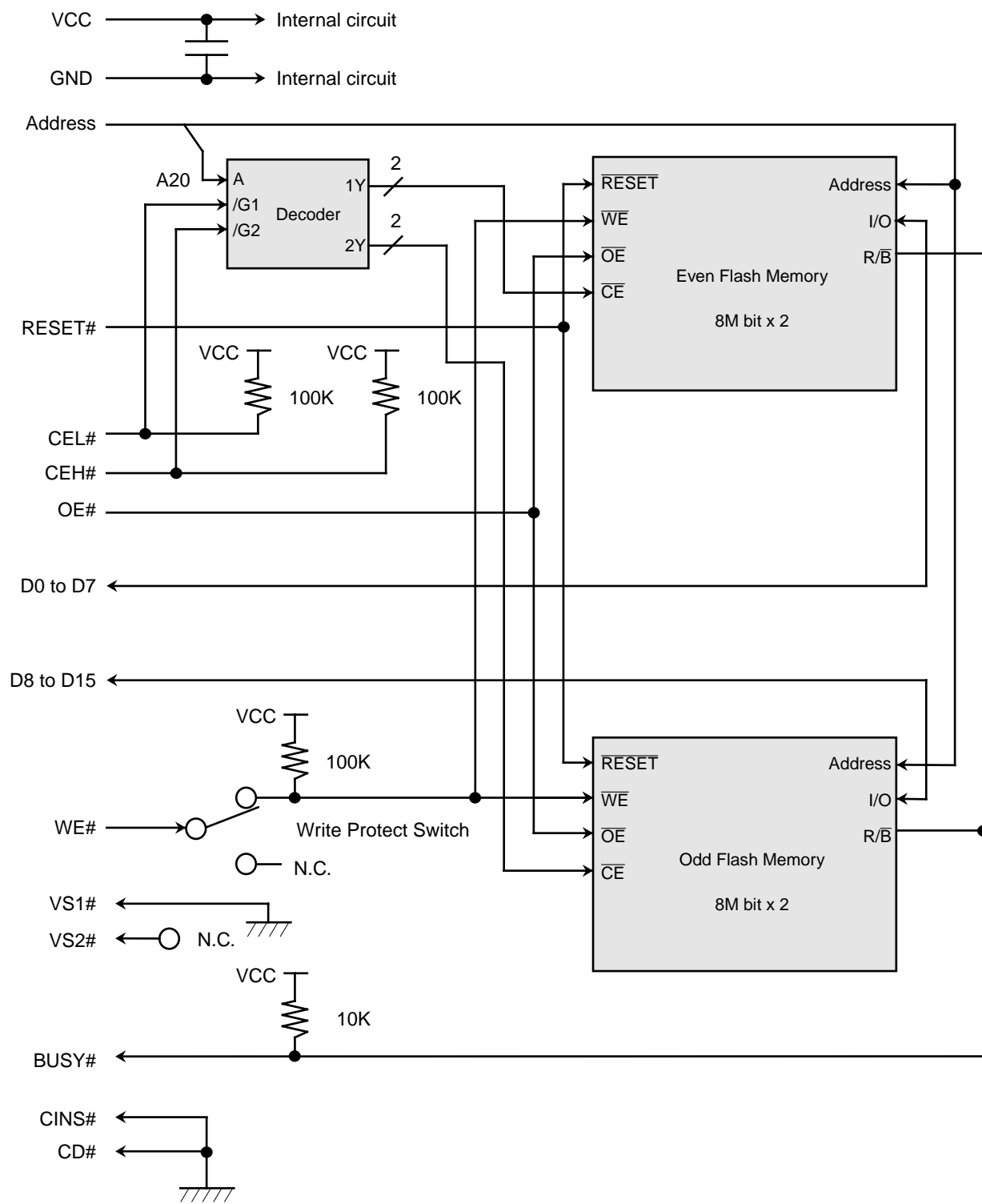
Fig. 2.1 — BLOCK DIAGRAM



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## MB98D81223

Fig. 2.2 — BLOCK DIAGRAM



## ■ CHIP AND SECTOR DECODING

### ERASE SECTOR DECODING TABLE

|                                | Sector Address (SA) |                 |                 |                 |
|--------------------------------|---------------------|-----------------|-----------------|-----------------|
|                                | A <sub>19</sub>     | A <sub>18</sub> | A <sub>17</sub> | A <sub>16</sub> |
| Sector 15                      | 1                   | 1               | 1               | 1               |
| Sector 14                      | 1                   | 1               | 1               | 0               |
| Sector 13                      | 1                   | 1               | 0               | 1               |
| Total 16 sectors<br>per 1 chip | •                   | •               | •               | •               |
|                                | •                   | •               | •               | •               |
|                                | •                   | •               | •               | •               |
|                                | •                   | •               | •               | •               |
| Sector 2                       | 0                   | 0               | 1               | 0               |
| Sector 1                       | 0                   | 0               | 0               | 1               |
| Sector 0                       | 0                   | 0               | 0               | 0               |

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## ■ CHIP CONFIGURATION

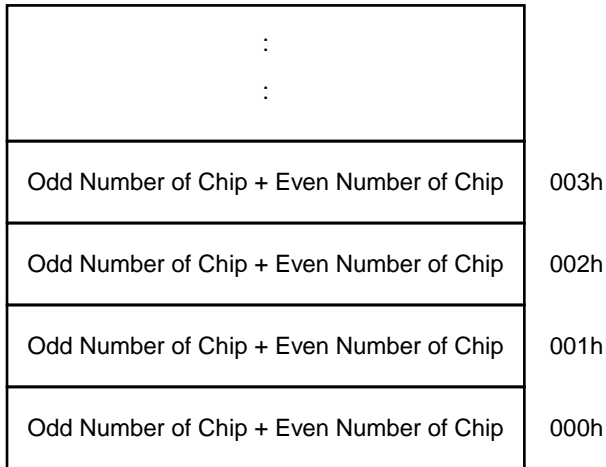
The miniature cards use 2 or 4 pcs of Flash Memory.

- 2 pcs of Flash Memory are operated simultaneously at 16 bit mode and even number of chip is applied to lower byte and odd number of chip is applied to upper byte.

At ×8 bit mode, even address and odd address are selected with CEL# and CEH#.

### ① × 16 bit mode

CEL# = "L", CEH# = "L"

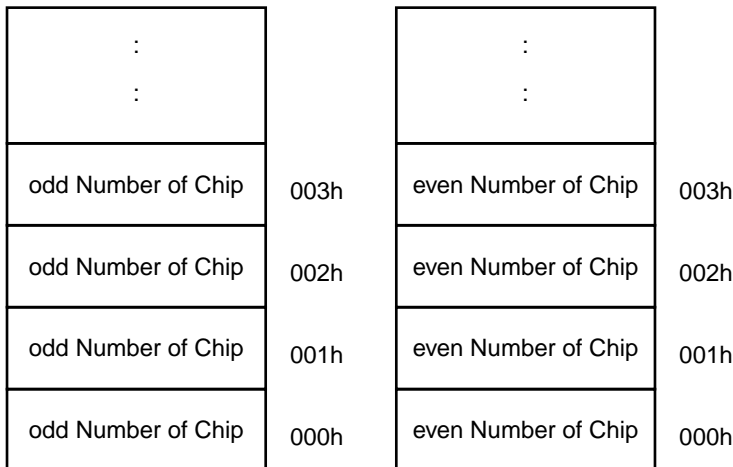


D15 • • • • • D0

### ② × 8 bit mode

CEL# = "H", CEH# = "L"

CEL# = "L", CEH# = "H"



D15 • • • • D8

D7 • • • • D0



## ■ FUNCTION DESCRIPTIONS

### 1. Read Mode

The data in the common can be read with "OE#=VIL" and "WE#=VIH". The address is selected with A0-A20. And CEL# and CEH# select output mode.

### 2. Standby Mode

- CEL# and CEH# at "VIH" place the card in Standby mode. D0-D15 are placed in a high-Z state independent of the status "OE#" and "WE#".

### 3. Output Disable Mode

- The outputs are disabled with OE# and WE# at "VIH". D0-D15 are placed in high-Z state.

### 4. Write Mode

#### 1) Common Memory Write

- The card is in Write mode with "OE#=VIH" and "WE# and CE#=VIL".
- Commands can be written at the Write mode.
- Two types of the Write mode, "WE# control" and "CE# control" are available.

### 5. Command Definitions

- User can select the card operation by writing the specific address and data sequences into the command register. If incorrect address and data are written or improper sequence is done, the card is reset to read mode. See "COMMAND DEFINITION TABLE".

### 6. Automated Program Capability

- Programming operation can switch the data from "1" to "0".
- The data is programmed on a byte-by-byte or word-by-word basis.
- The card will automatically provide adequate internally generated programming pulses and verify the programmed cell margin by writing four bus cycle operation. The card returns to Common Memory Read mode automatically after the programming is completed.
- Addresses are latched at falling edge of WE# or CE# and data is latched at rising edge of WE# or CE#. The fourth rising edge of WE# or CE# on the command write cycle begins programming operation.
- We can check whether a byte (word) programming operation is completed successfully by sequence flag with BUSY#, Data# Polling or Toggle Bit function. See "WRITE OPERATION STATUS".
- Any commands written to the chip during programming operation will be ignored.

### 7. Automated Chip Erase Capability

- We can execute chip erase operation by 6 bus cycle operation. Chip erase does not require the user to program the chip prior to erase. Upon executing the Erase command sequence the chip automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timing during these operations.
- The card returns to Common Memory Read mode automatically after the chip erasing is completed.
- Whether or not chip erase operation is completed successfully can be checked by sequence flag with BUSY#, Data# Polling or Toggle Bit function. See "WRITE OPERATION STATUS".
- Any commands written to the chip during programming operation will be ignored.

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## 8. Automated Sector Erase Capability

- We can execute the erase operation on any sectors by 6 bus cycle operation.
- A time-out of 50  $\mu$ s (typ.) from the rising edge of the last Sector Erase command will initiate the Sector Erase command(s).
- Multiple sectors in a chip can be erased concurrently. This sequence is followed with writes of 30H to addresses in other sectors desired to be concurrently erased. The time between writes 30H must be less than 50  $\mu$ s, otherwise that command will not be accepted. Any command other than Sector Erase or Erase Suspend during this time-out period will reset the chip to Read mode. The automated sector erase begins after the 50  $\mu$ s (typ.) time out from the rising edge of WE# pulse for the last Sector Erase command pulse. Whether the sector erase window is still open can be monitored with D3 and D11.
- Sector Erase does not require the user to program the chip prior to erase. The chip automatically programs “0” to all memory locations in the sector(s) prior to electrical erase. The system is not required to provide any controls or timing during these operations.
- The card returns to Common Memory Read mode automatically after the chip erasing is completed.
- Whether or not sector erase operation is completed successfully can be checked by sequence flug with BUSY#, Data# Polling or Toggle Bit function. The sequence flug must be read from the address of the sector involved in erase operation. See “WRITE OPERATION STATUS”.

## 9. Erase Suspend

- Erase Suspend command allows the user to interrupt the sector erase operation and then do data reads or program from or to a non-busy sector in the chip which has the sector(s) suspended erase. This command is applicable only during the sector erase operation (including the sector erase time-out period after the sector erase commands 30H) and will be ignored if written during the chip erase or programming operation. Writing this command during the time-out will result in immediate termination of the time-out period. The addresses are “don’t cares” in writing the Erase Suspend or Resume commands in the chip.
- When the Erase Suspend command is written during a Sector Erase operation, the chip will enter the Erase Suspend Read mode. User can read the data from other sectors than those in suspension. The read operation from sectors in suspension results D<sub>2</sub>/D<sub>10</sub> toggling. User can program to non-busy sectors by writing program commands.
- A read from a sector being erase suspended may result in invalid data.

## 10. Intelligent Identifier (ID) Read Mode

- Each common memory can execute an Intelligent Identifier operation, initiated by writing Intelligent ID command (90H). Following the command write, a read cycle from address 00H retrieves the manufacture code, and a read cycle from address 01H returns the device code as follows. To terminate the operation, it is necessary to write Read/Reset command.

## 11. Hardware Reset

- The Card may be reset by driving the RESET# pin to VIL. The RESET# pin must be kept High (VIL) for at least 500 ns. Any operation in progress will be terminated and the card will be reset to the read mode 20  $\mu$ s after the RESET# pin is driven Low. If a hardware reset occurs during a program operation, the data at that particular location will be indeterminate.
- When the RESET# pin is Low and the internal reset is complete, the Card goes to standby mode and cannot be accessed. Also, note that all the data output pins are High-Z for the duration of the RESET# pulse. Once the RESET# pin is taken high, the Card requires 500 ns of wake up time until outputs are valid for read access.
- If hardware reset occurs during a erase operation, there is a possibility that the erasing sector(s) cannot be used.

## 12. Data Protection

- The card has WP (Write Protect) switch for write lockout.
- To avoid initiation of a write cycle during  $V_{CC}$  power-up and power-down, a write cycle is locked out for  $V_{CC}$  less than 3.2 V. If  $V_{CC} < V_{LKO}$ , the command register is disabled and all internal program/erase circuits are disabled.  
Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the  $V_{CC}$  level is greater than  $V_{LKO}$ . It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when  $V_{CC}$  is above 3.2 V.
- If  $V_{CC}$  would be less than  $V_{LKO}$  during program/erase operation, the operation will stop. And after that, the operation will not resume even if  $V_{CC}$  returns recommended voltage level. Therefore, program command must be written again because the data on the address interrupted program operation is invalid. And regarding interrupting erase operation, there is possibility that the erasing sector(s) cannot be used.
- Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# will not initiate a write cycle.

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## ■ FUNCTION TRUTH TABLE

| Mode            | RESET# | CEH# | CEL# | OE#    | WE#    | WPSW *1 | Data Input/Output |          |        |
|-----------------|--------|------|------|--------|--------|---------|-------------------|----------|--------|
|                 |        |      |      |        |        |         | D8 to D15         | D0 to D7 |        |
| Hardware Reset  | L      | X    | X    | X      | X      | P or NP | High-Z            | High-Z   |        |
| Standby         | H      | H    | H    | X      | X      | P or NP | High-Z            | High-Z   |        |
| Read (×8 bit)   |        | H    | L    | L      | H      | P or NP | High-Z            | DOUT     |        |
|                 |        | L    | H    |        |        |         | DOUT              | High-Z   |        |
| Read (×16 bit)  |        | L    | L    | H      | L      | NP      | DOUT              | DOUT     |        |
| Write (×8 bit)  |        | H    | L    |        |        |         | High-Z            | DIN      |        |
|                 |        | L    | H    |        |        |         | DIN               | High-Z   |        |
| Write (×16 bit) |        | L    | L    |        |        |         | DIN               | DIN      |        |
| Output Disable  |        | H    | L    |        |        |         | P                 | High-Z   | High-Z |
|                 |        | L    | H    |        |        |         |                   | High-Z   | High-Z |
|                 |        | L    | L    | High-Z | High-Z |         |                   |          |        |

H : "H" level, L : "L" level , X : "H" or "L"

**Note:** \*1. WPSW = Write Protect Switch, NP = NON-PROTECT, P = PROTECT

## ■ COMMAND DEFINITION TABLE

### Command Table for 8-bit Mode

| Command                   | Bus Cycle | 1st Bus Write Cycle |     | 2nd Bus Write/Read Cycle |     | 3rd Bus Write Cycle |     | 4th Bus Write/Read Cycle |     | 5th Bus Write Cycle |     | 6th Bus Write Cycle |     |
|---------------------------|-----------|---------------------|-----|--------------------------|-----|---------------------|-----|--------------------------|-----|---------------------|-----|---------------------|-----|
| Read/Reset 1              | 2         | Write               |     | Read                     |     |                     |     |                          |     |                     |     |                     |     |
|                           |           | CA                  | F0H | RA                       | RD  |                     |     |                          |     |                     |     |                     |     |
| Read/Reset 2              | 4         | Write               |     | Write                    |     | Write               |     | Read                     |     |                     |     |                     |     |
|                           |           | CA                  | AAH | CA                       | 55H | CA                  | F0H | RA                       | RD  |                     |     |                     |     |
| Read Intelligent ID Codes | 4         | Write               |     | Write                    |     | Write               |     | Read                     |     |                     |     |                     |     |
|                           |           | CA                  | AAH | CA                       | 55H | CA                  | 90H | IA                       | ID  |                     |     |                     |     |
| Byte Program              | 4         | Write               |     | Write                    |     | Write               |     | Write                    |     |                     |     |                     |     |
|                           |           | CA                  | AAH | CA                       | 55H | CA                  | A0H | PA                       | PD  |                     |     |                     |     |
| Sector Erase              | 6         | Write               |     | Write                    |     | Write               |     | Write                    |     | Write               |     | Write               |     |
|                           |           | CA                  | AAH | CA                       | 55H | CA                  | 80H | CA                       | AAH | CA                  | 55H | SA                  | 30H |
| Chip Erase                | 6         | Write               |     | Write                    |     | Write               |     | Write                    |     | Write               |     | Write               |     |
|                           |           | CA                  | AAH | CA                       | 55H | CA                  | 80H | CA                       | AAH | CA                  | 55H | CA                  | 10H |
| Sector Erase Suspend      | 1         | Write               |     |                          |     |                     |     |                          |     |                     |     |                     |     |
|                           |           | CA                  | B0H |                          |     |                     |     |                          |     |                     |     |                     |     |
| Sector Erase Resume       | 1         | Write               |     |                          |     |                     |     |                          |     |                     |     |                     |     |
|                           |           | CA                  | 30H |                          |     |                     |     |                          |     |                     |     |                     |     |

**Note:** CA: Chip Address. (address in chip selected by A20 for MB98D81223)  
 SA: Sector Address (address in 64 KB selected by A16, A17, A18, A19 and A20)  
 PA: Program Address (address to be programmed)  
 RA: Read Address (address to be read)  
 IA: Intelligent ID read address (Manufacture Code 0000H, Device Code 0001H)

PD: Programming data  
 RD: Read data  
 ID: Intelligent Identifier (ID) Code

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## Command Table for 16-bit Mode

| Command                   | Bus Cycle | 1st Bus Write Cycle |       | 2nd Bus Write/Read Cycle |       | 3rd Bus Write Cycle |       | 4th Bus Write/Read Cycle |       | 5th Bus Write Cycle |       | 6th Bus Write Cycle |       |
|---------------------------|-----------|---------------------|-------|--------------------------|-------|---------------------|-------|--------------------------|-------|---------------------|-------|---------------------|-------|
| Read/Reset 1              | 2         | Write               |       | Read                     |       |                     |       |                          |       |                     |       |                     |       |
|                           |           | CA                  | F0F0H | RA                       | RD    |                     |       |                          |       |                     |       |                     |       |
| Read/Reset 2              | 4         | Write               |       | Write                    |       | Write               |       | Read                     |       |                     |       |                     |       |
|                           |           | CA                  | AAAAH | CA                       | 5555H | CA                  | F0F0H | RA                       | RD    |                     |       |                     |       |
| Read Intelligent ID Codes | 4         | Write               |       | Write                    |       | Write               |       | Read                     |       |                     |       |                     |       |
|                           |           | CA                  | AAAAH | CA                       | 5555H | CA                  | 9090H | IA                       | ID    |                     |       |                     |       |
| Byte Program              | 4         | Write               |       | Write                    |       | Write               |       | Write                    |       |                     |       |                     |       |
|                           |           | CA                  | AAAAH | CA                       | 5555H | CA                  | A0A0H | PA                       | PD    |                     |       |                     |       |
| Sector Erase              | 6         | Write               |       | Write                    |       | Write               |       | Write                    |       | Write               |       | Write               |       |
|                           |           | CA                  | AAAAH | CA                       | 5555H | CA                  | 8080H | CA                       | AAAAH | CA                  | 5555H | SA                  | 3030H |
| Chip Erase                | 6         | Write               |       | Write                    |       | Write               |       | Write                    |       | Write               |       | Write               |       |
|                           |           | CA                  | AAAAH | CA                       | 5555H | CA                  | 8080H | CA                       | AAAAH | CA                  | 5555H | CA                  | 1010H |
| Sector Erase Suspend      | 1         | Write               |       |                          |       |                     |       |                          |       |                     |       |                     |       |
|                           |           | CA                  | B0B0H |                          |       |                     |       |                          |       |                     |       |                     |       |
| Sector Erase Resume       | 1         | Write               |       |                          |       |                     |       |                          |       |                     |       |                     |       |
|                           |           | CA                  | 3030H |                          |       |                     |       |                          |       |                     |       |                     |       |

**Note:** CA: Chip Address. (address in chip selected by A20 for MB98D81223)  
 SA: Sector Address (address in 128 KB selected by A16, A17, A18, A19 and A20)  
 PA: Program Address (address to be programmed)  
 RA: Read Address (address to be read)  
 IA: Intelligent ID read address (Manufacture Code 0000H, Device Code 0001H)

PD: Programming data

RD: Read data

ID: Intelligent Identifier (ID) Code

## ■ WRITE OPERATION STATUS

### Hardware Sequence Flag Table

| Status               |                       | D <sub>7</sub> , D <sub>15</sub>    | D <sub>6</sub> , D <sub>14</sub> | D <sub>5</sub> , D <sub>13</sub> | D <sub>3</sub> , D <sub>11</sub> | D <sub>2</sub> , D <sub>10</sub> | BUSY#                 |   |
|----------------------|-----------------------|-------------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-----------------------|---|
| In Progress          | Programming           | D <sub>7</sub> #, D <sub>15</sub> # | Toggle                           | 0                                | 0                                | 1                                | 0                     |   |
|                      | Erasing               | 0                                   | Toggle                           | 0                                | 1                                | Toggle                           | 0                     |   |
|                      | Erase Suspend Read    | (1)                                 | 1                                | 1                                | 0                                | 0                                | Toggle * <sub>1</sub> | 1 |
|                      |                       | (2)                                 | Data                             | Data                             | Data                             | Data                             | Data                  | 1 |
|                      | Erase Suspend Program | D <sub>7</sub> #, D <sub>15</sub> # | Toggle * <sub>2</sub>            | 0                                | 0                                | * <sub>1</sub> , * <sub>3</sub>  | 0                     |   |
| Exceeded Time Limits | Programming           | D <sub>7</sub> #, D <sub>15</sub> # | Toggle                           | 1                                | 0                                | 1                                | 0                     |   |
|                      | Erasing               | 0                                   | Toggle                           | 1                                | 1                                | N/A                              | 0                     |   |
|                      | Erase Suspend Program | D <sub>7</sub> #, D <sub>15</sub> # | Toggle                           | 1                                | 0                                | N/A                              | 0                     |   |

(1): Erase Suspended Sector (2): Non-Erase Suspended Sector

- Notes:**
- \*1. Performing successive read operations from the erase-suspended sector will cause D<sub>2</sub>, D<sub>10</sub> to toggle.
  - \*2. Performing successive read operations from any address will cause D<sub>6</sub>, D<sub>14</sub> to toggle.
  - \*3. Reading the byte address being programmed while in the erase-suspend program mode will indicate logic '1' at the D<sub>2</sub>, D<sub>10</sub> bit. However, successive reads from the erase-suspended sector will cause D<sub>2</sub>, D<sub>10</sub> to toggle.

### D<sub>7</sub>, D<sub>15</sub> (Data# Polling)

The card features Data# Polling as a method to indicate to the host that the Program/Erase Operation are in progress or completed. During the program operation an attempt to read the program address will produce the compliment of the data last written to D<sub>7</sub>/D<sub>15</sub>. Upon completion of the program operation, an attempt to read the program address will produce the true data last written to D<sub>7</sub>/D<sub>15</sub>. During the erase operation, an attempt to read the program address will produce a "0" at the D<sub>7</sub>/D<sub>15</sub> output. Upon completion of the erase operation an attempt to read the device will produce a "1" at the D<sub>7</sub>/D<sub>15</sub> output.

For Chip Erase, the Data# Polling is valid after the rising edge of the sixth WE# pulse in the six write pulse sequence. For sector erase, the Data# Polling is valid after the last rising edge of the sector erase WE# pulse. Even if the device has completed the operation and D<sub>7</sub>/D<sub>15</sub> has a valid data, the data outputs on D<sub>0</sub> to D<sub>6</sub>/D<sub>8</sub> to D<sub>14</sub> may be still invalid. The valid data on D<sub>0</sub> to D<sub>7</sub>/D<sub>8</sub> to D<sub>15</sub> will be read on the successive read attempts.

The Data# Polling feature is only active during the programming operation, erase operation, sector erase time-out, Erase Suspend Read mode and Erase Suspend Program mode.

### D<sub>6</sub>, D<sub>14</sub> (Toggle Bit I)

The card also features the "Toggle Bit" as a method to indicate to the host system that the Program/Erase Operation are in progress or completed.

During an Program or Erase cycle, successive attempts to read (OE# or CE# toggling) data from the card will result in D<sub>6</sub>/D<sub>14</sub> toggling between one and zero. Once the Program or Erase cycle is completed, D<sub>6</sub>/D<sub>14</sub> will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth WE# pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth WE# pulse in the six write pulse sequence. For sector erase, the Toggle Bit is valid after the last rising edge of the sector erase WE# pulse. The Toggle Bit is also active during the sector time out.

Either CE# or OE# toggling will cause the D<sub>6</sub>/D<sub>14</sub> to toggle.

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## D5, D13 (Exceeded Timing Limits)

D<sub>5</sub>/D<sub>13</sub> will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions D<sub>5</sub>/D<sub>13</sub> will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data# Polling is the only operating function of the card under this condition. If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The chip must be reset to use other sectors. Write the Reset command sequence to the chip, and then execute Program or Erase command sequence. This allows the system to continue to use the other active sectors in the chip.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The D<sub>5</sub>/D<sub>13</sub> failure condition may also appear if a user tries to program a non blank location without erasing. In this case the card locks out and never completes the card operation. Hence, the system never reads a valid data on D<sub>7</sub>/D<sub>15</sub> bit and D<sub>6</sub>/D<sub>14</sub> never stops toggling. Once the card has exceeded timing limits, the D<sub>5</sub>/D<sub>13</sub> bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

## D3, D11 (Sector Erase Timer)

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D<sub>3</sub>/D<sub>11</sub> will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the card has been written with a valid erase command, D<sub>3</sub>/D<sub>11</sub> may be used to determine if the sector erase timer window is still open. If D<sub>3</sub>/D<sub>11</sub> is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the card will be ignored until the erase operation is completed as indicated by Data# Polling or Toggle Bit. If D<sub>3</sub>/D<sub>11</sub> is low ("0"), the card will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of D<sub>3</sub>/D<sub>11</sub> prior to and following each subsequent sector erase command. If D<sub>3</sub>/D<sub>11</sub> were high on the second status check, the command may not have been accepted.

Refer to Table: Hardware Sequence Flags.

## D2, D10

This Toggle bit, along with D<sub>6</sub>, can be used to determine whether the card is in the Erase operation or in Erase Suspend.

Successive reads from the erasing sector will cause D<sub>2</sub> to toggle during the Erase operation. If the card is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause D<sub>2</sub> to toggle. When the card is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic '1' at the D<sub>2</sub> bit.

D<sub>6</sub> is different from D<sub>2</sub> in that D<sub>6</sub> toggles only when the standard Program or Erase, or Erase Suspend Program operation is in progress.

## BUSY#

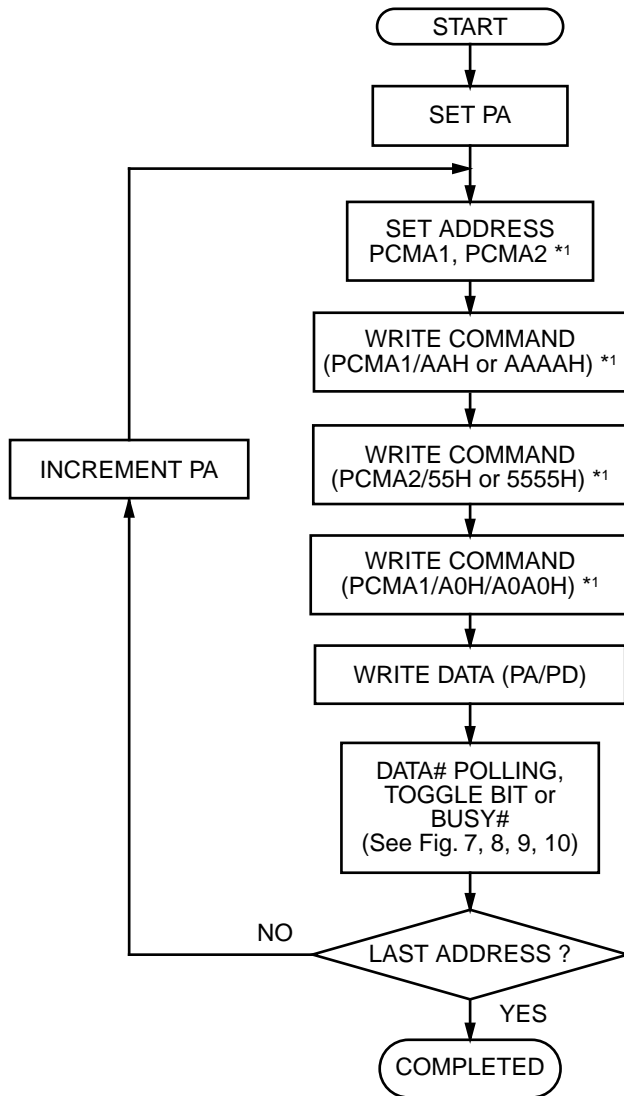
The card provides a BUSY# open-drain output pin as a way to indicate to the system that the program or erase operation are either in progress or has been completed. If the output is low, the card is busy with either a program or erase operation. If the card is placed in an Erase Suspend mode, the BUSY# output will be high.

During programming, the BUSY# pin is driven low after the rising edge of the fourth WE# pulse. During an erase operation, the BUSY# pin is driven low after the rising edge of the sixth WE# pulse. The BUSY# pin will indicate a busy condition during the RESET# pulse.



## PROGRAM/ERASE FLOWCHART

Fig. 3 — PROGRAM FLOWCHART



PD : PROGRAM DATA  
PA : PROGRAM ADDRESS

\*1. See "COMMAND DEFINITION TABLE".

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Fig. 4 — CHIP ERASE FLOWCHART

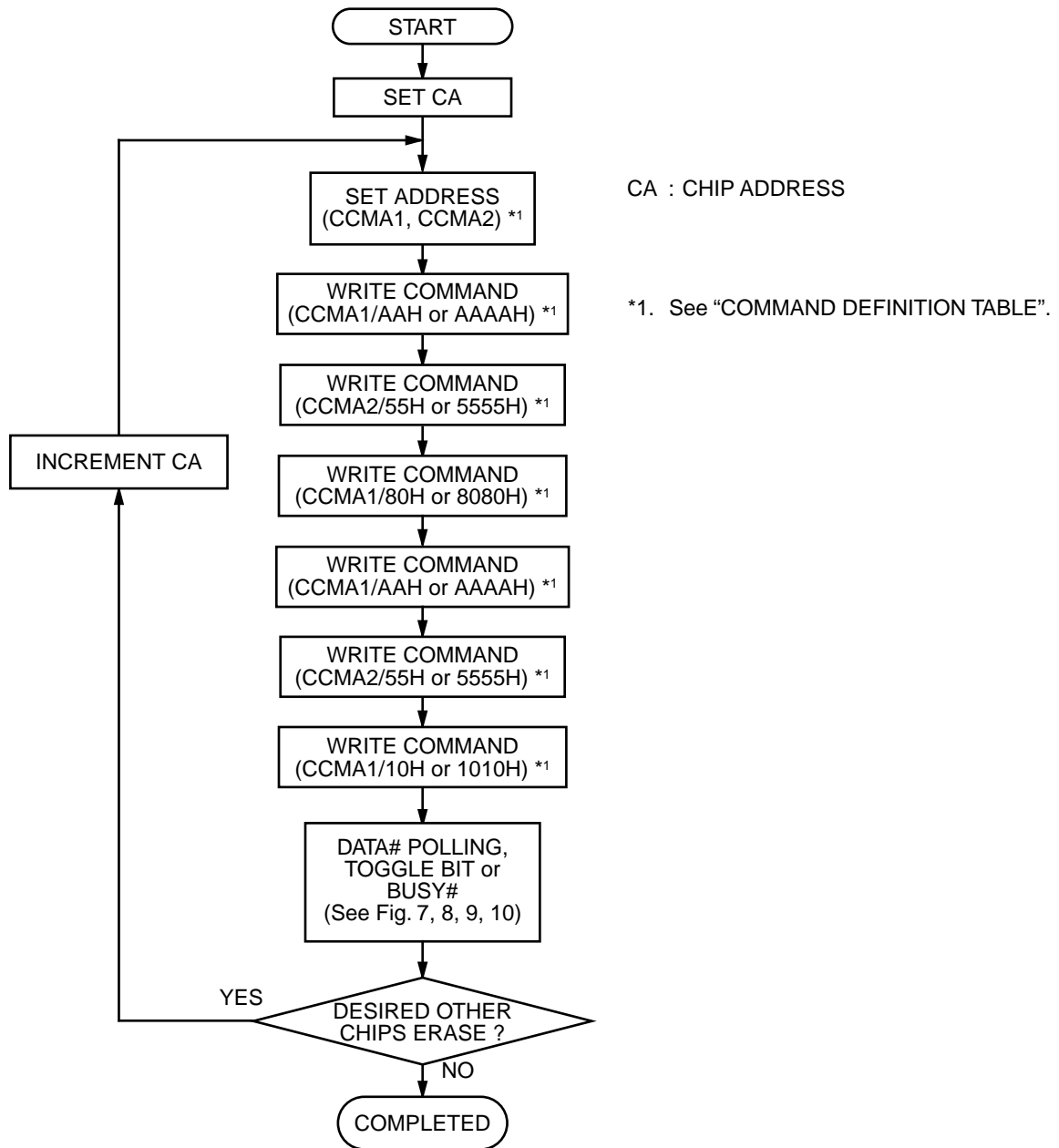
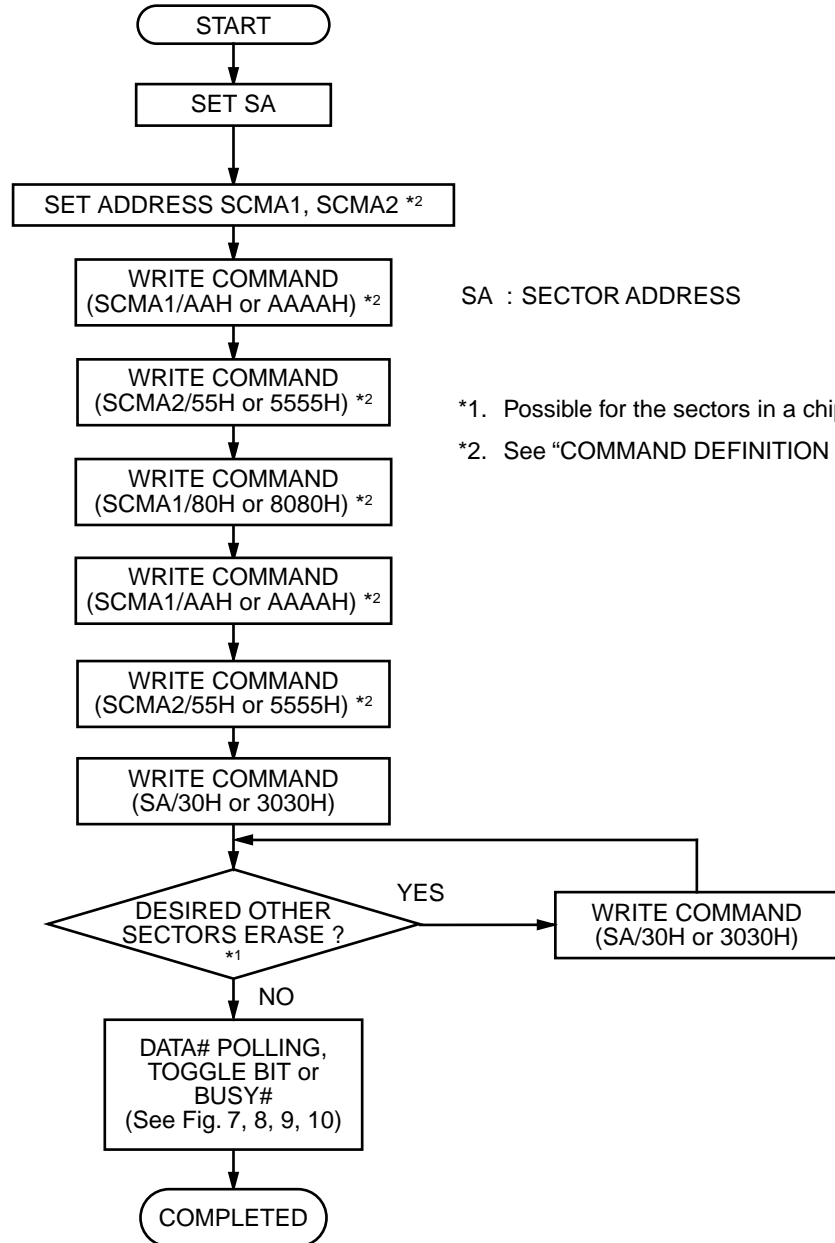
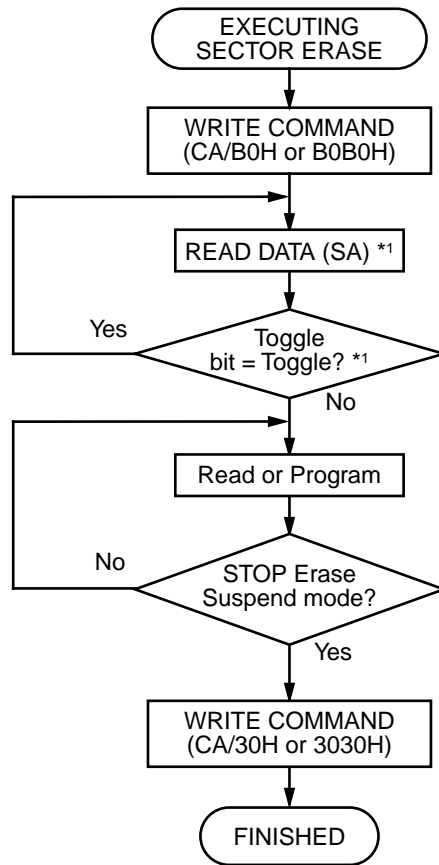


Fig. 5 — SECTOR ERASE FLOWCHART



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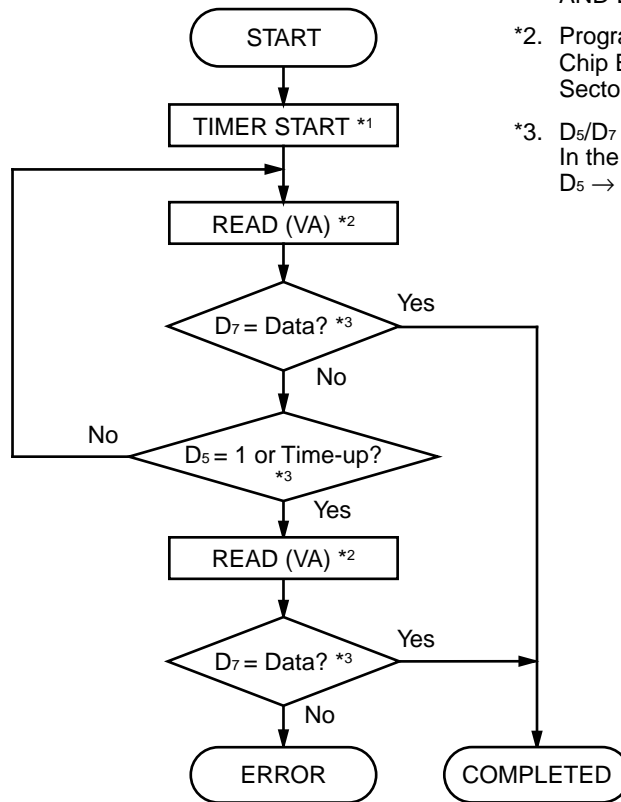
Fig. 6 — ERASE SUSPEND FLOWCHART



CA : CHIP ADDRESS  
SA : SECTOR ADDRESS  
RA : READ ADDRESS

\*1. Detection whether suspend mode is valid can be done by Data# Polling, Toggle Bit or BUSY# also.

Fig. 7 — DATA# POLLING FLOWCHART: x8 bit mode



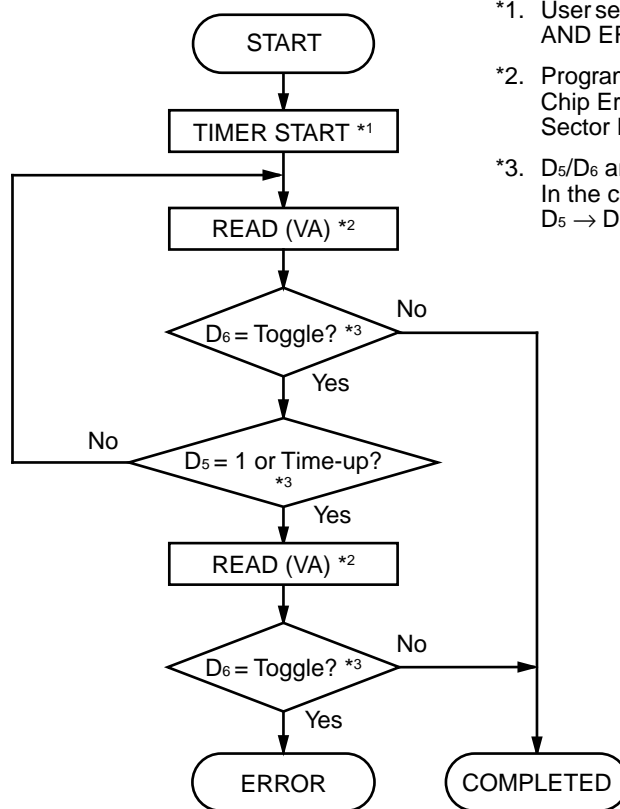
\*1. User sets the time period referring to "PROGRAM AND ERASE PERFORMANCES".

\*2. Program VA = PA  
Chip Erase VA = CA  
Sector Erase VA = SA

\*3. D<sub>5</sub>/D<sub>7</sub> are for even chip(s).  
In the case of odd chip(s),  
D<sub>5</sub> → D<sub>13</sub> and D<sub>7</sub> → D<sub>15</sub> are applied.

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Fig. 8 — TOGGLE BIT FLOWCHART: x8 bit mode

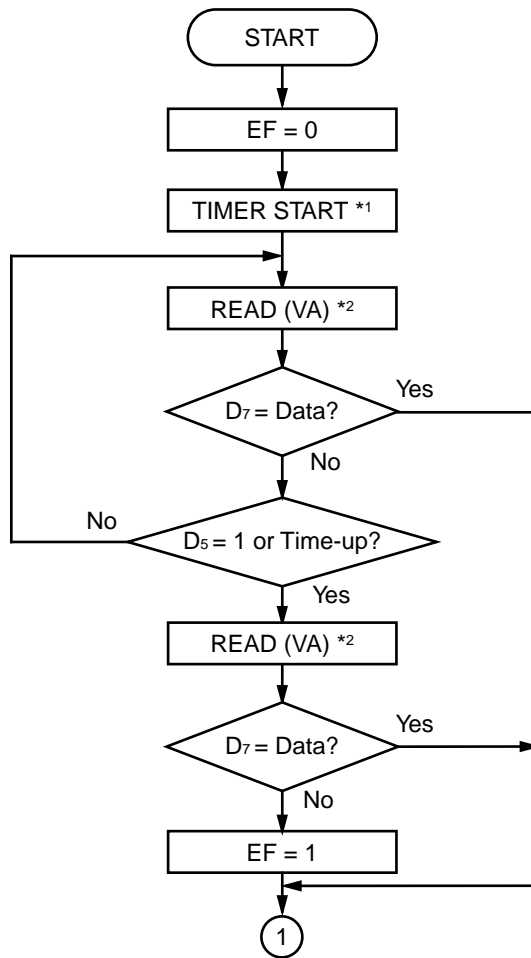


\*1. User sets the time period referring to "PROGRAM AND ERASE PERFORMANCES".

\*2. Program VA = PA  
Chip Erase VA = CA  
Sector Erase VA = SA

\*3. D<sub>5</sub>/D<sub>6</sub> are for even chip(s).  
In the case of odd chip(s),  
D<sub>5</sub> → D<sub>13</sub> and D<sub>6</sub> → D<sub>14</sub> are applied.

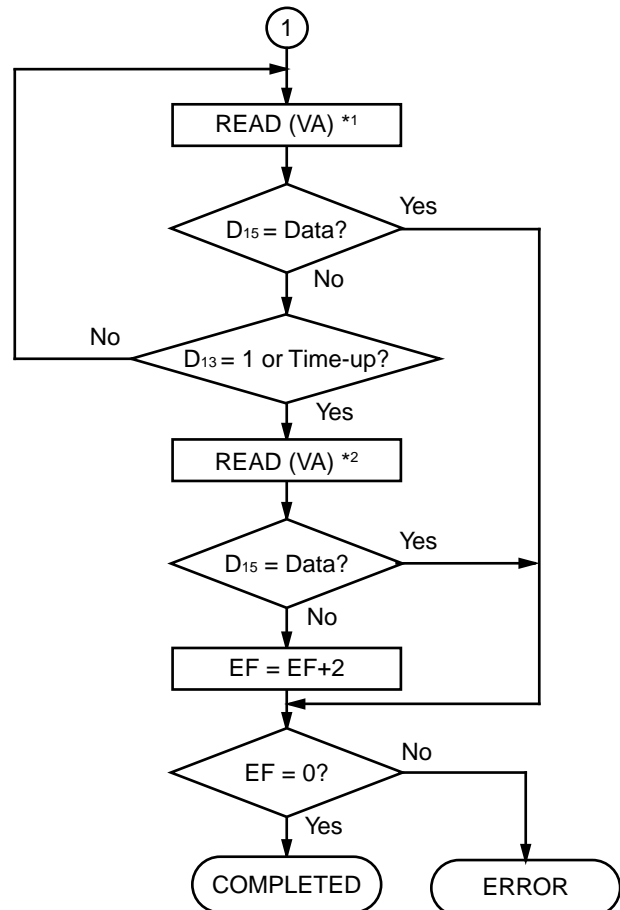
Fig. 9 — DATA# POLLING FLOWCHART: x16 bit mode



\*1. User sets the time period referring to "PROGRAM AND ERASE PERFORMANCES".

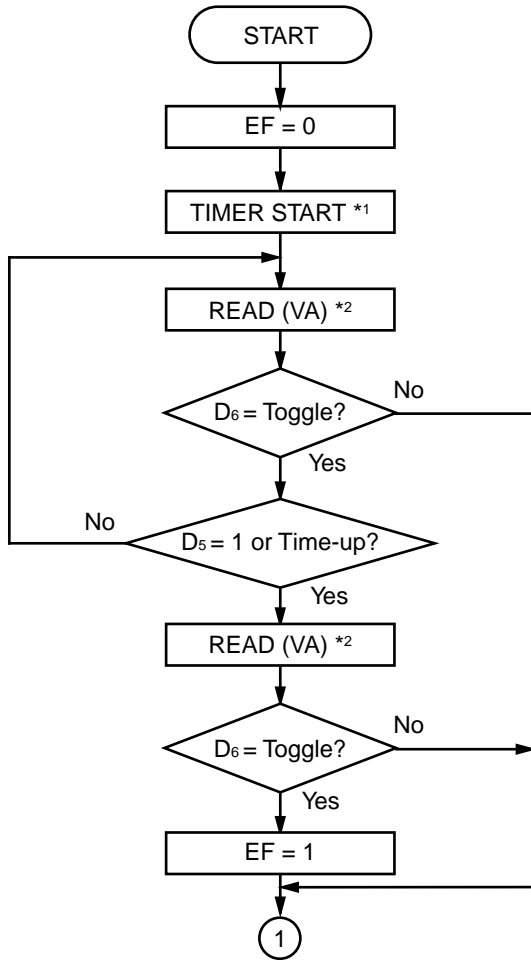
\*2. Program VA = PA  
Chip Erase VA = CA  
Sector Erase VA = SA

EF: Error Flag  
EF = 0: Operation Completed  
EF = 1: Lower Byte Error  
EF = 2: Upper Byte Error  
EF = 3: Lower/Upper Byte Error



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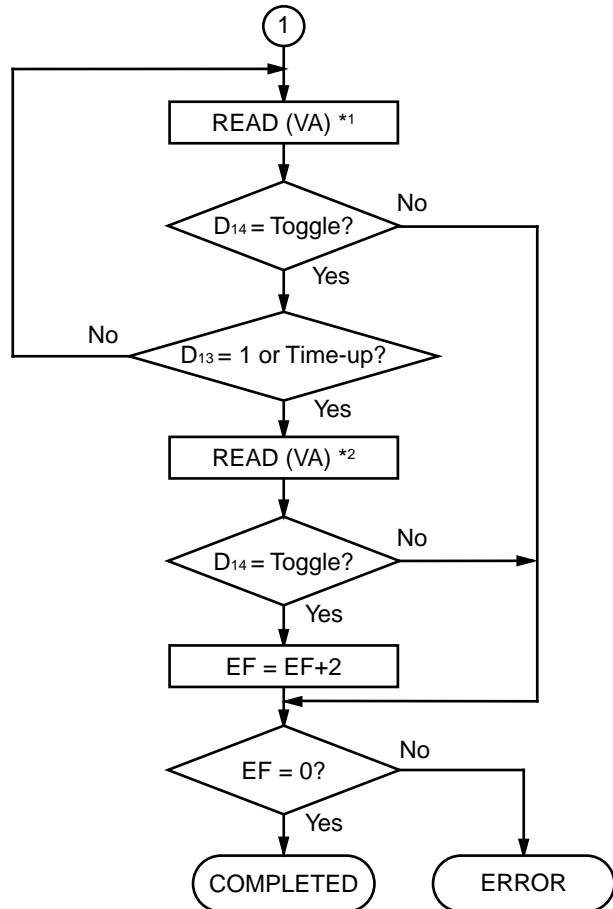
**Fig. 10 — TOGGLE BIT FLOWCHART: x16 bit mode**



\*1. User sets the time period referring to “PROGRAM AND ERASE PERFORMANCES”.

\*2. Program       VA = PA  
 Chip Erase    VA = CA  
 Sector Erase  VA = SA

EF:     Error Flag  
 EF = 0: Operation Completed  
 EF = 1: Lower Byte Error  
 EF = 2: Upper Byte Error  
 EF = 3: Lower/Upper Byte Error





## ■ ABSOLUTE MAXIMUM RATINGS \*1

| Parameter              | Symbol    | Value                  | Unit |
|------------------------|-----------|------------------------|------|
| Supply Voltage         | $V_{CC}$  | -0.5 to +5.5           | V    |
| Input Voltage          | $V_{IN}$  | -0.5 to $V_{CC} + 0.5$ | V    |
| Output Voltage         | $V_{OUT}$ | -0.5 to $V_{CC} + 0.5$ | V    |
| Temperature under Bias | $T_A$     | 0 to +60               | °C   |
| Storage Temperature    | $T_{STG}$ | -30 to +70             | °C   |

\*1. Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter               | Symbol   | Min   | Typ  | Max   | Unit |
|-------------------------|----------|-------|------|-------|------|
| $V_{CC}$ Supply Voltage | $V_{CC}$ | 3.135 | 3.30 | 3.465 | V    |
| Ground                  | GND      |       | 0    |       | V    |
| Ambient Temperature     | $T_A$    | 0     |      | 55    | °C   |

## ■ DC CHARACTERISTICS

| Parameter                     | Test Conditions  | Symbol    | Value        |     |                | Unit          |
|-------------------------------|--|-----------|--------------|-----|----------------|---------------|
|                               |  |           | Min          | Typ | Max            |               |
| Input Leakage Current *1      | $V_{CC} = V_{CC} \text{ max.}, V_{IN} = \text{GND or } V_{CC}$   | $I_{LI}$  |              |     | $\pm 10$       | $\mu\text{A}$ |
| Output Leakage Current *2     | $V_{CC} = V_{CC} \text{ max.}, V_{IN} = \text{GND or } V_{CC}$   | $I_{LO}$  |              |     | $\pm 10$       | $\mu\text{A}$ |
| Standby Current               | CEL#, CEH#,<br>RESET# = $V_{CC} \pm 0.3 \text{ V}$   | $I_{SB1}$ | —            | 10  | 70             | $\mu\text{A}$ |
|                               | CEL#, CEH#, RESET# = $V_{IH}$  | $I_{SB2}$ |              |     | 5.0            | mA            |
| Active Read Current           | $V_{CC} = V_{CC} \text{ max.}, \text{CEL\#, CEH\#} = V_{IL}$<br>Cycle = 150 ns, $I_{OUT} = 0 \text{ mA}$ | $I_{CC1}$ |              | 50  | 80             | mA            |
| Program Current               | Program in progress ( $\times 16$ mode)  | $I_{CC2}$ |              | 60  | 100            | mA            |
| Erase Current                 | Erase in progress ( $\times 16$ mode)  | $I_{CC3}$ |              | 60  | 100            | mA            |
| Input Low Voltage             | —  | $V_{IL}$  | -0.5         | —   | 0.6            | V             |
| Input High Voltage            | —  | $V_{IH}$  | $0.7 V_{CC}$ | —   | $V_{CC} + 0.5$ | V             |
| Output Low Voltage            | $I_{OL} = 4.0 \text{ mA}, V_{CC} = V_{CC} \text{ min.}$  | $V_{OL}$  |              |     | 0.45           | V             |
| Output High Voltage           | $I_{OH} = -2.0 \text{ mA}, V_{CC} = V_{CC} \text{ min.}$   | $V_{OH}$  | 2.4          |     |                | V             |
| Low $V_{CC}$ Lock-out Voltage | —  | $V_{LKO}$ | 2.3          | —   | 2.5            | V             |

**Notes:** \*1. This value does not apply to CEL#, CEH# and WE#.

\*2. This value does not apply to CD# and CINS#.

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## ■ CAPACITANCE ( $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{IN} = V_{IO} = \text{GND}$ )

| Parameter            | Symbol   | Min | Max | Unit |
|----------------------|----------|-----|-----|------|
| Input Capacitance *1 | $C_{IN}$ |     | 40  | pF   |
| I/O Capacitance *2   | $C_{IO}$ |     | 40  | pF   |

**Notes:** \*1. This value does not apply to CEL#, CEH# and WE#.

\*2. This value does not apply to VS1#, CD# and CINS#.

## ■ AC TEST CONDITIONS

- Input Pulse Levels:  $V_{IH} = 3.0\text{ V}$ ,  $V_{IL} = 0.0\text{ V}$
- Input Pulse Rise and Fall Times: 5 ns
- Timing Reference Levels
  - Input:  $V_{IL} = 1.5\text{ V}$ ,  $V_{IH} = 1.5\text{ V}$
  - Output:  $V_{OL} = 1.5\text{ V}$ ,  $V_{OH} = 1.5\text{ V}$
  - Output Load: 1TTL +100 pF

## ■ PROGRAM AND ERASE PERFORMANCES

| Parameter                | Min     | Typ | Max    | Unit          |
|--------------------------|---------|-----|--------|---------------|
| Byte Program Time *1     |         | 8   | 3600   | $\mu\text{s}$ |
| Chip Programming Time *1 |         | 8.4 | T.B.D. | Sec.          |
| Sector Erase Time *2     |         | 1   | 15     | Sec.          |
| Program/Erase Cycles     | 100,000 |     |        | Cycles        |

**Notes:** \*1. Excludes system-level overhead.

\*2. Excludes 00H programming prior to erasure.

## ■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### READ CYCLE \*1

| Parameter                             | Symbol           | Min | Max | Unit |
|---------------------------------------|------------------|-----|-----|------|
| Read Cycle Time                       | t <sub>RC</sub>  | 150 |     | ns   |
| Card Enable Access Time               | t <sub>CE</sub>  |     | 150 | ns   |
| Address Access Time                   | t <sub>ACC</sub> |     | 150 | ns   |
| Output Enable Access Time             | t <sub>OE</sub>  |     | 75  | ns   |
| Card Enable to Output in Low-Z *2     | t <sub>CLZ</sub> | 5   |     | ns   |
| Card Disable to Output in High-Z *2   | t <sub>CHZ</sub> |     | 75  | ns   |
| Output Enable to Output in Low-Z *2   | t <sub>OLZ</sub> | 5   |     | ns   |
| Output Disable to Output in High-Z *2 | t <sub>OHZ</sub> |     | 60  | ns   |
| Output Hold from Address Change       | t <sub>OH</sub>  | 0   |     | ns   |
| Ready Time from RESET#                | t <sub>RDY</sub> |     | 20  | μs   |

**Notes:** \*1. Rise/Fall time < 5 ns.

\*2. Transition is measured at the point of ±500 mV from steady state voltage.

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## PROGRAM/ERASE CYCLE

| Parameter   | Symbol             | Min | Typ | Max | Unit |
|---|--------------------|-----|-----|-----|------|
| Write Cycle Time                                    | t <sub>WC</sub>    | 150 |     |     | ns   |
| Address Setup Time                                  | t <sub>AS</sub>    | 20  |     |     | ns   |
| Address Hold Time                                   | t <sub>AH</sub>    | 20  |     |     | ns   |
| Data Setup Time                                     | t <sub>DS</sub>    | 50  |     |     | ns   |
| Data Hold Time                                      | t <sub>DH</sub>    | 20  |     |     | ns   |
| Read Recovery Time (WE# control)                    | t <sub>GHWL</sub>  | 10  |     |     | ns   |
| Read Recovery Time (CE# control)                    | t <sub>GHEL</sub>  | 10  |     |     | ns   |
| Output Enable Hold Time                             | t <sub>OEH</sub>   | 10  |     |     | ns   |
| Card Enable Setup Time                              | t <sub>CS</sub>    | 0   |     |     | ns   |
| Card Enable Hold Time                               | t <sub>CH</sub>    | 10  |     |     | ns   |
| Write Enable Pulse Width                            | t <sub>WP</sub>    | 80  |     |     | ns   |
| Write Enable Setup Time                             | t <sub>WS</sub>    | 0   |     |     | ns   |
| Write Enable Hold Time                              | t <sub>WH</sub>    | 10  |     |     | ns   |
| Card Enable Pulse Width                             | t <sub>CP</sub>    | 100 |     |     | ns   |
| Duration of Byte Program Operation<br>(/WE Control) | t <sub>WHWH1</sub> |     | 8   |     | μs   |
| Duration of Erase Operation *1<br>(/WE Control)     | t <sub>WHWH2</sub> |     | 1   | 15  | s    |
| Duration of Byte Program Operation<br>(/CE Control) | t <sub>EHEH1</sub> |     | 8   |     | μs   |
| Duration of Erase Operation *1<br>(/CE Control)     | t <sub>EHEH2</sub> |     | 1   | 15  | s    |
| V <sub>CC</sub> Setup Time *2                       | t <sub>VCS</sub>   | 50  |     |     | μs   |
| Reset Pulse Width                                   | t <sub>RP</sub>    | 500 |     |     | ns   |
| Busy Delay Time                                     | t <sub>BSY</sub>   | 90  |     |     | ns   |

**Notes:** \*1. These do not include the preprogramming time.

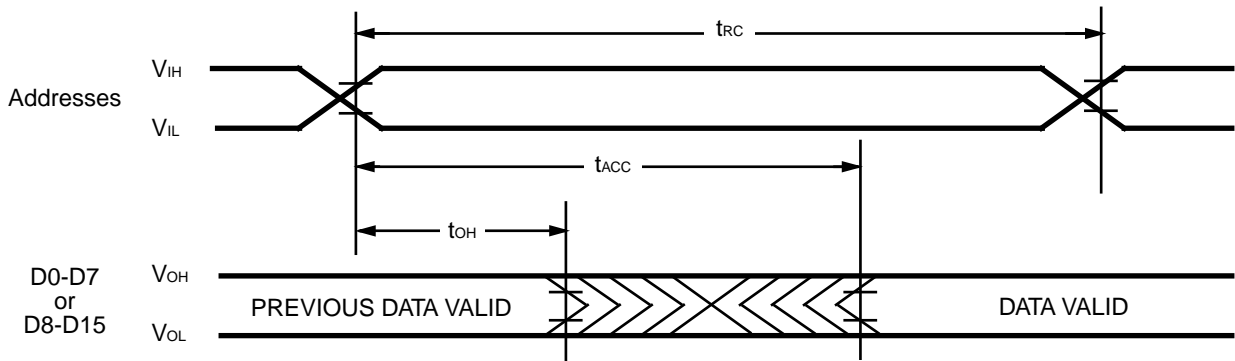
\*2. Not 100% tested.

# MB98D81123/81223-15

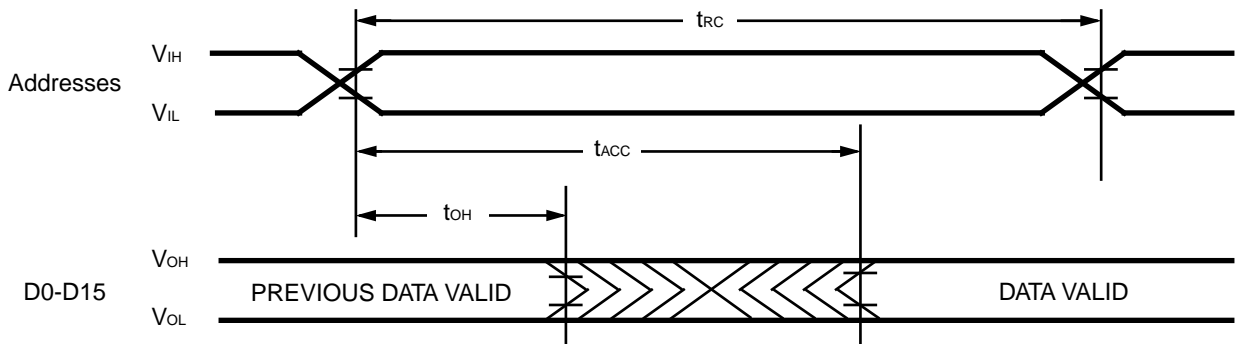
## ■ TIMING DIAGRAM


### READ CYCLE TIMING DIAGRAM (WE# = V<sub>IH</sub>, RESET# = V<sub>IH</sub>)

READ CYCLE (×8 bit mode): "CEL# = OE# = V<sub>IL</sub>, CEH# = V<sub>IH</sub>" or "CEH# = OE# = V<sub>IL</sub>, CEL# = V<sub>IH</sub>"



READ CYCLE (×16 bit mode): CEL# = CEH# = OE# = V<sub>IL</sub>

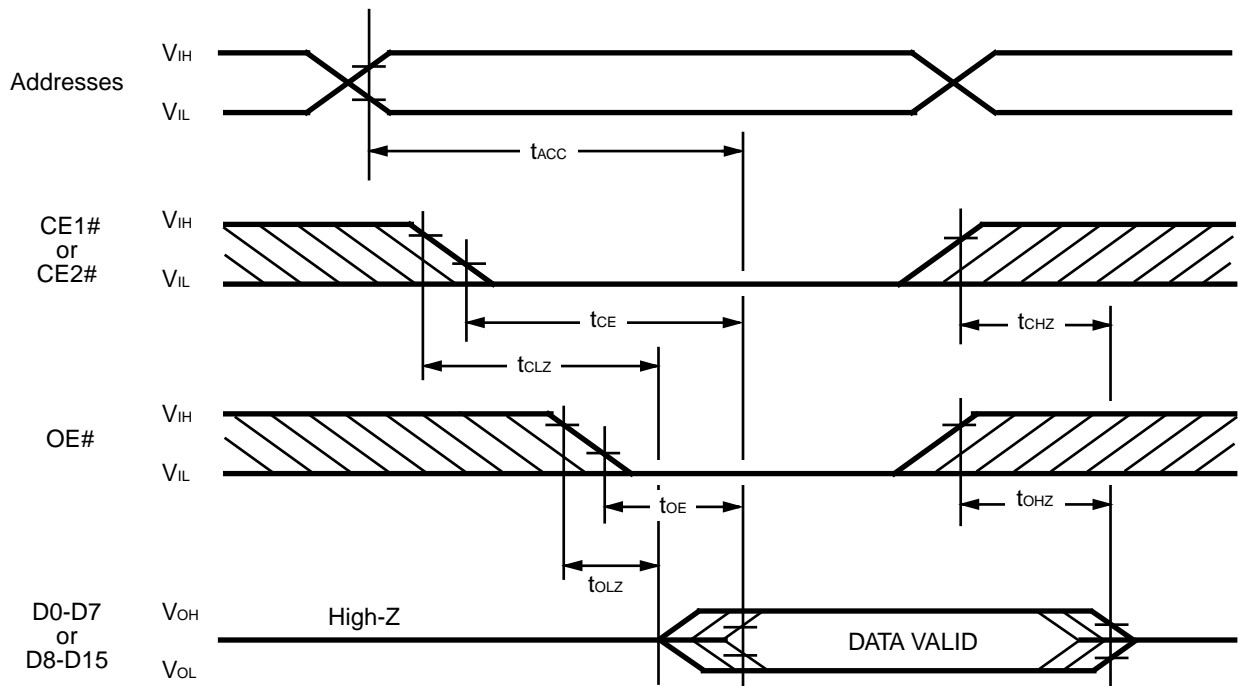



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# MB98D81123/81223-15

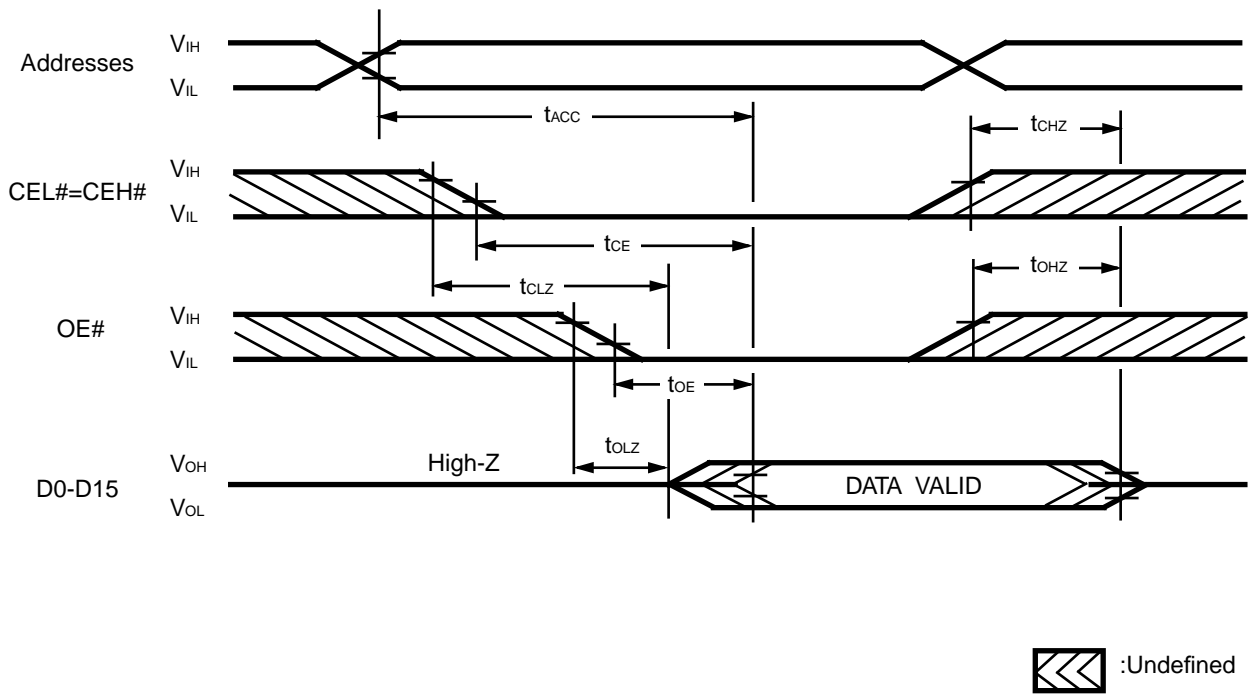
## READ CYCLE TIMING DIAGRAM (continued) (WE# = V<sub>IH</sub>, RESET# = V<sub>IH</sub>)

READ CYCLE 3: x8-bit Bus Organization



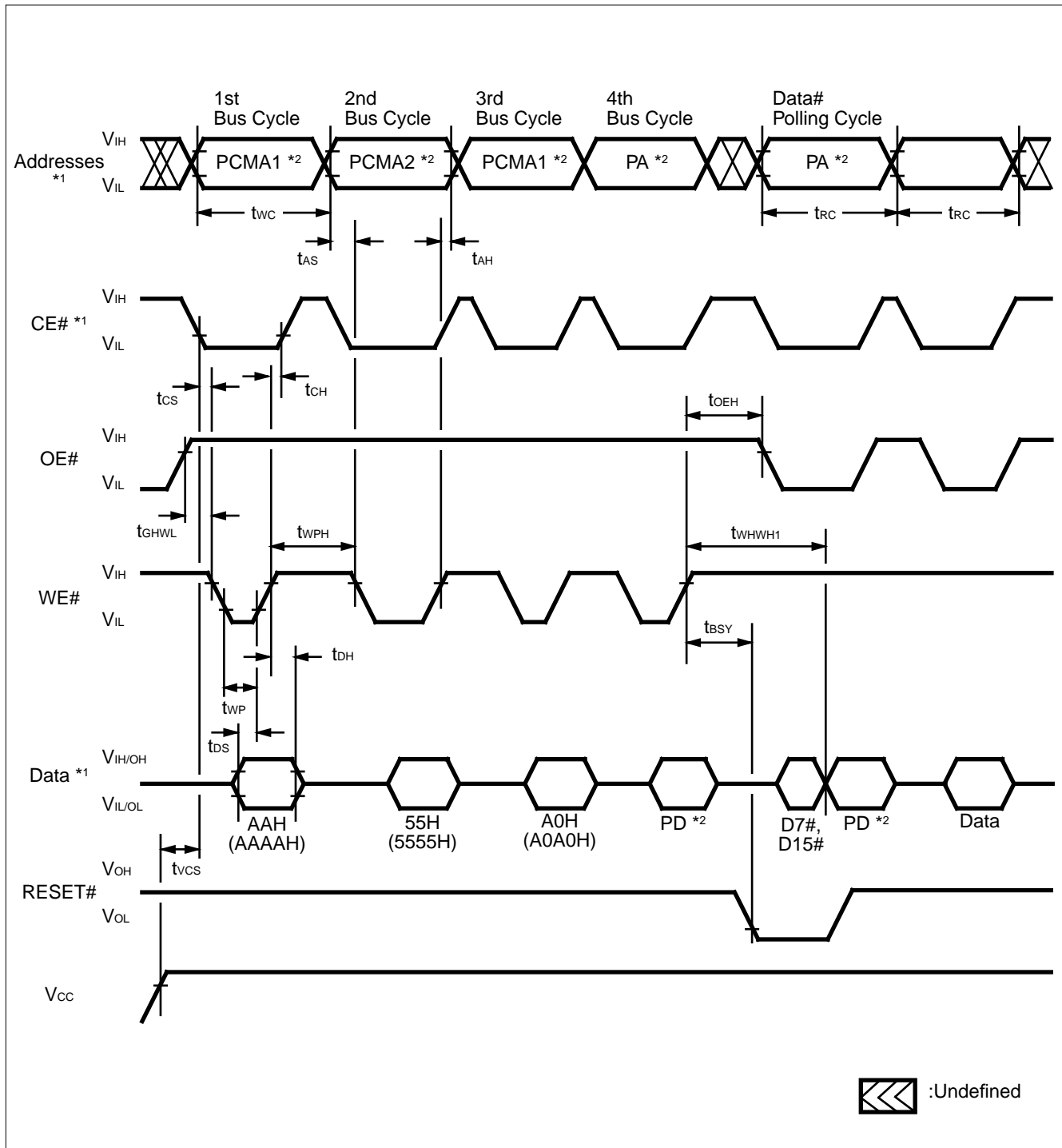
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READ CYCLE TIMING DIAGRAM (continued) (WE# = V<sub>IH</sub>, RESET# = V<sub>IH</sub>)READ CYCLE 4: CEL# = CEH# = V<sub>IL</sub>: ×16-bit Bus Organization

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## PROGRAM CYCLE TIMING DIAGRAM (WE# = CONTROLLED, RESET# = V<sub>IH</sub>)

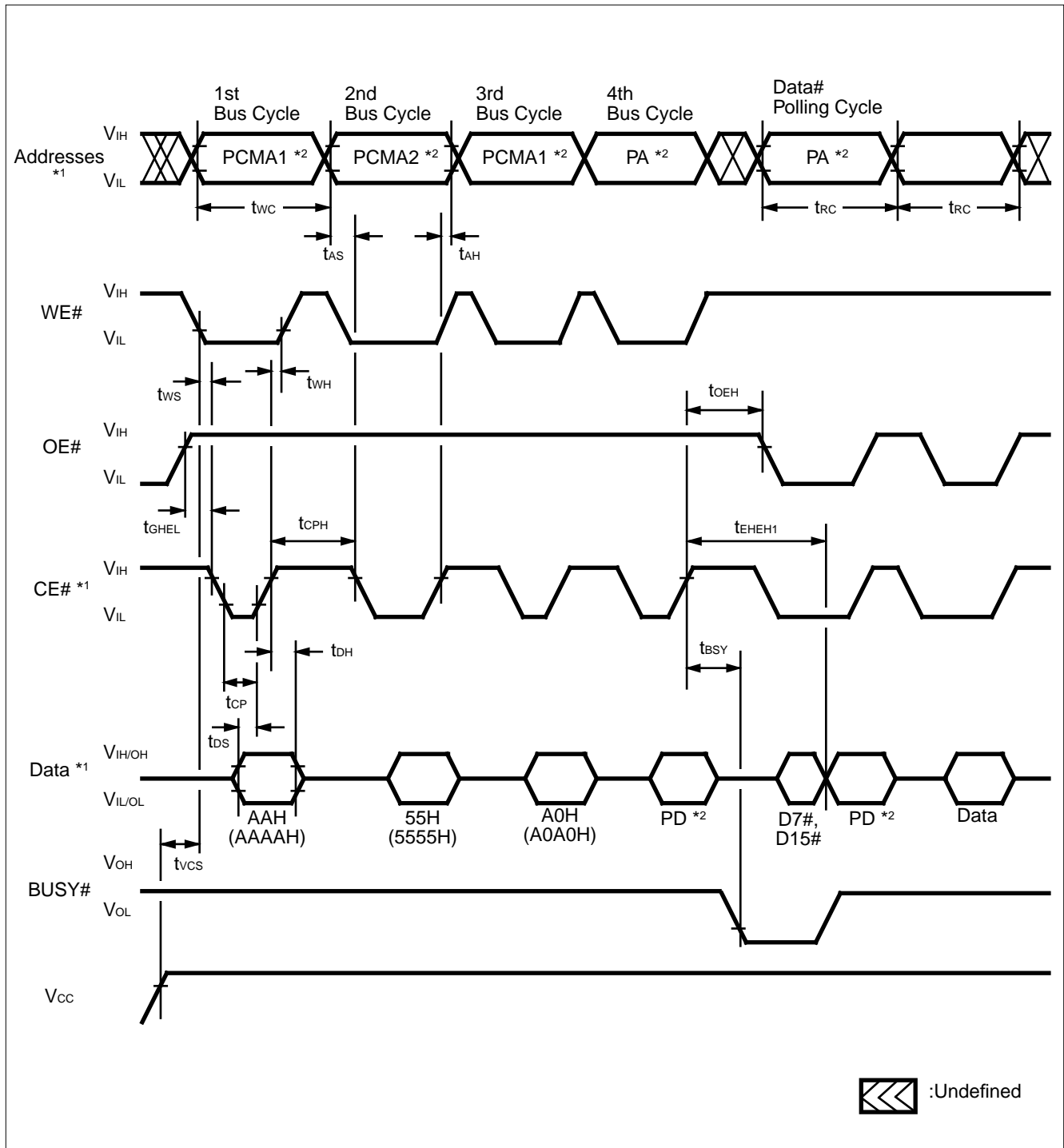


**Notes:** \*1. See "FUNCTION TRUTH TABLE".

\*2. PCMA1/PCMA2 = Command Address for Program, PA = Program Address, PD = Program Data. See "COMMAND DEFINITION TABLE".



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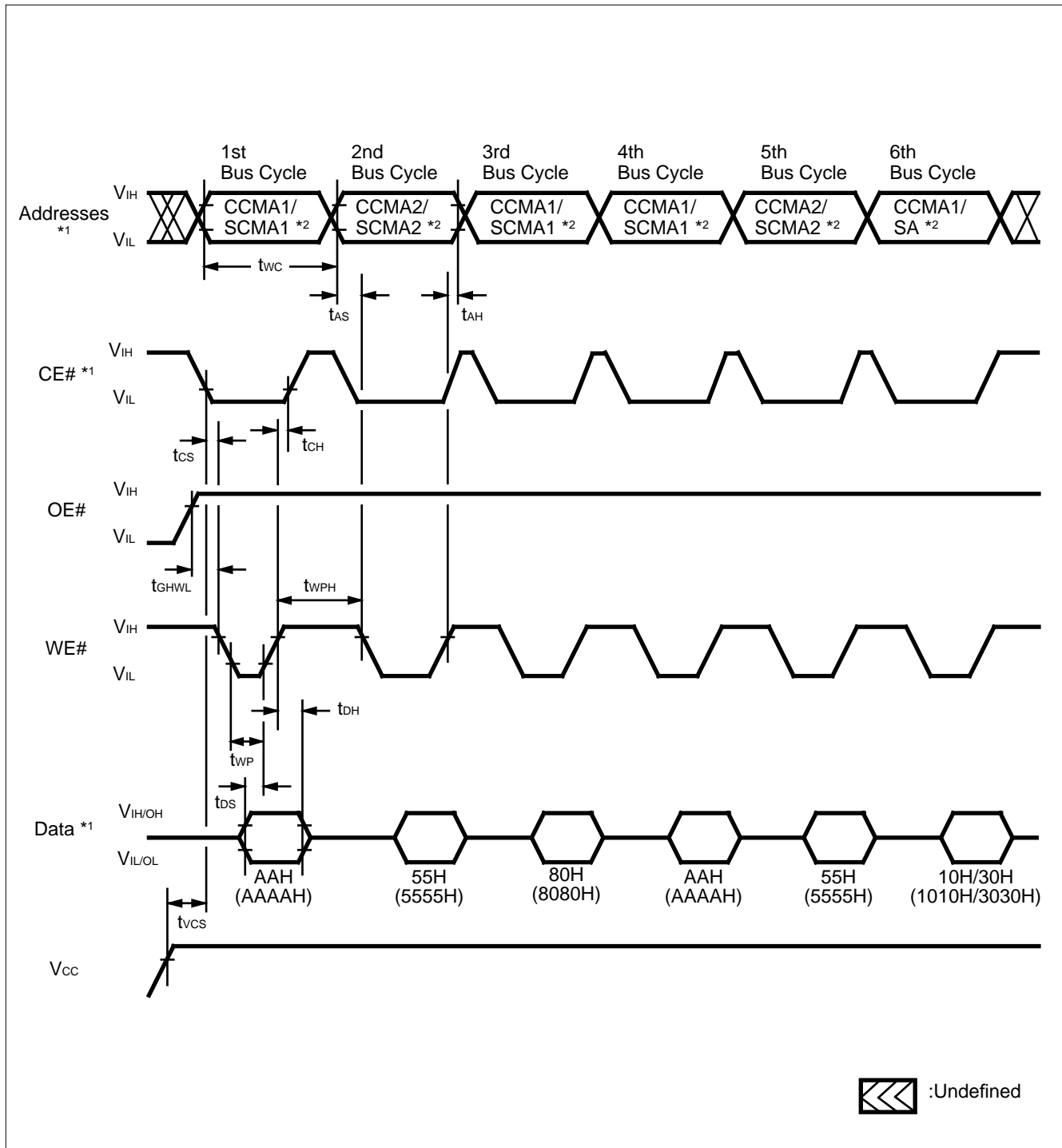
PROGRAM CYCLE TIMING DIAGRAM (CE# = CONTROLLED, RESET# = V<sub>IH</sub>)

**Notes:** \*1. See "FUNCTION TRUTH TABLE".

\*2. PCMA1/PCMA2 = Command Address for Program, PA = Program Address, PD = Program Data. See "COMMAND DEFINITION TABLE".

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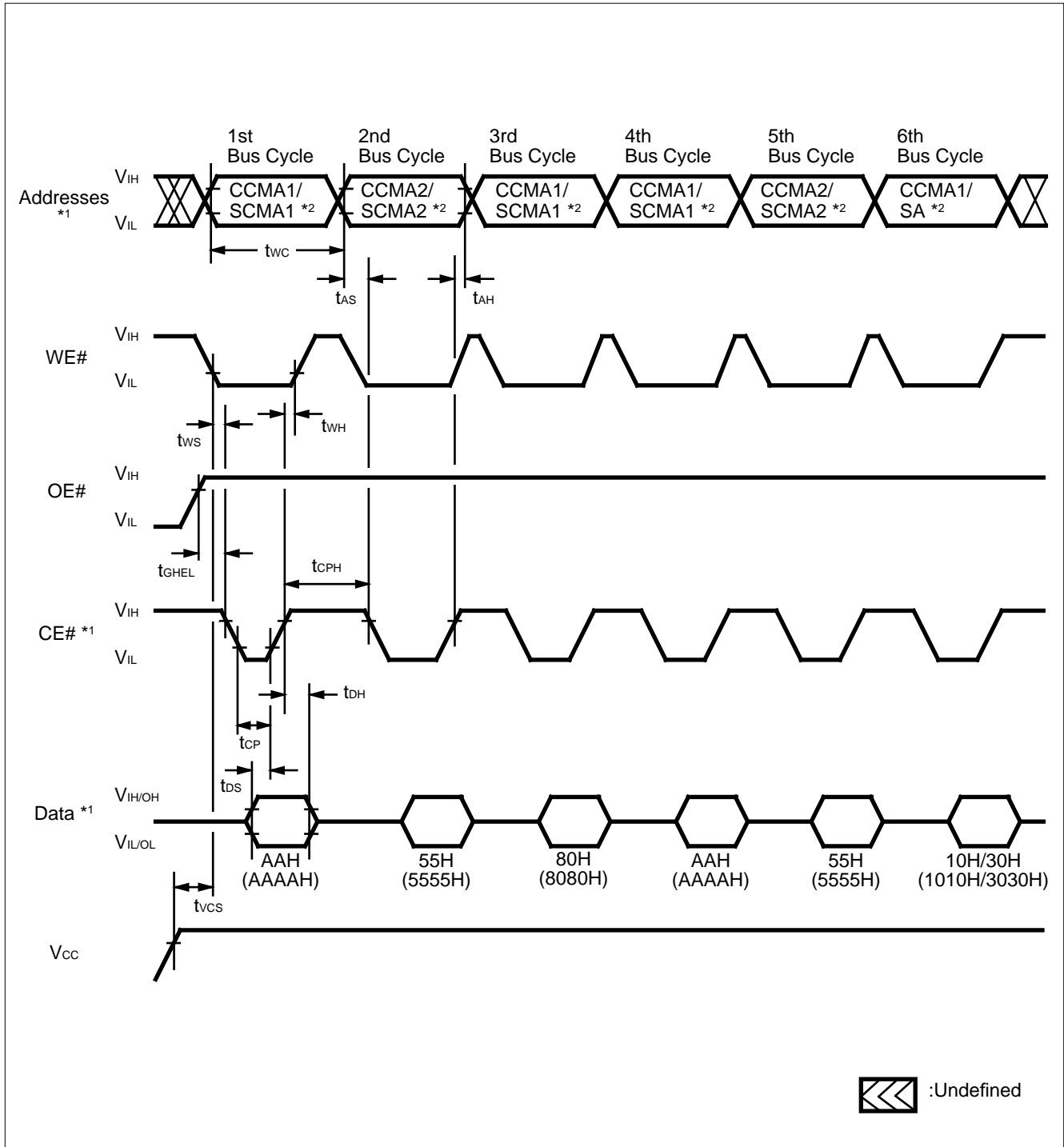
## ERASE CYCLE TIMING DIAGRAM (WE# = CONTROLLED, RESET# = V<sub>IH</sub>)



**Notes:** \*1. See "FUNCTION TRUTH TABLE".

\*2. CCMA1/CCMA2 = Command Address for Chip Erase, SCMA1/SCMA2 = Command Address for Sector Erase, SA = Sector Address. See "COMMAND DEFINITION TABLE".

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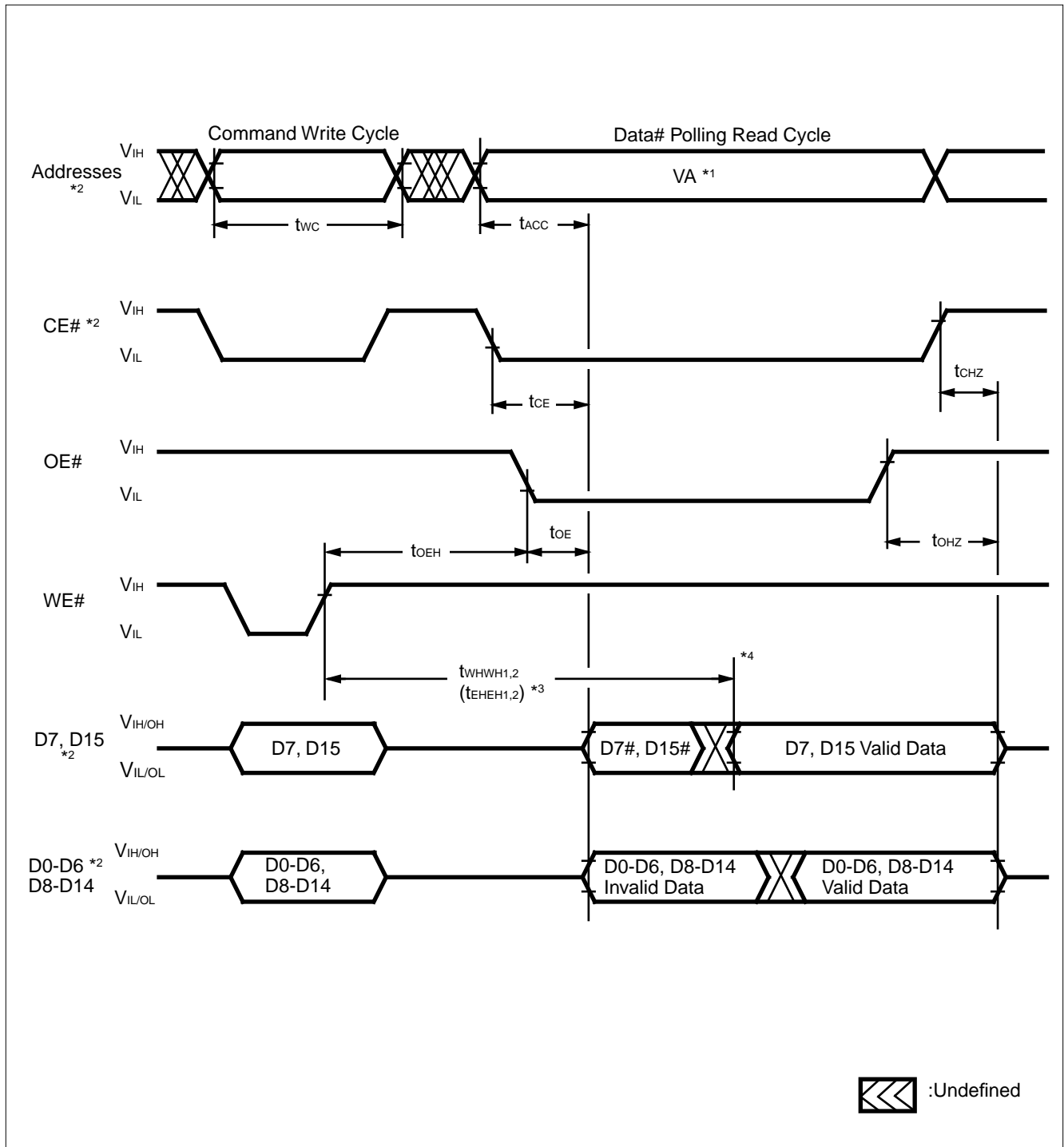
ERASE CYCLE TIMING DIAGRAM (CE# = CONTROLLED, RESET# = V<sub>IH</sub>)

**Notes:** \*1. See "FUNCTION TRUTH TABLE".

\*2. CCMA1/CCMA2 = Command Address for Chip Erase, SCMA1/SCMA2 = Command Address for Sector Erase, SA = Sector Address. See "COMMAND DEFINITION TABLE".

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## DATA# POLLING CYCLE TIMING DIAGRAM (RESET# = V<sub>IH</sub>)



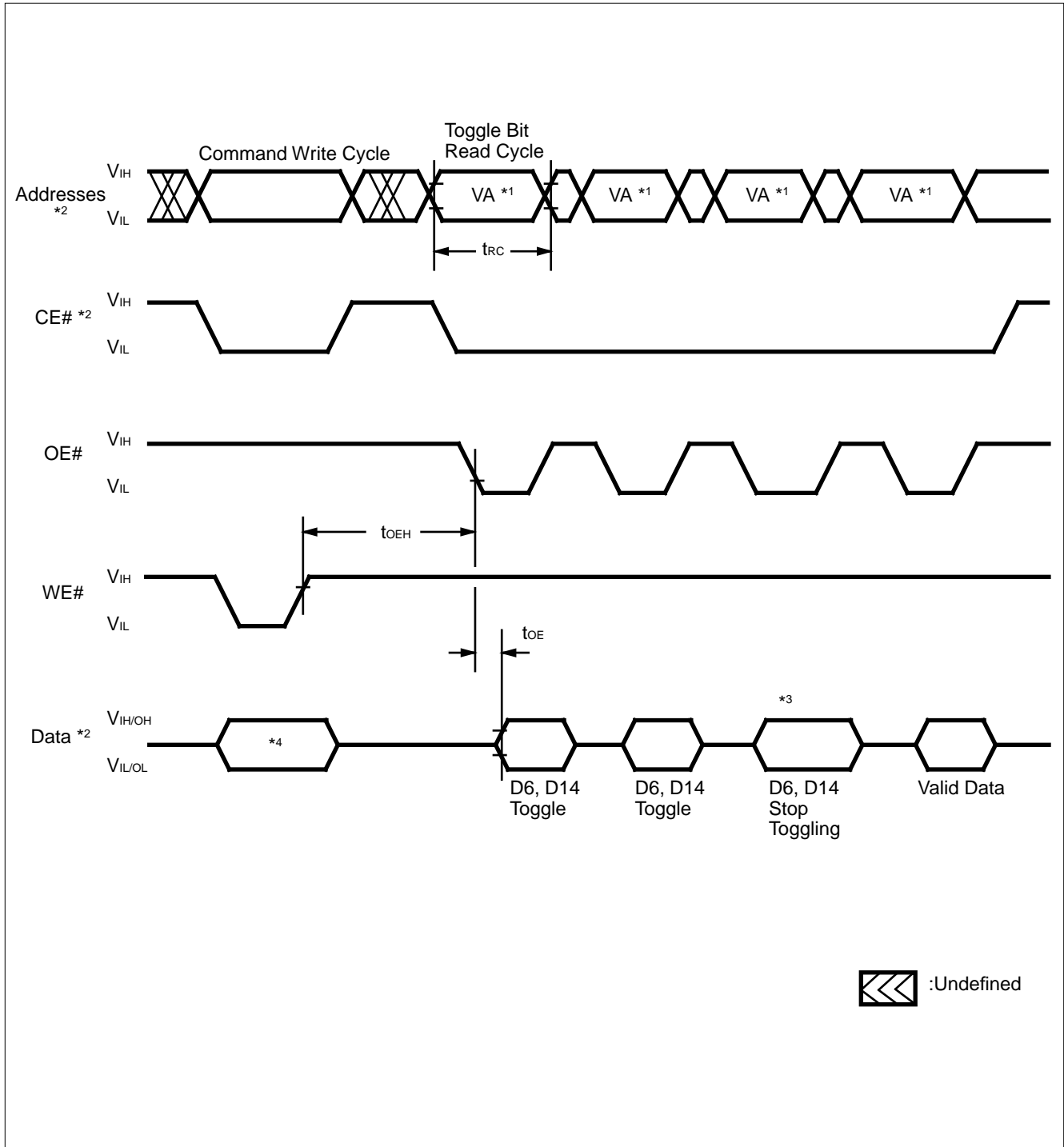
**Notes:** \*1. VA = PA for Programming Cycle, VA = SA for Sector Erase, VA = CA for Chip Erase.

\*2. See "FUNCTION TRUTH TABLE".

\*3.  $t_{EHEH1,2}$  for CE# Control.

\*4. Program/Erase operation is finished.

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TOGGLE BIT TIMING DIAGRAM (RESET# = V<sub>IH</sub>)

**Notes:** \*1. VA = PA for Programming Cycle, VA = SA for Sector Erase, VA = CA for Chip Erase.

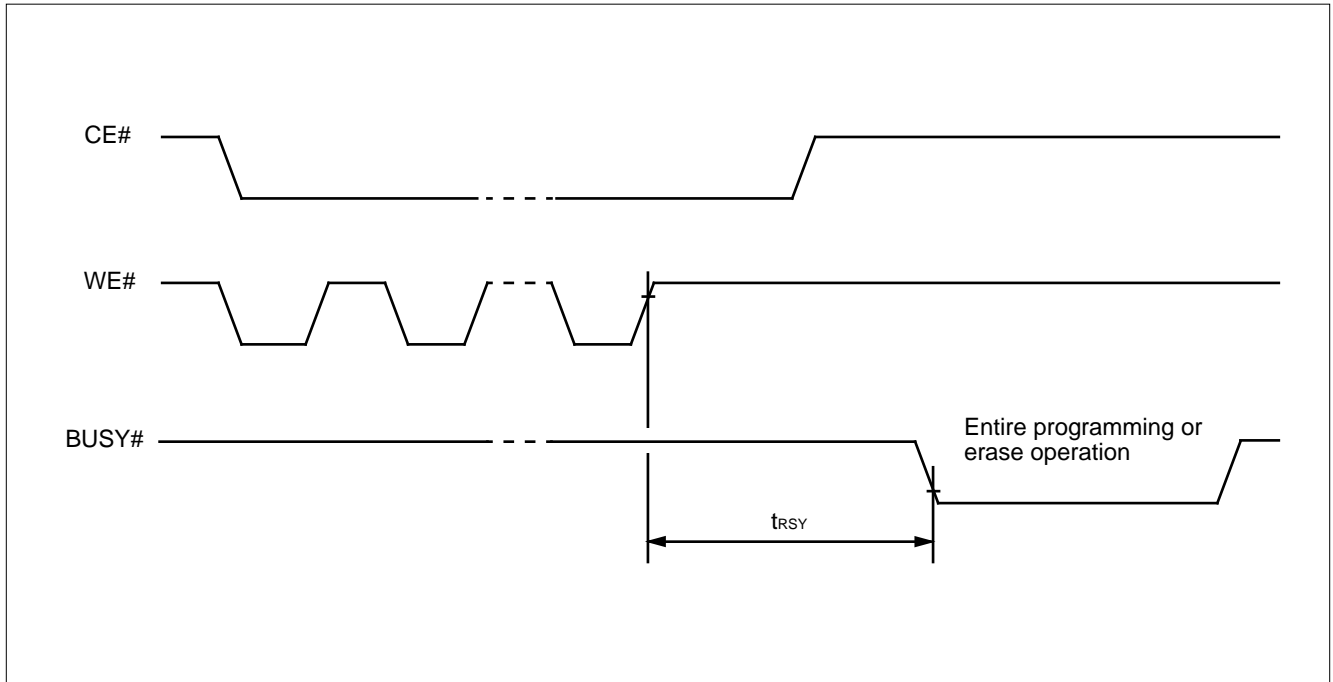
\*2. See "FUNCTION TRUTH TABLE".

\*3. Program/Erase operation is finished.

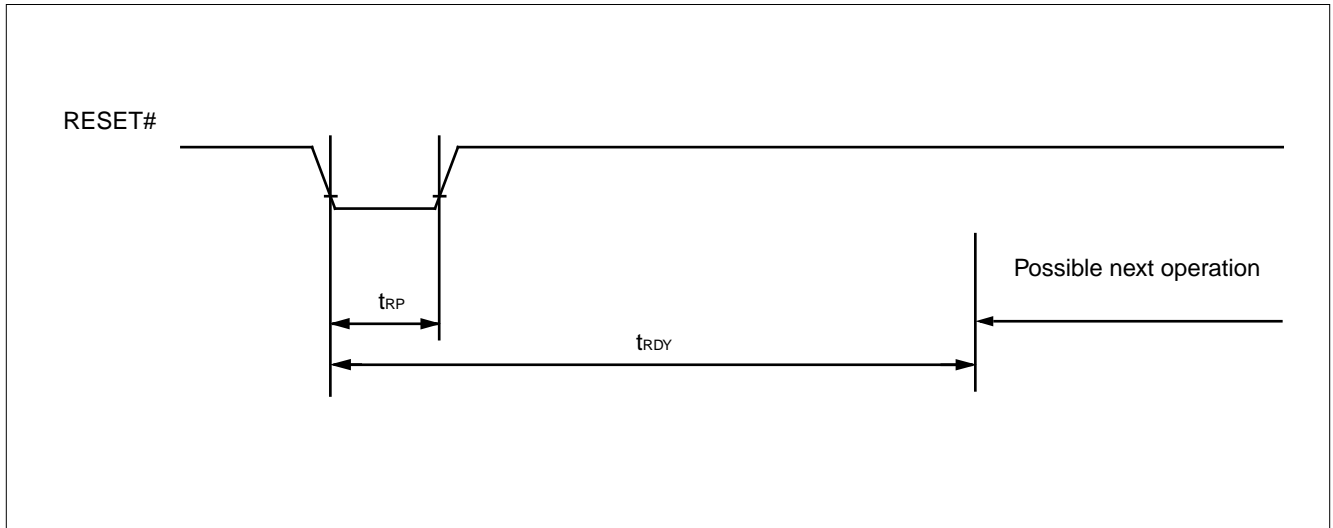
\*4. PD, 10H (1010H) or 30H (3030H)

# MB98D81123/81223-15

## BUSY# Timing Diagram During Program/Erase Operations



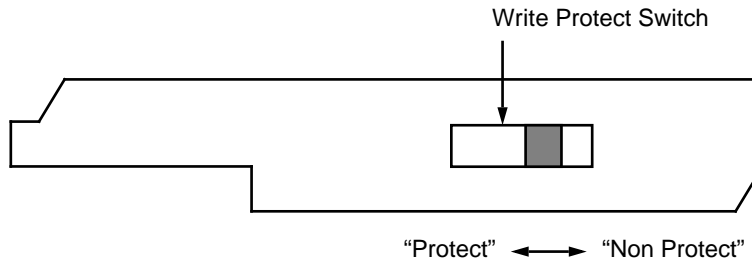
## RESET# Timing Diagram



# MB98D81123/81223-15

## UNIQUE FEATURES

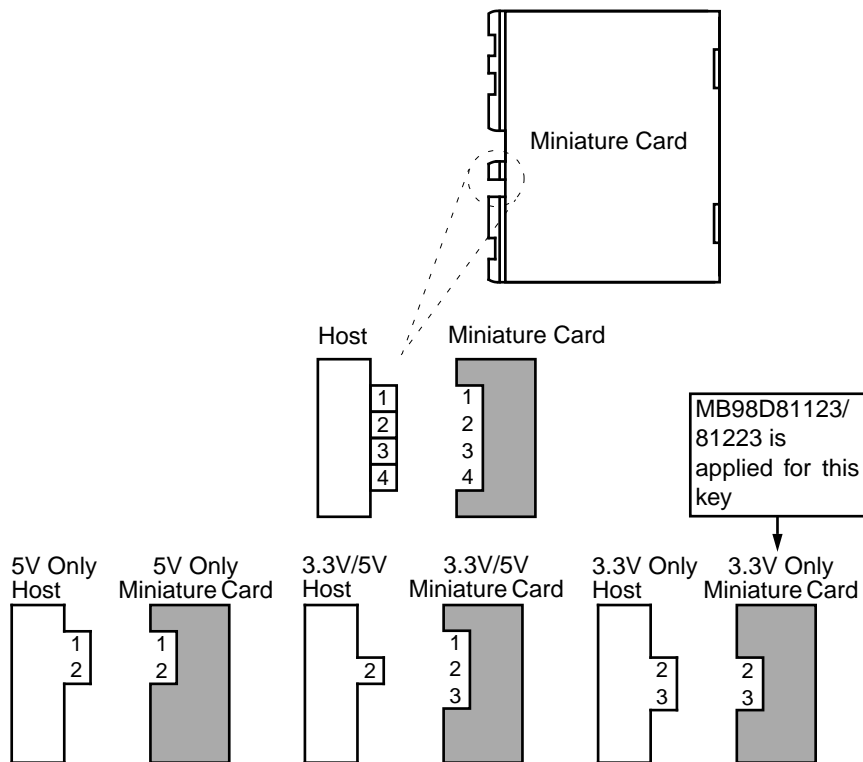
### Write Protect Switch



### Voltage Selection

The Miniature Card voltage is identified by both a mechanical key and voltage sense signals (VS1#, VS2#). The combination of the two allow the host to determine the proper voltage required to operate the Miniature Card, as well as a physical means to keep cards out of host systems that may damage the cards because of improper operational voltage.

Six different voltage key combinations are defined in "Miniature Card Specification": 5 volt only, 3.3 volt only, x.x volt only, 3V/5V, x.xV/3V, and x.xV/3V/5V. These keys consist of notches in the Miniature Card and corresponding tabs in the socket. The socket tabs are located in the front of the Miniature Card socket and are used to keep out cards that do not contain the corresponding notch. See Voltage Keying Mechanism below. (Now only defined about 5.0V and 3.3V)



# MB98D81123/81223-15

## ■ ATTRIBUTE INFORMATION STRUCTURE (AIS)

| Address | Data | Attribute                                      |
|---------|------|--|
| 0000    | 01   | [Common Memory device information tuple]       |
| 0001    | 03   | Link to next tuple                             |
| 0002    | 53   | Flash memory with 150 ns access time           |
| 0003    | 1D   | 2 MB device size for common memory [MB98D1123] |
|         | 0E   | 4 MB device size for common memory [MB98D1223] |
| 0004    | FF   | End of list                                    |
| 05 - 0D | 00   | [Nulltuple-ignore]                             |
| 000E    | 80   | [Vendor unique tuple]                          |
| 000F    | F1   | Link to next tuple                             |
| 0010    | 99   | "Miniature Card Identifier"                    |
| 0011    | 10   | "Level of Compliance"                          |
| 0012    | B5   | "AIS Checksum" (B00-A4B=B5) [MB98D81123]       |
|         | B3   | "AIS Checksum" (B00-A4D=B3) [MB98D81223]       |
| 0013    | 46   | "Manufacture Name" (F)                         |
| 0014    | 55   | (U)  |
| 0015    | 4A   | (J)  |
| 0016    | 49   | (I)  |
| 0017    | 54   | (T)  |
| 0018    | 53   | (S)  |
| 0019    | 55   | (U)  |
| 001A    | 00   |  |
| 001B    | 4C   | (L)  |
| 001C    | 49   | (I)  |
| 001D    | 4D   | (M)  |
| 001E    | 49   | (I)  |
| 001F    | 54   | (T)  |
| 0020    | 45   | (E)  |
| 0021    | 44   | (D)  |
| 0022    | 00   |  |
| 0023    | 00   |  |
| 0024    | 00   |  |
| 0025    | 00   |  |



## ■ ATTRIBUTE INFORMATION STRUCTURE (AIS) (continued)

| Address | Data | Attribute                           |
|---------|------|-------------------------------------|
| 0026    | 00   |                                     |
| 0027    | 4D   | "Card Name" (M)                     |
| 0028    | 42   | (B)                                 |
| 0029    | 39   | (9)                                 |
| 002A    | 38   | (8)                                 |
| 002B    | 44   | (D)                                 |
| 002C    | 38   | (8)                                 |
| 002D    | 30   | (0)                                 |
| 002E    | 30   | (0)                                 |
| 002F    | 32   | (2)                                 |
| 0030    | 33   | (3)                                 |
| 0031    | 00   |                                     |
| 0032    | 73   | (s)                                 |
| 0033    | 65   | (e)                                 |
| 0034    | 72   | (r)                                 |
| 0035    | 69   | (i)                                 |
| 0036    | 65   | (e)                                 |
| 0037    | 73   | (s)                                 |
| 0038    | 00   |                                     |
| 0039    | 00   |                                     |
| 003A    | 00   |                                     |
| 003B    | 01   | "Technology Count" (1)              |
| 003C    | 00   | "Reserved"                          |
| 003D    | 00   | "Reserved"                          |
| 003E    | 00   | "Reserved"                          |
| 003F    | 00   | "Reserved"                          |
| 0040    | 00   | "Memory Type" (Flash)               |
| 0041    | 04   | "JEDEC Manufacture ID" (FUJITSU)    |
| 0042    | 38   | "JEDEC Component ID" (MBM29LV080)   |
| 0043    | 01   | "Memory Size" (2MB) [MB98D81123]    |
|         | 03   | "Memory Size" (4MB) [MB98D81223]    |
| 0044    | 00   | "x.x V Access time" (Not supported) |

# MB98D81123/81223-15

## ■ ATTRIBUTE INFORMATION STRUCTURE (AIS) (continued)

| Address   | Data | Attribute                                   |
|-----------|------|---|
| 0045      | 0F   | "3.3 V Access time" (150 ns)                |
| 0046      | 00   | "5.0 V Access time" (Not supported)         |
| 0047      | 00   | "x.x V Read/Write" (Not supported)          |
| 0048      | 56   | "3.3 V Read/Write" (50 mA/60 mA)            |
| 0049      | 00   | "5.0 V Read/Write" (Not supported)          |
| 004A      | 01   | "Standby Current" (100 $\mu$ A)             |
| 004B      | 00   | "Reserved"                                  |
| 004C      | 00   | "Reserved"                                  |
| ↓<br>004D | 00   | "Reserved"                                  |
| 004E      | 00   | "Reserved"                                  |
| 004F      | 00   | "Reserved"                                  |
| 00FF      | 00   | "Reserved"                                  |
| 0100      | FF   | End of list                                 |
| 0101      | 15   | [Level 1 version/product-information tuple] |
| 0102      | 1C   | Link to next tuple                          |
| 0103      | 05   | PC Card Standard, February 1995             |
| 0104      | 00   |   |
| 0105      | 46   | (F)   |
| 0106      | 55   | (U)   |
| 0107      | 4A   | (J)   |
| 0108      | 49   | (I)   |
| 0109      | 54   | (T)   |
| 010A      | 53   | (S)   |
| 010B      | 55   | (U)   |
| 010C      | 00   |   |
| 010D      | 4D   | (M)   |
| 010E      | 42   | (B)   |
| 010F      | 39   | (9)   |
| 0110      | 38   | (8)   |
| 0111      | 44   | (D)   |
| 0112      | 38   | (8)   |
| 0113      | 30   | (0)   |

## MB98D81123/81223-15

## ■ ATTRIBUTE INFORMATION STRUCTURE (AIS) (continued)

| Address | Data | Attribute  |
|---------|------|--|
| 0114    | 30   | (0)  |
| 0115    | 32   | (2)  |
| 0116    | 33   | (3)  |
| 0117    | 73   | (s)  |
| 0118    | 65   | (e)  |
| 0119    | 72   | (r)  |
| 011A    | 69   | (i)  |
| 011B    | 65   | (e)  |
| 011C    | 73   | (s)  |
| 011D    | 00   |  |
| 011E    | FF   | End of list  |
| 011F    | 18   | [JEDEC programming information for Common Memory tuple]          |
| 0120    | 03   | Link to next tuple   |
| 0121    | 04   | JEDEC Manufacture ID (FUJITSU)                                   |
| 0122    | 38   | JEDEC Device ID (MB29LV080)                                      |
| 0123    | FF   | End of list  |
| 0124    | 1E   | [Device geometry information for Common Memory device tuple]     |
| 0125    | 07   | Link to next tuple   |
| 0126    | 02   | System bus width is 2 Bytes                                      |
| 0127    | 11   | Erase block size is 64 KBytes                                    |
| 0128    | 01   | Read block size is 1 Bytes                                       |
| 0129    | 01   | Write block size is 1 Bytes                                      |
| 012A    | 01   | No special partitioning requirements                             |
| 012B    | 01   | Non interleaved  |
| 012C    | FF   | End of list  |
| 012D    | 12   | [Longlink to Common Memory]                                      |
| 012E    | 05   | Link to next tuple   |
| 012F    | 00   | Target address; stored as an unsigned long, low-order byte first |
| 0130    | 00   |  |
| 0131    | 02   |  |
| 0132    | 00   |  |
| 0133    | FF   | End of list  |

# MB98D81123/81223-15

## ■ ATTRIBUTE INFORMATION STRUCTURE (AIS) (continued)

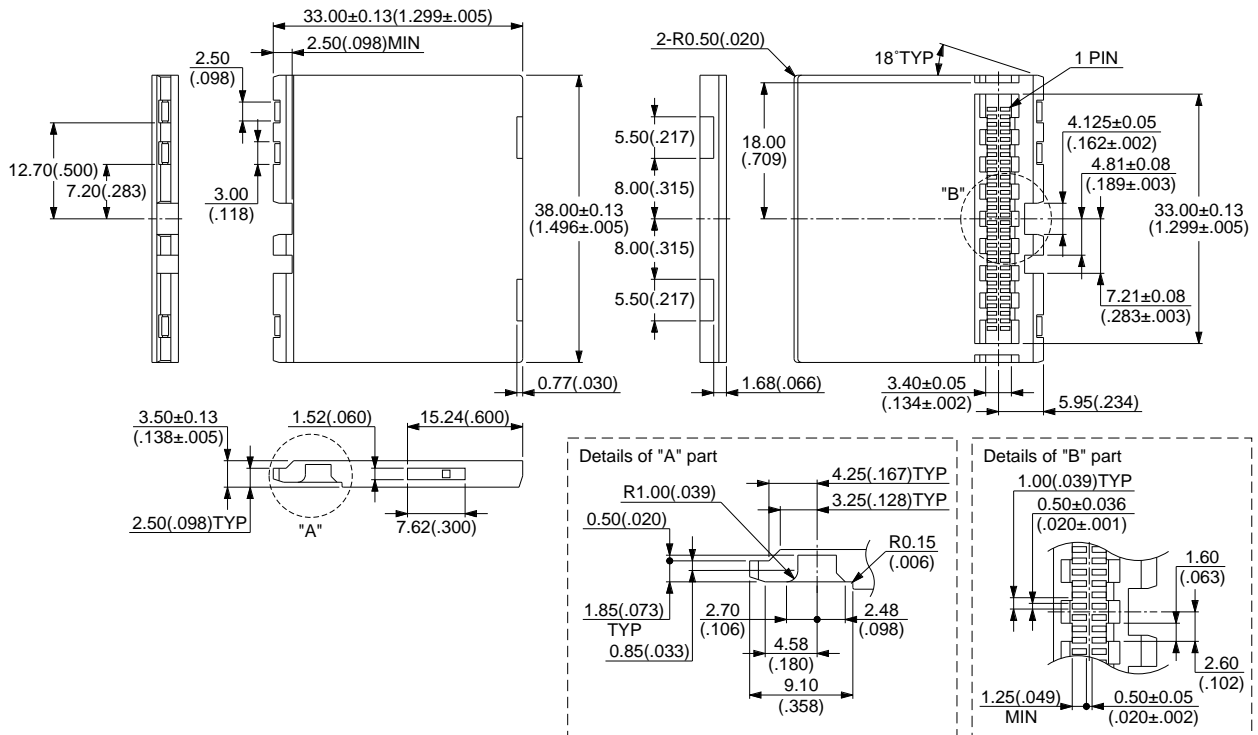
| Address | Data | Attribute   |
|---------|------|---|
| 0134    | 1C   | [Other operating conditions device information for Common Memory] |
| 0135    | 04   | Link to next tuple  |
| 0136    | 02   | Other Conditions Information: 3.3 V Operation                     |
| 0137    | 53   | Flash Memory with 150 ns access time                              |
| 0138    | 1D   | 2 MB device size for common memory [MB98D81123]                   |
|         | 0E   | 4 MB device size for common memory [MB98D81223]                   |
| 0139    | FF   | End of list   |
| 013A    | FF   | [The end-of-chain tuple]  |

**Notice:** AIS is programmed from the address "0000H" of Lower Byte. This AIS may be deleted on the driver software which does not consider AIS.

## MB98D81123/81223-15

## ■ PACKAGE DIMENSIONS

### 60-PIN MINIATURE CARD (CASE No.: CRD-60P-M02)



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Dimension in mm (inches)

# MB98D81123/81223-15

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