

# MEMORY

## LOW POWER SRAM CARD

PCMCIA Rel.2/JEIDA Ver.4 conformable

**MB98A9083x/9093x/9103x/9113x-20**

### LOW POWER STATIC RANDOM ACCESS MEMORY CARD 256 K/512 K/1 M/2 M-BYTE

#### ■ DESCRIPTION

The Fujitsu MB98A9083x, 9093x, 9103x and 9113x are Static Random Access Memory (SRAM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by two metal panels, each one at the top and the bottom of the card, that help to reduce chip damage from electrostatic discharge.

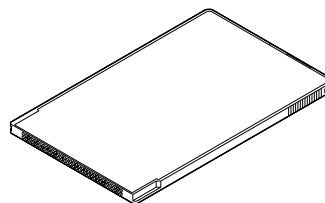
When the SRAM card is not powered by its system, an on-board, replaceable lithium battery (coin-type) is used to retain data. When the lithium battery must be replaced, rechargeable battery that are built in the SRAM card, maintain data. (See the BLOCK DIAGRAM for location of batteries.)

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specifications, SRAM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is an SRAM card option. (See page 3 for a description of the three available options.)

- Credit card size: 85.6 mm (length) × 54.0 mm (width) × 3.3 mm (thick).
- PCMCIA/JEIDA conformed two-piece 68-pin connector (with a two-row built-in 68-pin receptacle)
- Low operating and standby power consumption
- Built-in, rechargeable batteries for data retention during lithium battery replacement
- Battery voltage detect and write protect function

#### ■ PACKAGE



CRD-68P-M04

# MB98A9083x/9093x/9103x/9113x-20

## ■ ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the  $\overline{\text{REG}}$  pin on the card interface. Option descriptions as follows:

### OPTION 1: Attribute memory is not supported. REG Pin: Not Contacted

(JEIDA Ver.3 conformable)

| Part Number | Main Memory      |             | Attribute Memory |             | Memory Organization*           |
|-------------|------------------|-------------|------------------|-------------|--------------------------------|
|             | Memory Device    | Access Time | Memory Device    | Access Time |                                |
| MB98A90831  | 1M SRAM × 2 pcs  | 200 ns      | —                | —           | 256 K × 8 bits/128 K × 16 bits |
| MB98A90931  | 1M SRAM × 4 pcs  | 200 ns      | —                | —           | 512 K × 8 bits/256 K × 16 bits |
| MB98A91031  | 1M SRAM × 8 pcs  | 200 ns      | —                | —           | 1 M × 8 bits/512 K × 16 bits   |
| MB98A91131  | 1M SRAM × 16 pcs | 200 ns      | —                | —           | 2 M × 8 bits/1 M × 16 bits     |

### OPTION 2: Attribute memory in a separate location is not supported.

When the  $\overline{\text{REG}}$  line is asserted, “FF” is output to the data bus to indicate that attribute data may be stored in main memory.

(PCMCIA Rel.2/JEIDA Ver.4 conformable)

| Part Number | Main Memory      |             | Attribute Memory |             | Memory Organization*           |
|-------------|------------------|-------------|------------------|-------------|--------------------------------|
|             | Memory Device    | Access Time | Memory Device    | Access Time |                                |
| MB98A90832  | 1M SRAM × 2 pcs  | 200 ns      | —                | —           | 256 K × 8 bits/128 K × 16 bits |
| MB98A90932  | 1M SRAM × 4 pcs  | 200 ns      | —                | —           | 512 K × 8 bits/256 K × 16 bits |
| MB98A91032  | 1M SRAM × 8 pcs  | 200 ns      | —                | —           | 1 M × 8 bits/512 K × 16 bits   |
| MB98A91132  | 1M SRAM × 16 pcs | 200 ns      | —                | —           | 2 M × 8 bits/1 M × 16 bits     |

### OPTION 3: Attribute memory is supported. The data is stored in an 16K-bit EEPROM.

When the  $\overline{\text{REG}}$  line is asserted, data stored in EEPROM is output to the data bus.

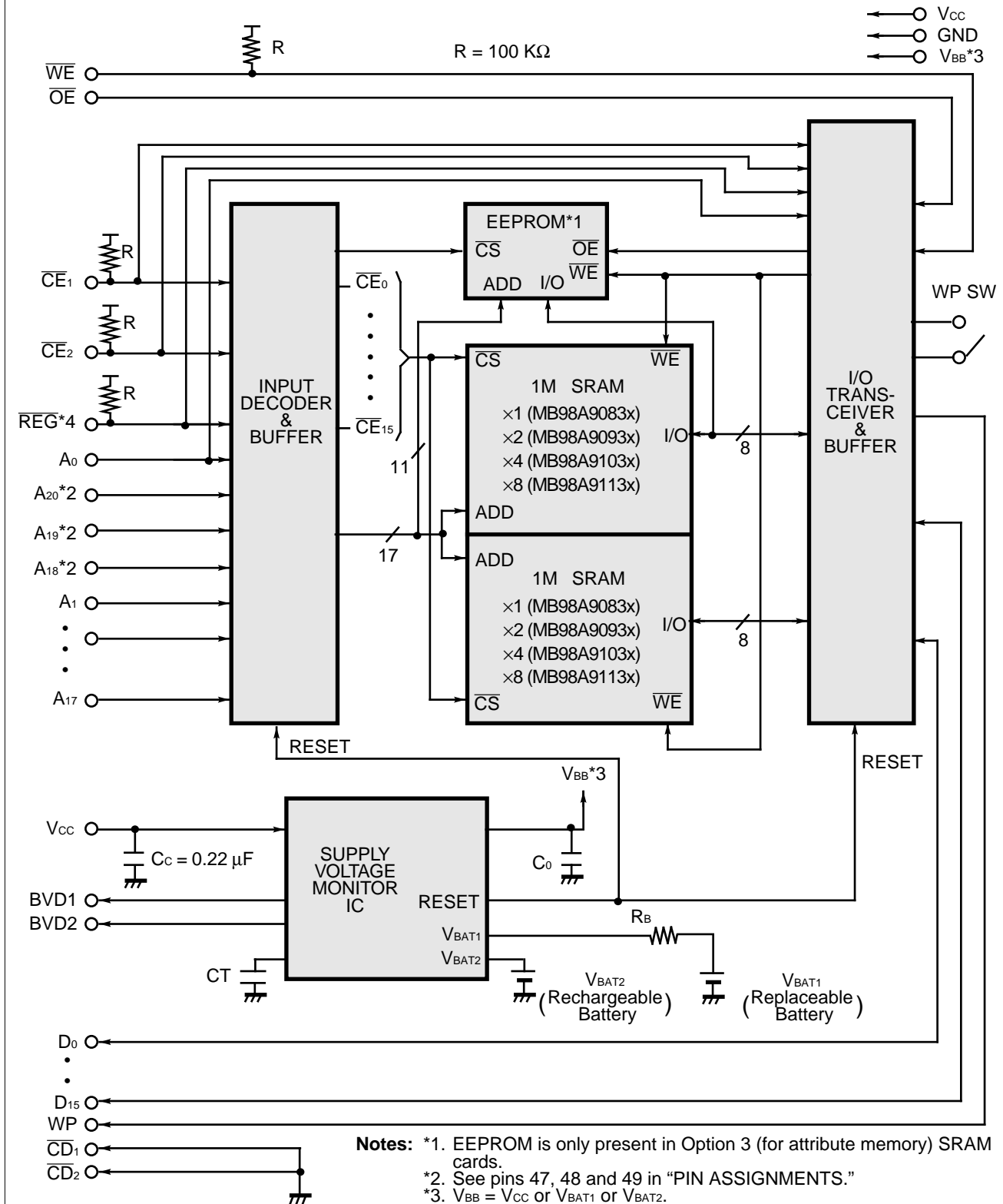
(PCMCIA Rel.2/JEIDA Ver.4 conformable)

| Part Number | Main Memory      |             | Attribute Memory |             | Memory Organization*           |
|-------------|------------------|-------------|------------------|-------------|--------------------------------|
|             | Memory Device    | Access Time | Memory Device    | Access Time |                                |
| MB98A90833  | 1M SRAM × 2 pcs  | 200 ns      | EEPROM × 1 pcs   | 300 ns      | 256 K × 8 bits/128 K × 16 bits |
| MB98A90933  | 1M SRAM × 4 pcs  | 200 ns      | EEPROM × 1 pcs   | 300 ns      | 512 K × 8 bits/256 K × 16 bits |
| MB98A91033  | 1M SRAM × 8 pcs  | 200 ns      | EEPROM × 1 pcs   | 300 ns      | 1 M × 8 bits/512 K × 16 bits   |
| MB98A91133  | 1M SRAM × 16 pcs | 200 ns      | EEPROM × 1 pcs   | 300 ns      | 2 M × 8 bits/1 M × 16 bits     |

**Note:** \* To be configured by user.

# MB98A9083x/9093x/9103x/9113x-20

Fig. 1 - MB98A9083x/9093x/9103x/9113x BLOCK DIAGRAM



- Notes:**
- \*1. EEPROM is only present in Option 3 (for attribute memory) SRAM cards.
  - \*2. See pins 47, 48 and 49 in "PIN ASSIGNMENTS."
  - \*3.  $V_{BB} = V_{CC}$  or  $V_{BAT1}$  or  $V_{BAT2}$ .
  - \*4. N.C. terminal in MB98A9XX31 series.

# MB98A9083x/9093x/9103x/9113x-20

## ■ PIN ASSIGNMENTS

| MB98A9083x        | MB98A9093x        | MB98A9103x        | MB98A9113x        | Pin No. |    | MB98A9083x             | MB98A9093x             | MB98A9103x             | MB98A9113x             |
|-------------------|-------------------|-------------------|-------------------|---------|----|------------------------|------------------------|------------------------|------------------------|
| GND               | GND               | GND               | GND               | 1       | 35 | GND                    | GND                    | GND                    | GND                    |
| D <sub>3</sub>    | D <sub>3</sub>    | D <sub>3</sub>    | D <sub>3</sub>    | 2       | 36 | $\overline{CD}_1$      | $\overline{CD}_1$      | $\overline{CD}_1$      | $\overline{CD}_1$      |
| D <sub>4</sub>    | D <sub>4</sub>    | D <sub>4</sub>    | D <sub>4</sub>    | 3       | 37 | D <sub>11</sub>        | D <sub>11</sub>        | D <sub>11</sub>        | D <sub>11</sub>        |
| D <sub>5</sub>    | D <sub>5</sub>    | D <sub>5</sub>    | D <sub>5</sub>    | 4       | 38 | D <sub>12</sub>        | D <sub>12</sub>        | D <sub>12</sub>        | D <sub>12</sub>        |
| D <sub>6</sub>    | D <sub>6</sub>    | D <sub>6</sub>    | D <sub>6</sub>    | 5       | 39 | D <sub>13</sub>        | D <sub>13</sub>        | D <sub>13</sub>        | D <sub>13</sub>        |
| D <sub>7</sub>    | D <sub>7</sub>    | D <sub>7</sub>    | D <sub>7</sub>    | 6       | 40 | D <sub>14</sub>        | D <sub>14</sub>        | D <sub>14</sub>        | D <sub>14</sub>        |
| $\overline{CE}_1$ | $\overline{CE}_1$ | $\overline{CE}_1$ | $\overline{CE}_1$ | 7       | 41 | D <sub>15</sub>        | D <sub>15</sub>        | D <sub>15</sub>        | D <sub>15</sub>        |
| A <sub>10</sub>   | A <sub>10</sub>   | A <sub>10</sub>   | A <sub>10</sub>   | 8       | 42 | $\overline{CE}_2$      | $\overline{CE}_2$      | $\overline{CE}_2$      | $\overline{CE}_2$      |
| $\overline{OE}$   | $\overline{OE}$   | $\overline{OE}$   | $\overline{OE}$   | 9       | 43 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>11</sub>   | A <sub>11</sub>   | A <sub>11</sub>   | A <sub>11</sub>   | 10      | 44 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>9</sub>    | A <sub>9</sub>    | A <sub>9</sub>    | A <sub>9</sub>    | 11      | 45 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>8</sub>    | A <sub>8</sub>    | A <sub>8</sub>    | A <sub>8</sub>    | 12      | 46 | A <sub>17</sub>        | A <sub>17</sub>        | A <sub>17</sub>        | A <sub>17</sub>        |
| A <sub>13</sub>   | A <sub>13</sub>   | A <sub>13</sub>   | A <sub>13</sub>   | 13      | 47 | N.C.                   | A <sub>18</sub>        | A <sub>18</sub>        | A <sub>18</sub>        |
| A <sub>14</sub>   | A <sub>14</sub>   | A <sub>14</sub>   | A <sub>14</sub>   | 14      | 48 | N.C.                   | N.C.                   | A <sub>19</sub>        | A <sub>19</sub>        |
| $\overline{WE}$   | $\overline{WE}$   | $\overline{WE}$   | $\overline{WE}$   | 15      | 49 | N.C.                   | N.C.                   | N.C.                   | A <sub>20</sub>        |
| N.C.              | N.C.              | N.C.              | N.C.              | 16      | 50 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| V <sub>CC</sub>   | V <sub>CC</sub>   | V <sub>CC</sub>   | V <sub>CC</sub>   | 17      | 51 | V <sub>CC</sub>        | V <sub>CC</sub>        | V <sub>CC</sub>        | V <sub>CC</sub>        |
| N.C.              | N.C.              | N.C.              | N.C.              | 18      | 52 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>16</sub>   | A <sub>16</sub>   | A <sub>16</sub>   | A <sub>16</sub>   | 19      | 53 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>15</sub>   | A <sub>15</sub>   | A <sub>15</sub>   | A <sub>15</sub>   | 20      | 54 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>12</sub>   | A <sub>12</sub>   | A <sub>12</sub>   | A <sub>12</sub>   | 21      | 55 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>7</sub>    | A <sub>7</sub>    | A <sub>7</sub>    | A <sub>7</sub>    | 22      | 56 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>6</sub>    | A <sub>6</sub>    | A <sub>6</sub>    | A <sub>6</sub>    | 23      | 57 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>5</sub>    | A <sub>5</sub>    | A <sub>5</sub>    | A <sub>5</sub>    | 24      | 58 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>4</sub>    | A <sub>4</sub>    | A <sub>4</sub>    | A <sub>4</sub>    | 25      | 59 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>3</sub>    | A <sub>3</sub>    | A <sub>3</sub>    | A <sub>3</sub>    | 26      | 60 | N.C.                   | N.C.                   | N.C.                   | N.C.                   |
| A <sub>2</sub>    | A <sub>2</sub>    | A <sub>2</sub>    | A <sub>2</sub>    | 27      | 61 | $\overline{REG}/N.C.*$ | $\overline{REG}/N.C.*$ | $\overline{REG}/N.C.*$ | $\overline{REG}/N.C.*$ |
| A <sub>1</sub>    | A <sub>1</sub>    | A <sub>1</sub>    | A <sub>1</sub>    | 28      | 62 | BVD2                   | BVD2                   | BVD2                   | BVD2                   |
| A <sub>0</sub>    | A <sub>0</sub>    | A <sub>0</sub>    | A <sub>0</sub>    | 29      | 63 | BVD1                   | BVD1                   | BVD1                   | BVD1                   |
| D <sub>0</sub>    | D <sub>0</sub>    | D <sub>0</sub>    | D <sub>0</sub>    | 30      | 64 | D <sub>8</sub>         | D <sub>8</sub>         | D <sub>8</sub>         | D <sub>8</sub>         |
| D <sub>1</sub>    | D <sub>1</sub>    | D <sub>1</sub>    | D <sub>1</sub>    | 31      | 65 | D <sub>9</sub>         | D <sub>9</sub>         | D <sub>9</sub>         | D <sub>9</sub>         |
| D <sub>2</sub>    | D <sub>2</sub>    | D <sub>2</sub>    | D <sub>2</sub>    | 32      | 66 | D <sub>10</sub>        | D <sub>10</sub>        | D <sub>10</sub>        | D <sub>10</sub>        |
| WP                | WP                | WP                | WP                | 33      | 67 | $\overline{CD}_2$      | $\overline{CD}_2$      | $\overline{CD}_2$      | $\overline{CD}_2$      |
| GND               | GND               | GND               | GND               | 34      | 68 | GND                    | GND                    | GND                    | GND                    |

\* : N.C. terminal in MB98A9XX31 series.

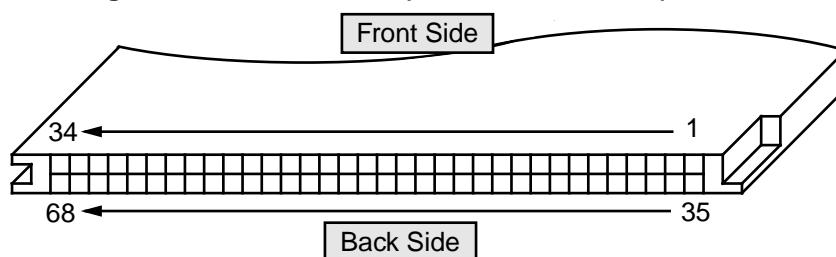
# MB98A9083x/9093x/9103x/9113x-20

## ■ PIN DESCRIPTIONS

| Symbol                             | Pin Name                   | Input/Output | Function   |
|------------------------------------|----------------------------|--------------|--|
| A <sub>0</sub> to A <sub>20</sub>  | Address Input              | Input        | Address Inputs, A <sub>0</sub> to A <sub>20</sub> .  |
| D <sub>0</sub> to D <sub>15</sub>  | Data Input/Output          | Input/Output | Data Inputs/Outputs.<br>The data bus size (8-bit or 16-bit) selected with $\overline{CE}_1$ and $\overline{CE}_2$ .  |
| $\overline{CE}_1$                  | Card Enable for Lower Byte | Input        | Active Low<br>– Lower byte (D <sub>0</sub> to D <sub>7</sub> ) is selected for read/write function of SRAM cards.  |
| $\overline{CE}_2$                  | Card Enable for Upper Byte | Input        | Active Low<br>– Upper byte (D <sub>8</sub> to D <sub>15</sub> ) is selected for read/write function of SRAM cards.   |
| $\overline{REG}$                   | Attribute Memory Select    | Input        | Active Low<br>– Attribute memory is selected for read/write function of identification data of SRAM cards. (N.C. or “FF” data or attribute data.)  |
| $\overline{OE}$                    | Output Enable              | Input        | Active Low<br>– Output enable for SRAM cards.  |
| $\overline{WE}$                    | Write Enable               | Input        | Active Low<br>– Write enable for SRAM cards.   |
| $\overline{CD}_1, \overline{CD}_2$ | Card Detect                | Output       | These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.   |
| WP                                 | Write Protect              | Output       | Write controller for SRAM cards<br>This pin outputs the Protect / Non Protect status of “WP Switch”.   |
| BVD1                               | Battery Voltage Detect 1   | Output       | These pins indicate the battery condition of the SRAM cards.<br>a) BVD1 = BVD2 = V <sub>OH</sub><br>– Battery voltage is a safe level.<br>b) BVD2 = V <sub>OL</sub> , BVD1 = V <sub>OH</sub><br>– Battery voltage is lower than 2.65 V.<br>Battery should be replaced.<br>c) BVD1 = BVD2 = V <sub>OL</sub><br>– Battery voltage is lower than 2.37 V, or battery is not present. |
| BVD2                               | Battery Voltage Detect 2   | Output       |  |
| V <sub>cc</sub>                    | Power Supply               | —            | Power Supply Voltage (+5.0 V±5%)   |
| GND                                | Ground                     | —            | System Ground  |
| N.C.                               | No Connection              | —            |  |

## ■ PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



# MB98A9083x/9093x/9103x/9113x-20

## FUNCTIONAL TRUTH TABLE

MAIN MEMORY FUNCTION \*1 ( $\overline{\text{REG}} = V_{\text{IH}}$ )

| $\overline{\text{CE}}_2$ | $\overline{\text{CE}}_1$ | $A_0$<br>(Byte) | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | WP | Mode           | Data Input/Output                 |                                  | WP SW |
|--------------------------|--------------------------|-----------------|------------------------|------------------------|----|----------------|-----------------------------------|----------------------------------|-------|
|                          |                          |                 |                        |                        |    |                | D <sub>15</sub> to D <sub>8</sub> | D <sub>7</sub> to D <sub>0</sub> |       |
| H                        | H                        | X               | X                      | X                      | L  | Standby        | High-Z                            |                                  | NP    |
| H                        | L                        | L               | L                      | H                      | L  | Read (×8)      | High-Z                            | D <sub>OUT</sub><br>(Lower Byte) | NP    |
| H                        | L                        | H               | L                      | H                      | L  | Read (×8)      | High-Z                            | D <sub>OUT</sub><br>(Upper Byte) | NP    |
| H                        | L                        | L               | H*2                    | L                      | L  | Write (×8)     | High-Z                            | D <sub>IN</sub><br>(Lower Byte)  | NP    |
| H                        | L                        | H               | H*2                    | L                      | L  | Write (×8)     | High-Z                            | D <sub>IN</sub><br>(Upper Byte)  | NP    |
| L                        | H                        | X               | L                      | H                      | L  | Read (×8)      | D <sub>OUT</sub><br>(Upper Byte)  | High-Z                           | NP    |
| L                        | H                        | X               | H*2                    | L                      | L  | Write (×8)     | D <sub>IN</sub><br>(Upper Byte)   | High-Z                           | NP    |
| L                        | L                        | X               | L                      | H                      | L  | Read (×16)     | D <sub>OUT</sub>                  |                                  | NP    |
| L                        | L                        | X               | H*2                    | L                      | L  | Write (×16)    | D <sub>IN</sub>                   |                                  | NP    |
| X                        | X                        | X               | H                      | H                      | L  | Output Disable | High-Z                            |                                  | NP    |

|   |   |   |     |   |   |                |                                  |                                  |   |
|---|---|---|-----|---|---|----------------|----------------------------------|----------------------------------|---|
| H | H | X | X   | X | H | Standby        | High-Z                           |                                  | P |
| H | L | L | L   | H | H | Read (×8)      | High-Z                           | D <sub>OUT</sub><br>(Lower Byte) | P |
| H | L | H | L   | H | H | Read (×8)      | High-Z                           | D <sub>OUT</sub><br>(Upper Byte) | P |
| H | L | L | H*2 | L | H | Output Disable | High-Z                           |                                  | P |
| H | L | H | H*2 | L | H | Output Disable | High-Z                           |                                  | P |
| L | H | X | L   | H | H | Read (×8)      | D <sub>OUT</sub><br>(Upper Byte) | High-Z                           | P |
| L | H | X | H*2 | L | H | Output Disable | High-Z                           |                                  | P |
| L | L | X | L   | H | H | Read (×16)     | D <sub>OUT</sub>                 |                                  | P |
| L | L | X | H*2 | L | H | Output Disable | High-Z                           |                                  | P |
| X | X | X | H   | H | H | Output Disable | High-Z                           |                                  | P |

**Notes:** \*1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Either V<sub>IL</sub> or V<sub>IH</sub>, WP SW = Write Protect Switch, NP = Non Protect, P = Protect  
\*2. H-level is recommended though it is functionable at L-level.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY FUNCTION \*1 ( $\overline{\text{REG}} = V_{\text{IL}}$ ) \*2

| $\overline{\text{CE}}_2$ | $\overline{\text{CE}}_1$ | $A_0$<br>(Byte) | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | WP | Mode           | Data Input/Output                 |                                     | WP SW |
|--------------------------|--------------------------|-----------------|------------------------|------------------------|----|----------------|-----------------------------------|-------------------------------------|-------|
|                          |                          |                 |                        |                        |    |                | D <sub>15</sub> to D <sub>8</sub> | D <sub>7</sub> to D <sub>0</sub>    |       |
| H                        | H                        | X               | X                      | X                      | L  | Standby        | High-Z                            |                                     | NP    |
| H                        | L                        | L               | L                      | H                      | L  | Read (×8)      | High-Z                            | D <sub>OUT</sub> *3<br>(Lower Byte) | NP    |
| H                        | L                        | H               | L                      | H                      | L  | Read (×8)      | High-Z                            | H-level                             | NP    |
| H                        | L                        | L               | H                      | L                      | L  | Write (×8)     | High-Z                            | D <sub>IN</sub><br>(Lower Byte)     | NP    |
| H                        | L                        | H               | H                      | L                      | L  | Write (×8)     | High-Z                            | X                                   | NP    |
| L                        | H                        | X               | L                      | H                      | L  | Read (×8)      | H-level                           | High-Z                              | NP    |
| L                        | H                        | X               | H                      | L                      | L  | Write (×8)     | High-Z                            | High-Z                              | NP    |
| L                        | L                        | X               | L                      | H                      | L  | Read (×16)     | H-level                           | D <sub>OUT</sub> *3<br>(Lower Byte) | NP    |
| L                        | L                        | X               | H                      | L                      | L  | Write (×16)    | X                                 | D <sub>IN</sub><br>(Lower Byte)     | NP    |
| X                        | X                        | X               | H                      | H                      | L  | Output Disable | High-Z                            |                                     | NP    |

|   |   |   |   |   |   |                |         |                                     |   |
|---|---|---|---|---|---|----------------|---------|-------------------------------------|---|
| H | H | X | X | X | H | Standby        | High-Z  |                                     | P |
| H | L | L | L | H | H | Read (×8)      | High-Z  | D <sub>OUT</sub> *3<br>(Lower Byte) | P |
| H | L | H | L | H | H | Read (×8)      | High-Z  | H-level                             | P |
| H | L | L | H | L | H | Output Disable | High-Z  |                                     | P |
| H | L | H | H | L | H | Output Disable | High-Z  |                                     | P |
| L | H | X | L | H | H | Read (×8)      | H-level | High-Z                              | P |
| L | H | X | H | L | H | Output Disable | High-Z  |                                     | P |
| L | L | X | L | H | H | Read (×16)     | H-level | D <sub>OUT</sub> *3<br>(Lower Byte) | P |
| L | L | X | H | L | H | Output Disable | High-Z  |                                     | P |
| X | X | X | H | H | H | Output Disable | High-Z  |                                     | P |

**Notes:** \*1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Either V<sub>IL</sub> or V<sub>IH</sub>, WP SW = Write Protect Switch, NP = Non Protect, P = Protect

\*2. N.C. for MB98A90831, 90931, 91031 and 91131.

\*3. H-level is output for MB98A90832, 90932, 91032 and 91132.

# MB98A9083x/9093x/9103x/9113x-20

## ■ ADDRESS CONFIGURATIONS \*1 (MAIN MEMORY)

### 8-BIT BUS ORGANIZATION ( $\overline{CE}_1 = V_{IL}$ , $\overline{CE}_2 = V_{IH}$ )

| A <sub>20</sub> to A <sub>0</sub> |      |      |      |      |      | $\overline{CE}_2$ | $\overline{CE}_1$ | D <sub>15</sub> to D <sub>8</sub> | D <sub>7</sub> to D <sub>0</sub> |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 0                                 | 0000 | 0000 | 0000 | 0000 | 0000 | H                 | L                 | -----                             | 0 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 0001 | H                 | L                 | -----                             | 1 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 0010 | H                 | L                 | -----                             | 2 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 0011 | H                 | L                 | -----                             | 3 Add.                           |
| ↓                                 | ↓    | ↓    | ↓    | ↓    | ↓    | ↓                 | ↓                 | ↓ ↓                               | ↓ ↓                              |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 1100 | H                 | L                 | -----                             | 2,097,148 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 1101 | H                 | L                 | -----                             | 2,097,149 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 1110 | H                 | L                 | -----                             | 2,097,150 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 1111 | H                 | L                 | -----                             | 2,097,151 Add.                   |

### 8-BIT BUS ORGANIZATION ( $\overline{CE}_1 = V_{IH}$ , $\overline{CE}_2 = V_{IL}$ ) \*2

| A <sub>20</sub> to A <sub>0</sub> |      |      |      |      |      | $\overline{CE}_2$ | $\overline{CE}_1$ | D <sub>15</sub> to D <sub>8</sub> | D <sub>7</sub> to D <sub>0</sub> |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 0                                 | 0000 | 0000 | 0000 | 0000 | 000x | L                 | H                 | 1 Add.                            | -----                            |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 001x | L                 | H                 | 3 Add.                            | -----                            |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 010x | L                 | H                 | 5 Add.                            | -----                            |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 011x | L                 | H                 | 7 Add.                            | -----                            |
| ↓                                 | ↓    | ↓    | ↓    | ↓    | ↓    | ↓                 | ↓                 | ↓ ↓                               | ↓ ↓                              |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 100x | L                 | H                 | 2,097,145 Add.                    | -----                            |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 101x | L                 | H                 | 2,097,147 Add.                    | -----                            |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 110x | L                 | H                 | 2,097,149 Add.                    | -----                            |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 111x | L                 | H                 | 2,097,151 Add.                    | -----                            |

### 16-BIT BUS ORGANIZATION ( $\overline{CE}_1 = V_{IL}$ , $\overline{CE}_2 = V_{IL}$ )

| A <sub>20</sub> to A <sub>0</sub> |      |      |      |      |      | $\overline{CE}_2$ | $\overline{CE}_1$ | D <sub>15</sub> to D <sub>8</sub> | D <sub>7</sub> to D <sub>0</sub> |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 0                                 | 0000 | 0000 | 0000 | 0000 | 000x | L                 | L                 | 1 Add.                            | 0 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 001x | L                 | L                 | 3 Add.                            | 2 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 010x | L                 | L                 | 5 Add.                            | 4 Add.                           |
| 0                                 | 0000 | 0000 | 0000 | 0000 | 011x | L                 | L                 | 7 Add.                            | 6 Add.                           |
| ↓                                 | ↓    | ↓    | ↓    | ↓    | ↓    | ↓                 | ↓                 | ↓ ↓                               | ↓ ↓                              |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 100x | L                 | L                 | 2,097,145 Add.                    | 2,097,144 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 101x | L                 | L                 | 2,097,147 Add.                    | 2,097,146 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 110x | L                 | L                 | 2,097,149 Add.                    | 2,097,148 Add.                   |
| 1                                 | 1111 | 1111 | 1111 | 1111 | 111x | L                 | L                 | 2,097,151 Add.                    | 2,097,150 Add.                   |

Notes: \*1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Either 0 or 1.

\*2. Even addresses are not available in this mode.



# MB98A9083x/9093x/9103x/9113x-20

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter           | Symbol    | Value                  | Unit |
|---------------------|-----------|------------------------|------|
| Supply Voltage      | $V_{CC}$  | -0.5 to +6.0           | V    |
| Input Voltage       | $V_{IN}$  | -0.5 to $V_{CC} + 0.5$ | V    |
| Output Voltage      | $V_{OUT}$ | -0.5 to $V_{CC} + 0.5$ | V    |
| Ambient Temperature | $T_A$     | -10 to +60 *1          | °C   |
| Storage Temperature | $T_{STG}$ | -20 to +65 *2          | °C   |

**Notes:** \*1. This value does not apply to the replaceable battery.

\*2. This value does not apply to the replaceable battery and data retention.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

| Parameter             | Symbol   | Min. | Typ. | Max.           | Unit |
|-----------------------|----------|------|------|----------------|------|
| Supply Voltage        | $V_{CC}$ | 4.75 | 5.0  | 5.25           | V    |
| Ground                | GND      | —    | 0    | —              | V    |
| Input High Voltage    | $V_{IH}$ | 2.4  | —    | $V_{CC} + 0.3$ | V    |
| Input Low Voltage     | $V_{IL}$ | -0.3 | —    | 0.8            | V    |
| Ambient Temperature * | $T_A$    | 0    | —    | 55             | °C   |

**Note:** \* This value does not apply to the replaceable lithium battery. See  $V_{BAT1}$  in Fig.1.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

( $T_A = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ ,  $V_{IN} = V_{I/O} = \text{GND}$ )

| Parameter         | Notes | Symbol    | Min. | Typ. | Max. | Unit |
|-------------------|-------|-----------|------|------|------|------|
| Input Capacitance | *1    | $C_{IN}$  | —    | —    | 50   | pF   |
| I/O Capacitance   | *2    | $C_{I/O}$ | —    | —    | 50   | pF   |

**Notes:** \*1. This value does not apply to  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{REG}$  and  $\overline{WE}$ .

\*2. This value does not apply to  $\overline{BVD}_1$ ,  $\overline{BVD}_2$ ,  $\overline{CD}_1$  and  $\overline{CD}_2$ .

# MB98A9083x/9093x/9103x/9113x-20

## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

| Parameter                | Notes            | Symbol           | Condition  | Min. | Typ. | Max. | Unit |
|--------------------------|------------------|------------------|--|------|------|------|------|
| Standby Supply Current   | *1               | I <sub>SB1</sub> | $\overline{CE}_1, \overline{CE}_2 \geq V_{CC} - 0.2 \text{ V}$   | —    | —    | 0.5  | mA   |
|                          |                  | I <sub>SB2</sub> | $\overline{CE}_1, \overline{CE}_2 = V_{IH}$  | —    | —    | 5.0  | mA   |
| Active Supply Current    |                  | I <sub>CC1</sub> | $V_{IN} = V_{IH} \text{ or } V_{IL}$<br>$\overline{CE}_1, \overline{CE}_2 = V_{IL}, I_{OUT} = 0 \text{ mA}$                                    | —    | —    | 50   | mA   |
| Operating Supply Current | MB98A9083x/9093x | I <sub>CC2</sub> | $V_{IN} = V_{IH} \text{ or } V_{IL}$ , Cycle = Min<br>Duty = 100%, I <sub>OUT</sub> = 0 mA<br>$\overline{OE} = V_{IH}$ during Write Cycle      | —    | —    | 180  | mA   |
|                          | MB98A9103x/9113x |                  |  | —    | —    | 240  |      |
| Input Leakage Current    | *2               | I <sub>LI</sub>  | $V_{IN} = 0 \text{ V to } V_{CC}$  | -10  | —    | 10   | μA   |
| Output Leakage Current   | *3               | I <sub>L/O</sub> | $V_{OUT} = 0 \text{ V to } V_{CC}$ ,<br>$\overline{CE}_1, \overline{CE}_2 = V_{IH}$ or<br>$\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ | -10  | —    | 10   | μA   |
| Output High Voltage      | *4               | V <sub>OH</sub>  | I <sub>OH</sub> = -1.0 mA  | 2.4  | —    | —    | V    |
| Output Low Voltage       |                  | V <sub>OL</sub>  | I <sub>OL</sub> = 2.1 mA   | —    | —    | 0.4  | V    |

**Notes:** \*1. This value does not apply to recharge current from system or replaceable lithium battery to rechargeable battery.

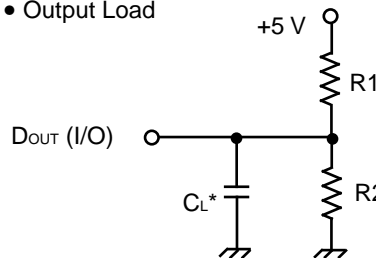
\*2. This value does not apply to  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{REG}$  and  $\overline{WE}$ .

\*3. This value does not apply to BVD1, BVD2,  $\overline{CD}_1$ ,  $\overline{CD}_2$  and WP.

\*4. This value does not apply to  $\overline{CD}_1$  and  $\overline{CD}_2$ .

**Fig. 3 – AC TEST CONDITIONS**

• Output Load



• Input Pulse Levels: 0.6 V to 2.6 V

• Input Pulse Rise and Fall Times: 5 ns (Transition between 0.8 V and 2.4 V)

• Timing Reference Levels

Input:  $V_{IL} = 0.8 \text{ V}$ ,  $V_{IH} = 2.4 \text{ V}$

Output:  $V_{OL} = 0.8 \text{ V}$ ,  $V_{OH} = 2.0 \text{ V}$

\* Including Jig and stray capacitance

|         | R1     | R2    | CL     | Parameters Measured   |
|---------|--------|-------|--------|---|
| Load I  | 1.8 kΩ | 990 Ω | 100 pF | All parameters except t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>RCLZ</sub> , t <sub>ROLZ</sub> , t <sub>RCHZ</sub> , t <sub>ROHZ</sub> , t <sub>WLZ</sub> and t <sub>WHZ</sub> |
| Load II | 1.8 kΩ | 990 Ω | 5 pF   | t <sub>CLZ</sub> , t <sub>OLZ</sub> , t <sub>CHZ</sub> , t <sub>OHZ</sub> , t <sub>RCLZ</sub> , t <sub>ROLZ</sub> , t <sub>RCHZ</sub> , t <sub>ROHZ</sub> , t <sub>WLZ</sub> and t <sub>WHZ</sub>                       |

# MB98A9083x/9093x/9103x/9113x-20

## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE

| Parameter                       | Notes | Symbol           | Min. | Max. | Unit |
|---------------------------------|-------|------------------|------|------|------|
| Read Cycle Time                 |       | t <sub>RC</sub>  | 200  | —    | ns   |
| Address Access Time             |       | t <sub>AA</sub>  | —    | 200  | ns   |
| Card Enable Access Time         |       | t <sub>CE</sub>  | —    | 200  | ns   |
| Output Enable Access Time       |       | t <sub>OE</sub>  | —    | 100  | ns   |
| Output Hold from Address Change |       | t <sub>OH</sub>  | 5    | —    | ns   |
| Card Enable to Output Low-Z     | *1, 2 | t <sub>CLZ</sub> | 5    | —    | ns   |
| Output Enable to Output Low-Z   | *1, 2 | t <sub>OLZ</sub> | 5    | —    | ns   |
| Card Enable to Output High-Z    | *1, 2 | t <sub>CHZ</sub> | —    | 50   | ns   |
| Output Enable to Output High-Z  | *1, 2 | t <sub>OHZ</sub> | —    | 50   | ns   |

### ATTRIBUTE MEMORY READ CYCLE \*3

| Parameter                       | Notes | Symbol            | Min. | Max. | Unit |
|---------------------------------|-------|-------------------|------|------|------|
| Read Cycle Time                 |       | t <sub>RRC</sub>  | 300  | —    | ns   |
| Address Access Time             |       | t <sub>RAA</sub>  | —    | 300  | ns   |
| Card Enable Access Time         |       | t <sub>RCE</sub>  | —    | 300  | ns   |
| Output Enable Access Time       |       | t <sub>ROE</sub>  | —    | 150  | ns   |
| Output Hold from Address Change |       | t <sub>ROH</sub>  | 5    | —    | ns   |
| Card Enable to Output Low-Z     | *1, 2 | t <sub>RCLZ</sub> | 5    | —    | ns   |
| Output Enable to Output Low-Z   | *1, 2 | t <sub>ROLZ</sub> | 5    | —    | ns   |
| Card Enable to Output High-Z    | *1, 2 | t <sub>RCHZ</sub> | —    | 60   | ns   |
| Output Enable to Output High-Z  | *1, 2 | t <sub>ROHZ</sub> | —    | 60   | ns   |

**Notes:** \*1. Transition is measured at the point of  $\pm 500$  mV from steady state voltage.

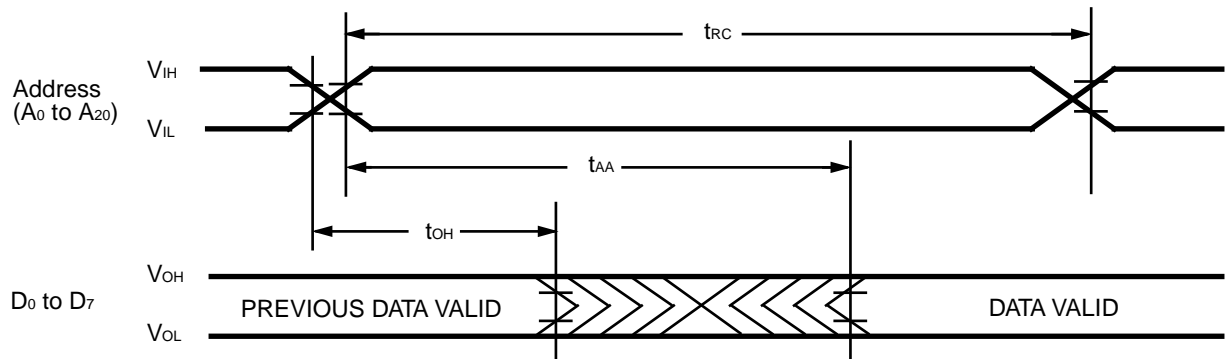
\*2. This parameter is specified using Load II in Fig.3.

\*3. This parameter is for MB98A90833, 90933, 91033 and 91133.

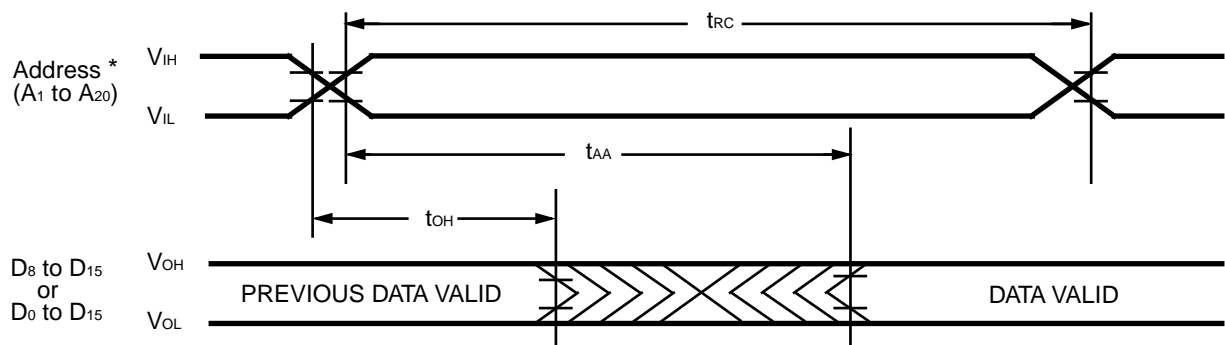
# MB98A9083x/9093x/9103x/9113x-20


## MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IH}$ )

READ CYCLE 1:  $\overline{CE}_1 = \overline{OE} = V_{IL}$ ,  $\overline{CE}_2 = V_{IH}$ : × 8-bit Bus Organization



READ CYCLE 2:  $\overline{CE}_1 = V_{IH}$ ,  $\overline{CE}_2 = \overline{OE} = V_{IL}$ : × 8-bit Bus Organization  
 $\overline{CE}_1 = \overline{CE}_2 = \overline{OE} = V_{IL}$ : × 16-bit Bus Organization



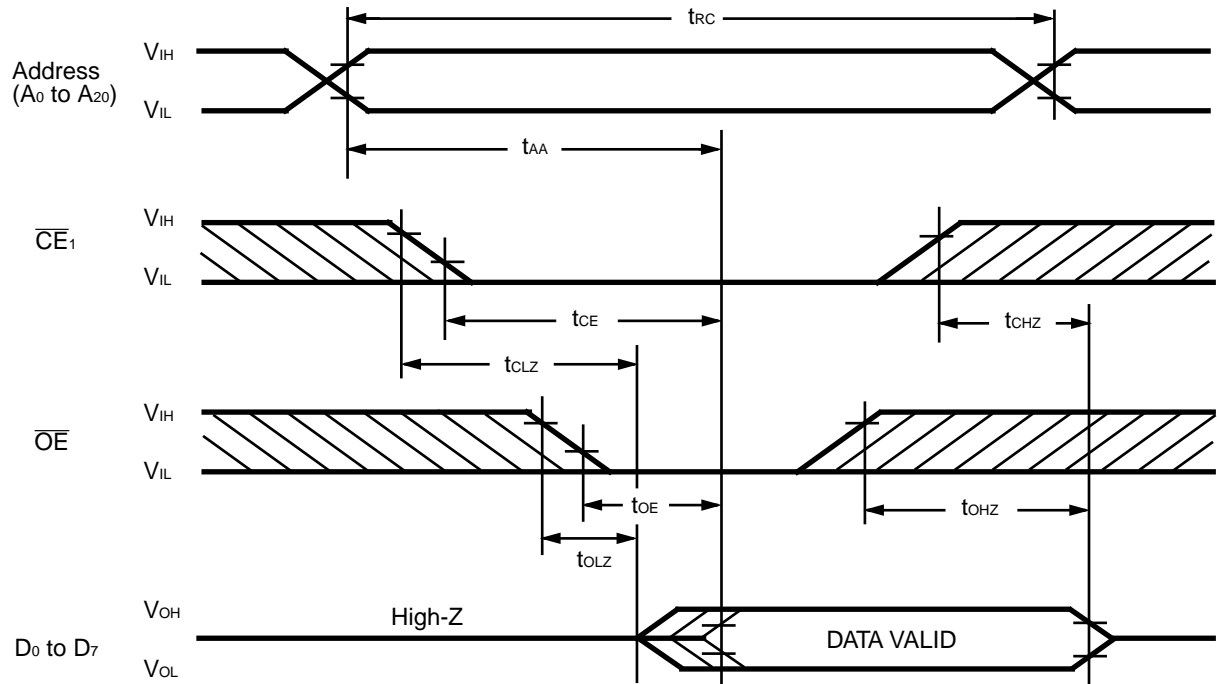
 : Undefined

**Note:** \* A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub>.

# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IH}$ )

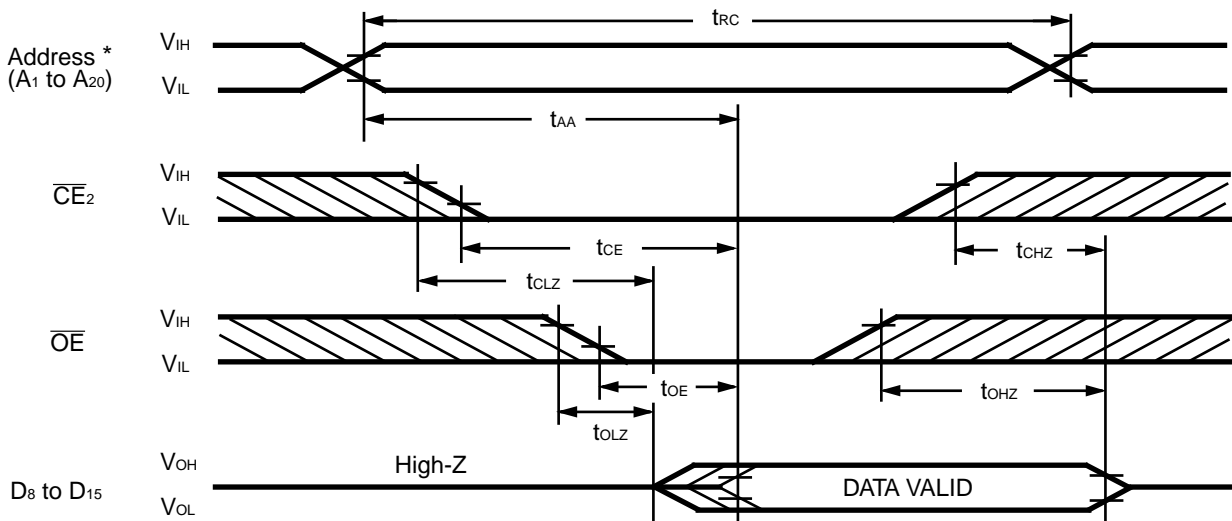
READ CYCLE 3:  $\overline{CE}_2 = V_{IH}$ : × 8-bit Bus Organization



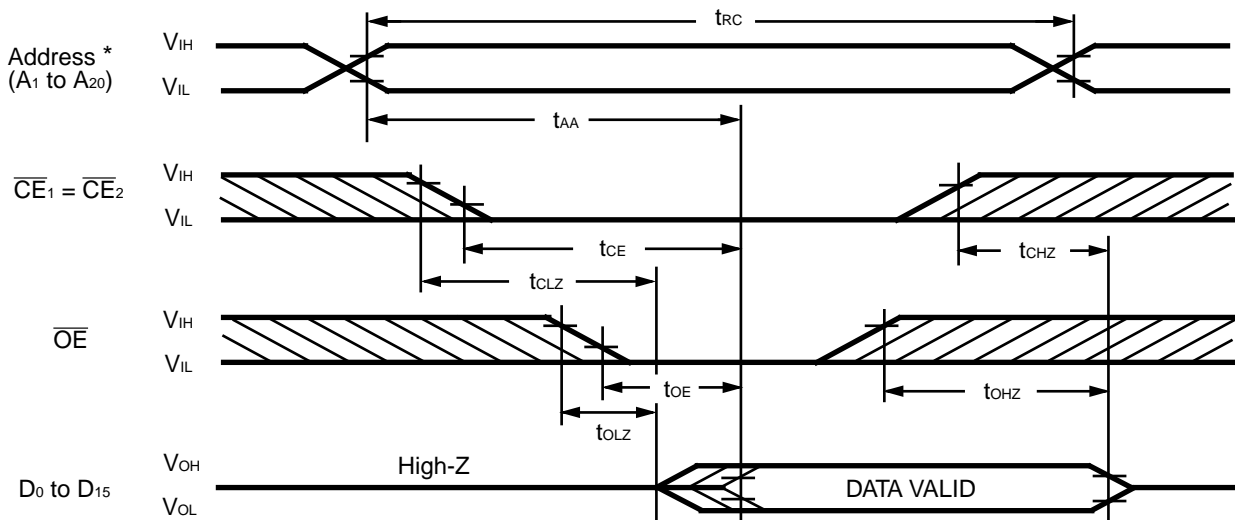
# MB98A9083x/9093x/9103x/9113x-20


## MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IH}$ )

READ CYCLE 4:  $\overline{CE}_1 = V_{IH}$ : × 8-bit Bus Organization



READ CYCLE 5:  $\overline{CE}_1 = \overline{CE}_2$ : × 16-bit Bus Organization

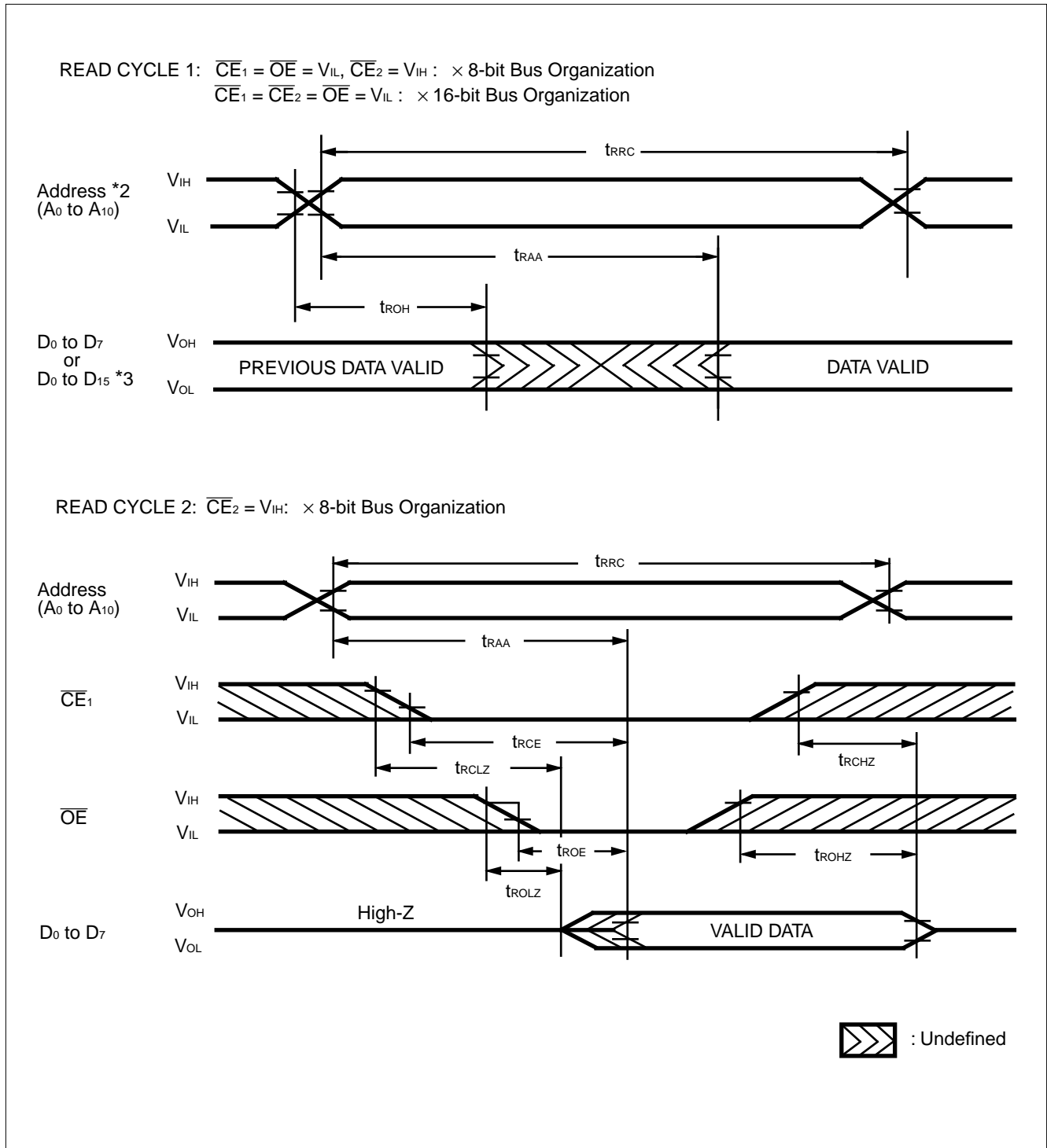


 : Undefined

Note: \* A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub>.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IL}$ ) \*1



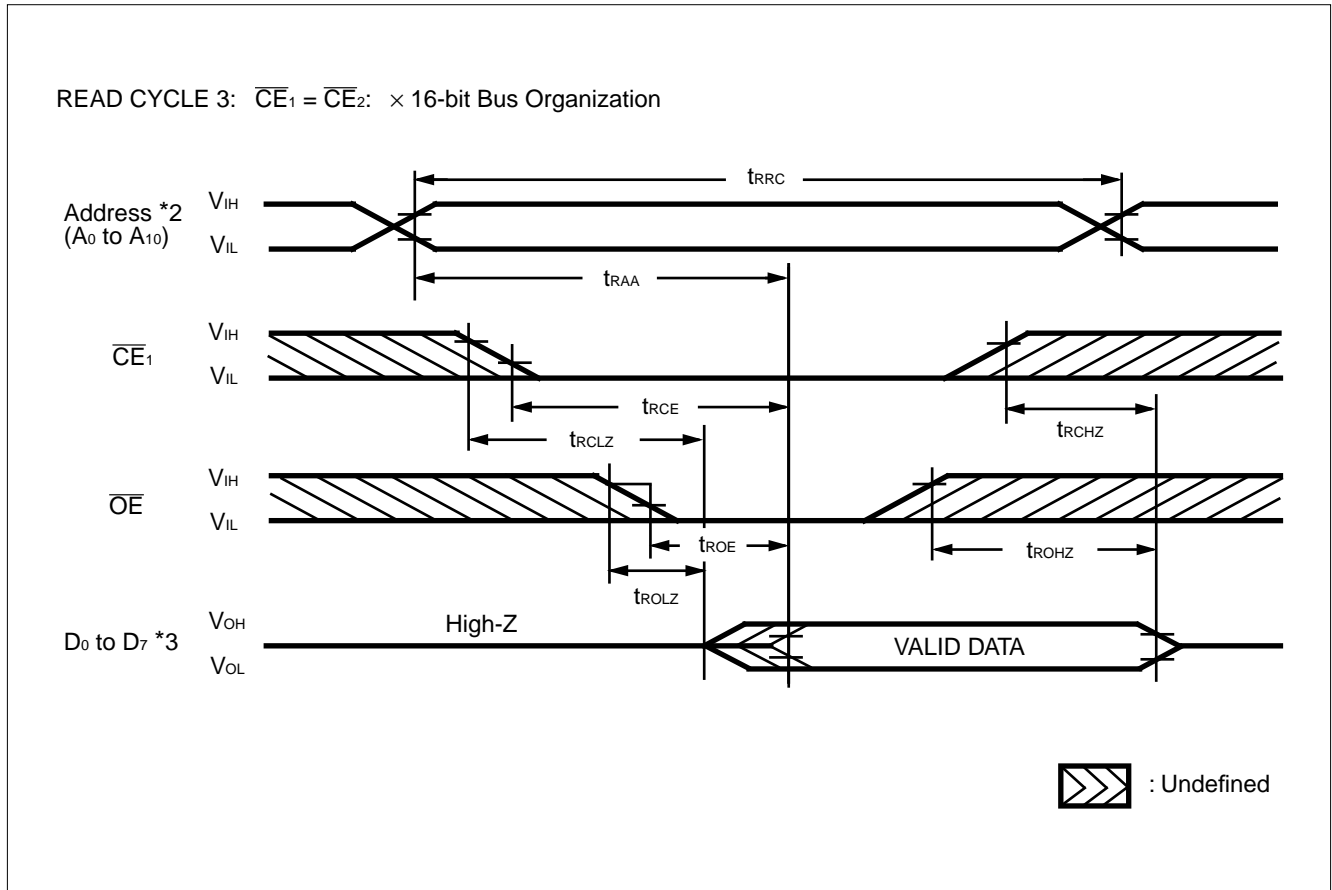
**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033 and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub> for a 16-bit bus organization.

\*3. H-level is output from D<sub>8</sub> to D<sub>15</sub>.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = V_{IH}$ , $\overline{REG} = V_{IL}$ ) \*1



**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub>.

\*3. H-level is output from D<sub>8</sub> to D<sub>15</sub>.



# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY WRITE CYCLE \*1

| Parameter                      | Notes | Symbol           | Min. | Max. | Unit |
|--------------------------------|-------|------------------|------|------|------|
| Write Cycle Time               |       | t <sub>WC</sub>  | 200  | —    | ns   |
| Address Valid to End of Write  |       | t <sub>AW</sub>  | 140  | —    | ns   |
| Chip Select to End of Write    |       | t <sub>CW</sub>  | 140  | —    | ns   |
| Data Valid to End of Write     |       | t <sub>DW</sub>  | 60   | —    | ns   |
| Data Hold Time                 |       | t <sub>DH</sub>  | 30   | —    | ns   |
| Write Pulse Width              |       | t <sub>WP</sub>  | 120  | —    | ns   |
| Address Set Up Time            |       | t <sub>AS</sub>  | 20   | —    | ns   |
| Write Recovery Time            |       | t <sub>WR</sub>  | 30   | —    | ns   |
| Output Enable to Output Low-Z  | *2    | t <sub>OLZ</sub> | 5    | —    | ns   |
| Output Enable to Output High-Z | *2    | t <sub>OHZ</sub> | —    | 50   | ns   |
| Write Enable to Output Low-Z   | *2, 3 | t <sub>WLZ</sub> | 5    | —    | ns   |
| Write Enable to Output High-Z  | *2, 3 | t <sub>WHZ</sub> | —    | 50   | ns   |
| Output Enable Set Up Time      |       | t <sub>OES</sub> | 10   | —    | ns   |
| Output Enable Hold Time        |       | t <sub>OEH</sub> | 10   | —    | ns   |

## ATTRIBUTE MEMORY WRITE CYCLE \*4

| Parameter                   | Symbol            | Min.  | Max. | Unit  |
|-----------------------------|-------------------|-------|------|-------|
| Byte Write Cycle Time       | t <sub>RWR</sub>  | —     | 10   | ms    |
| Address Set Up Time         | t <sub>RAS</sub>  | 20    | —    | ns    |
| Chip Enable Set Up Time     | t <sub>RCS</sub>  | 0     | —    | ns    |
| Output Enable Set Up Time   | t <sub>ROES</sub> | 20    | —    | ns    |
| Write Pulse Width           | t <sub>RWP</sub>  | 100   | —    | ns    |
| Address Hold Time           | t <sub>RAH</sub>  | 50    | —    | ns    |
| Data Set Up Time            | t <sub>RDS</sub>  | 50    | —    | ns    |
| Data Hold Time              | t <sub>RDH</sub>  | 20    | —    | ns    |
| Chip Enable Hold Time       | t <sub>RCH</sub>  | 0     | —    | ns    |
| Output Enable Hold Time     | t <sub>ROEH</sub> | 20    | —    | ns    |
| Write Recovery Time         | t <sub>RRE</sub>  | 50    | —    | ns    |
| End of Write to Output Time | t <sub>RRBO</sub> | —     | 100  | ns    |
| Number of Write per Byte    | N                 | 10000 | —    | Times |
| Write Enable Hold Time      | t <sub>RWEH</sub> | 10    | —    | ns    |

**Notes:** \*1. If  $\overline{OE}$ ,  $\overline{CE}_1$ , and  $\overline{CE}_2$  are in the Read Mode during this period, then the I/O pins are in the output state and the input signals of the phase opposite to the outputs must be applied.

\*2. Transition is measured at the point of  $\pm 500$  mV from steady state voltage.

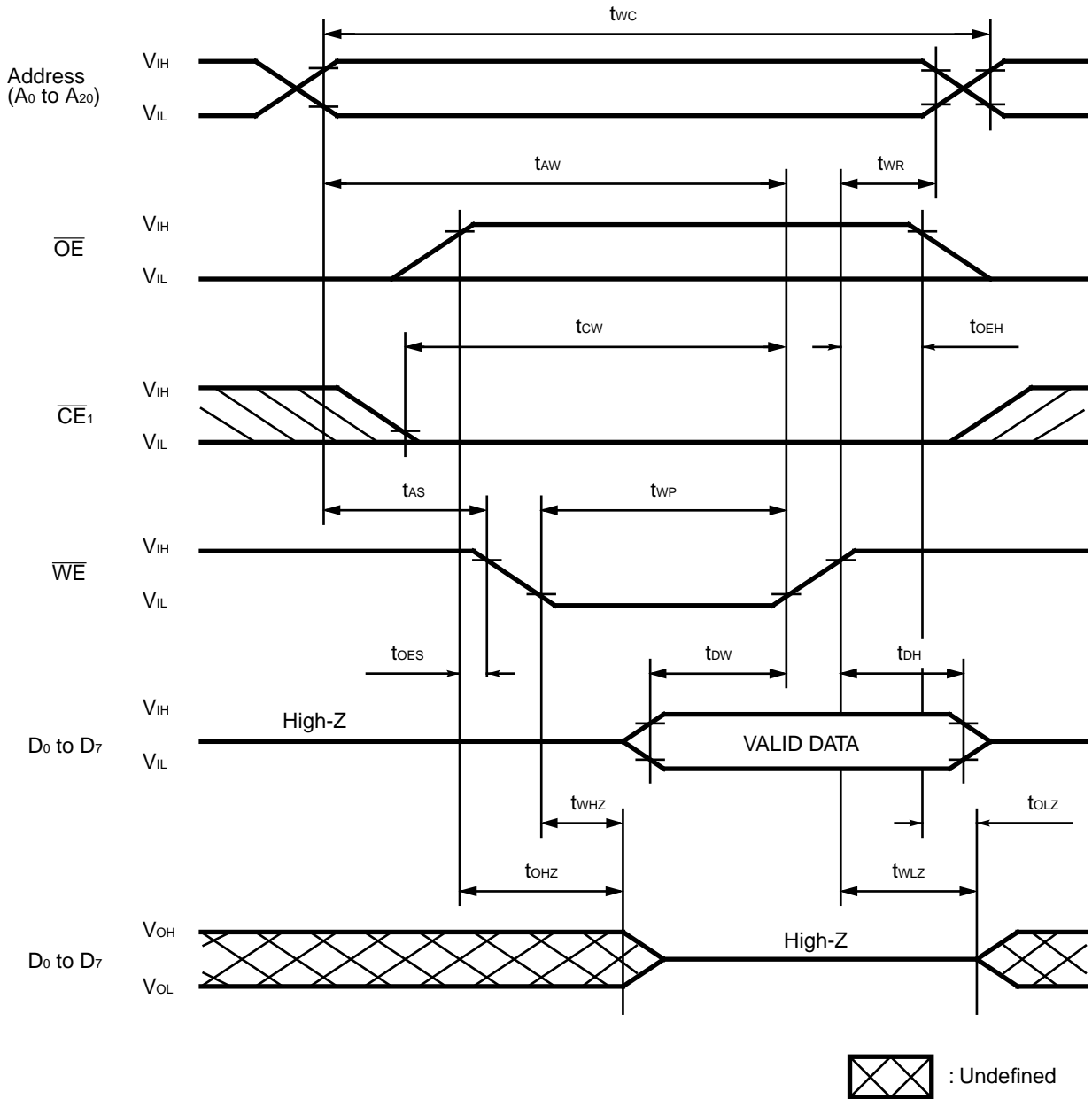
\*3. This parameter is specified only during write cycle with  $\overline{OE} = V_{IL}$  and specified using Load II in Fig.3.

\*4. This parameter is for MB98A90833, 90933, 91033 and 91133.

# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )

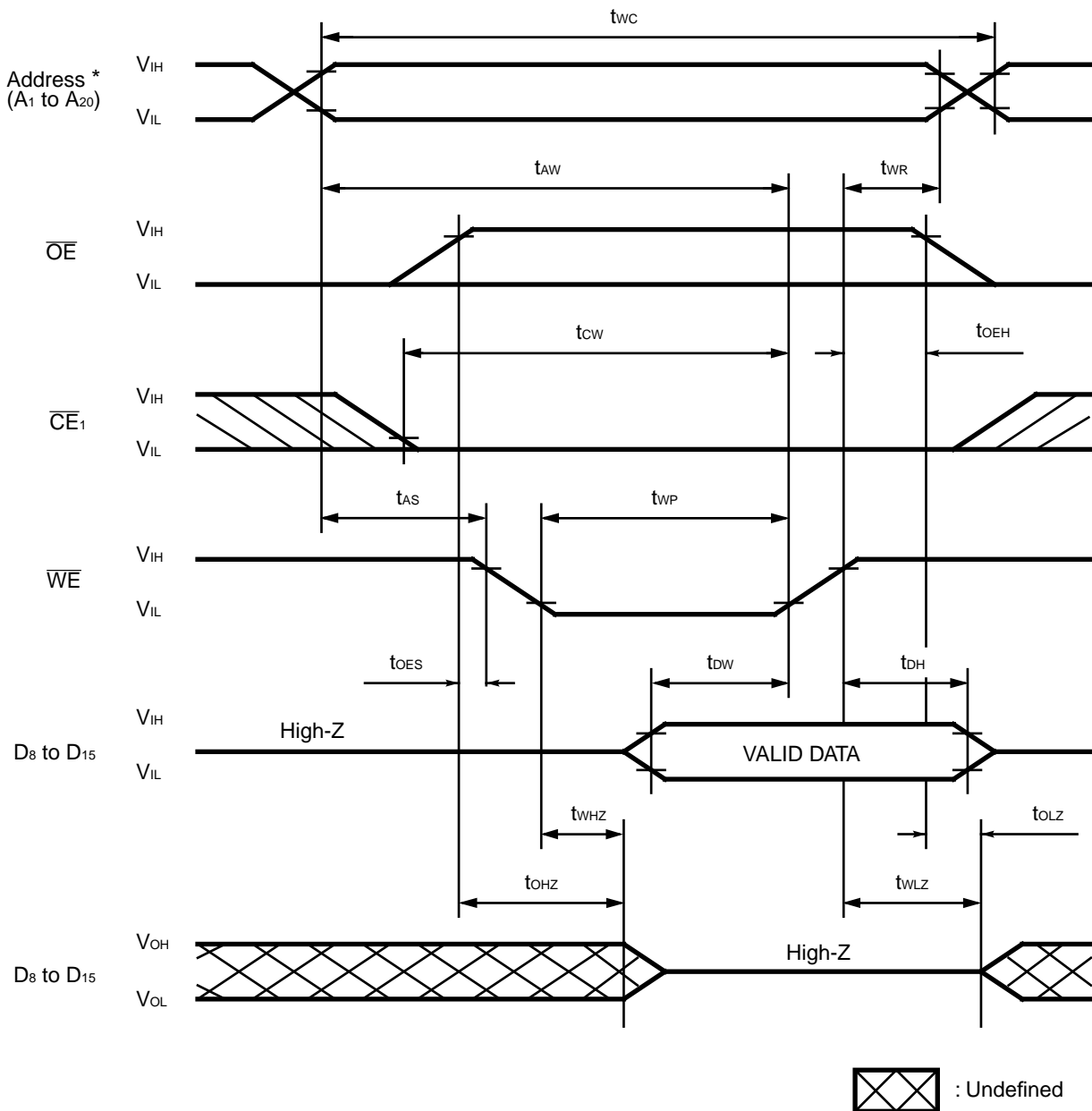
WRITE CYCLE 1:  $\overline{CE}_2 = V_{IH}$  : × 8-bit Bus Organization



# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )

WRITE CYCLE 2:  $\overline{CE}_1 = V_{IH}$  : × 8-bit Bus Organization

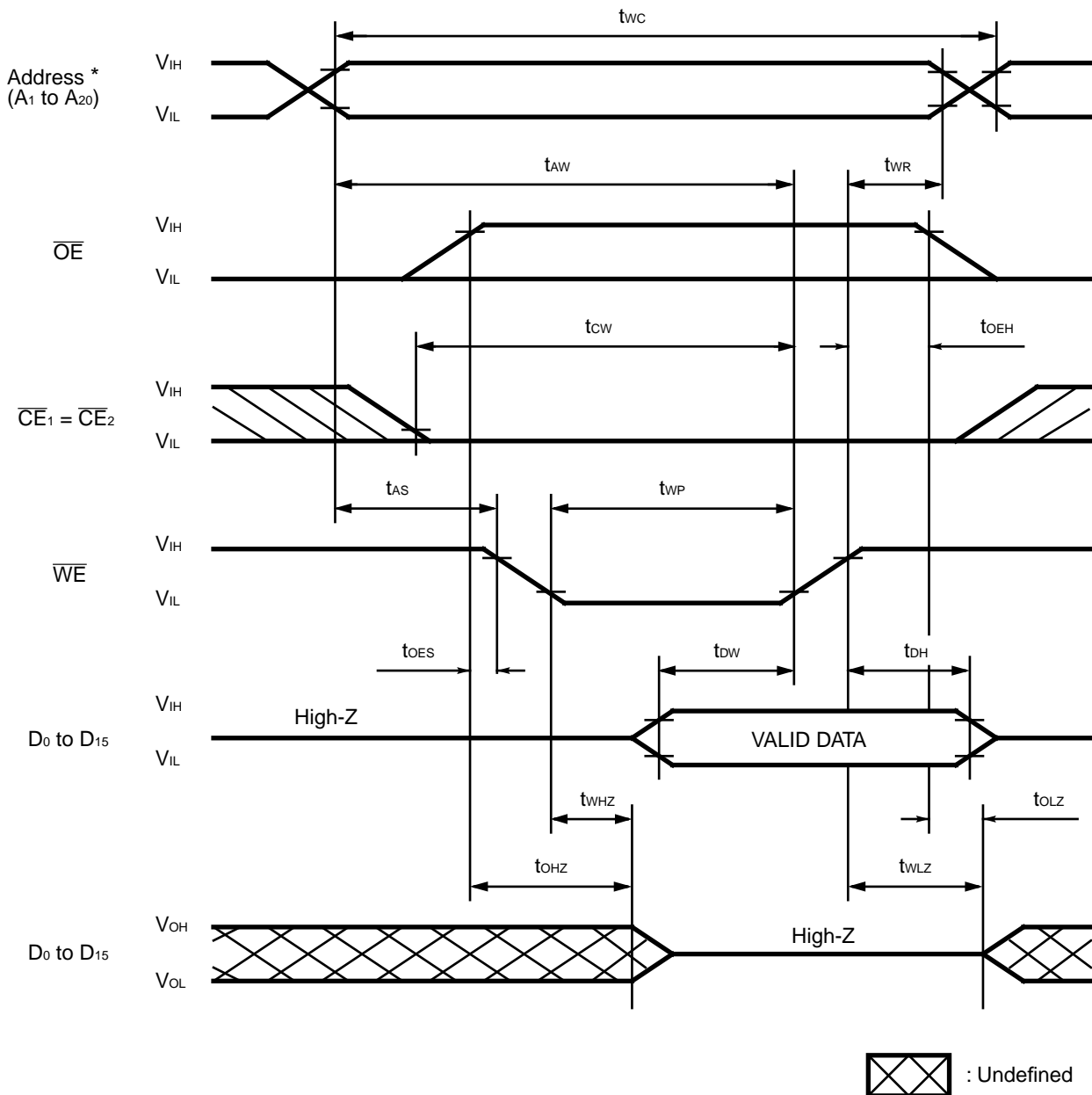


Note: \*  $A_0 = \text{Either } V_{IH} \text{ or } V_{IL}$ .

# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )

WRITE CYCLE 3:  $\overline{CE}_1 = \overline{CE}_2$  :  $\times 16$ -bit Bus Organization

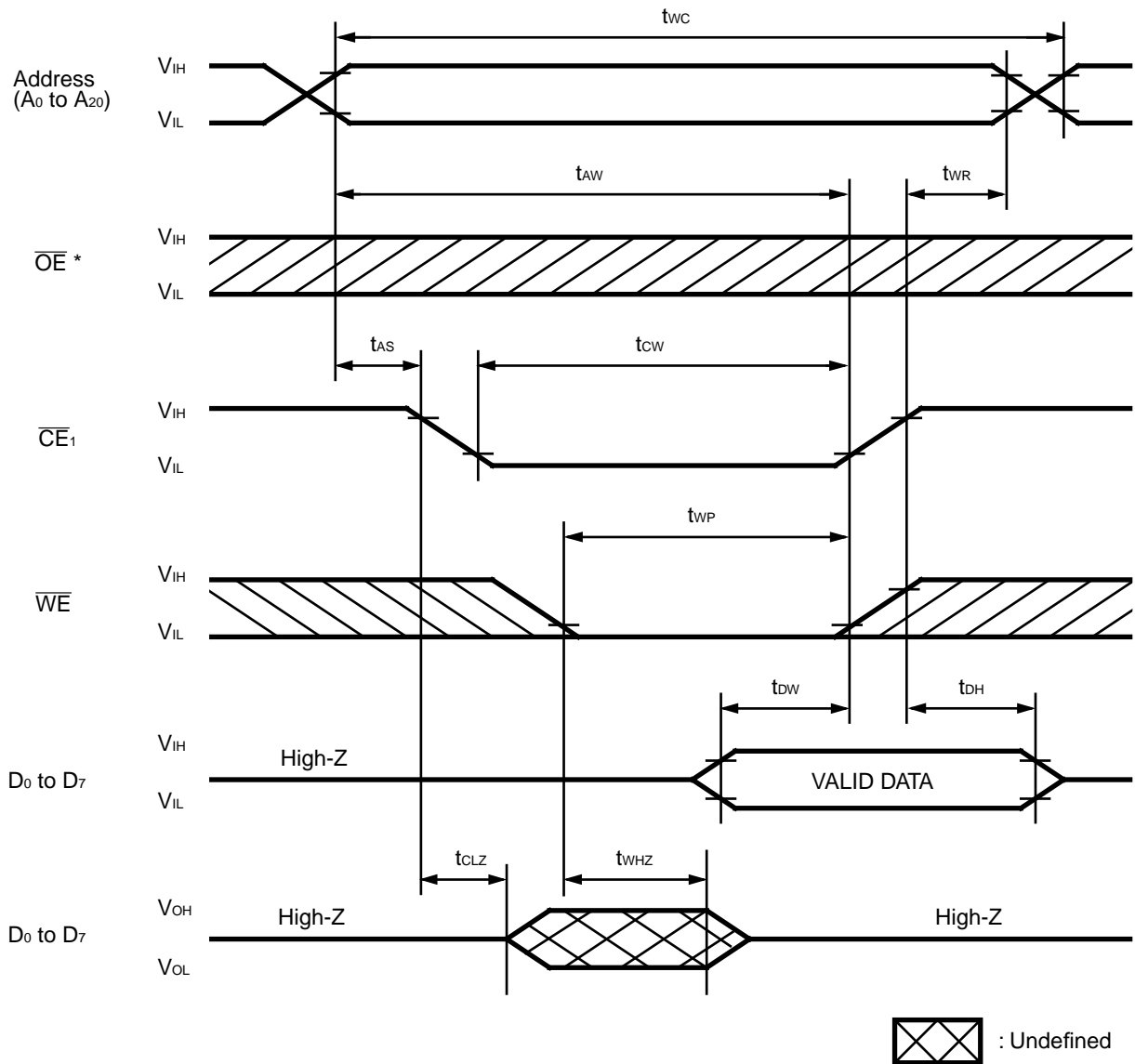


**Note:** \* A<sub>0</sub> = Either  $V_{IH}$  or  $V_{IL}$ .

# MB98A9083x/9093x/9103x/9113x-20

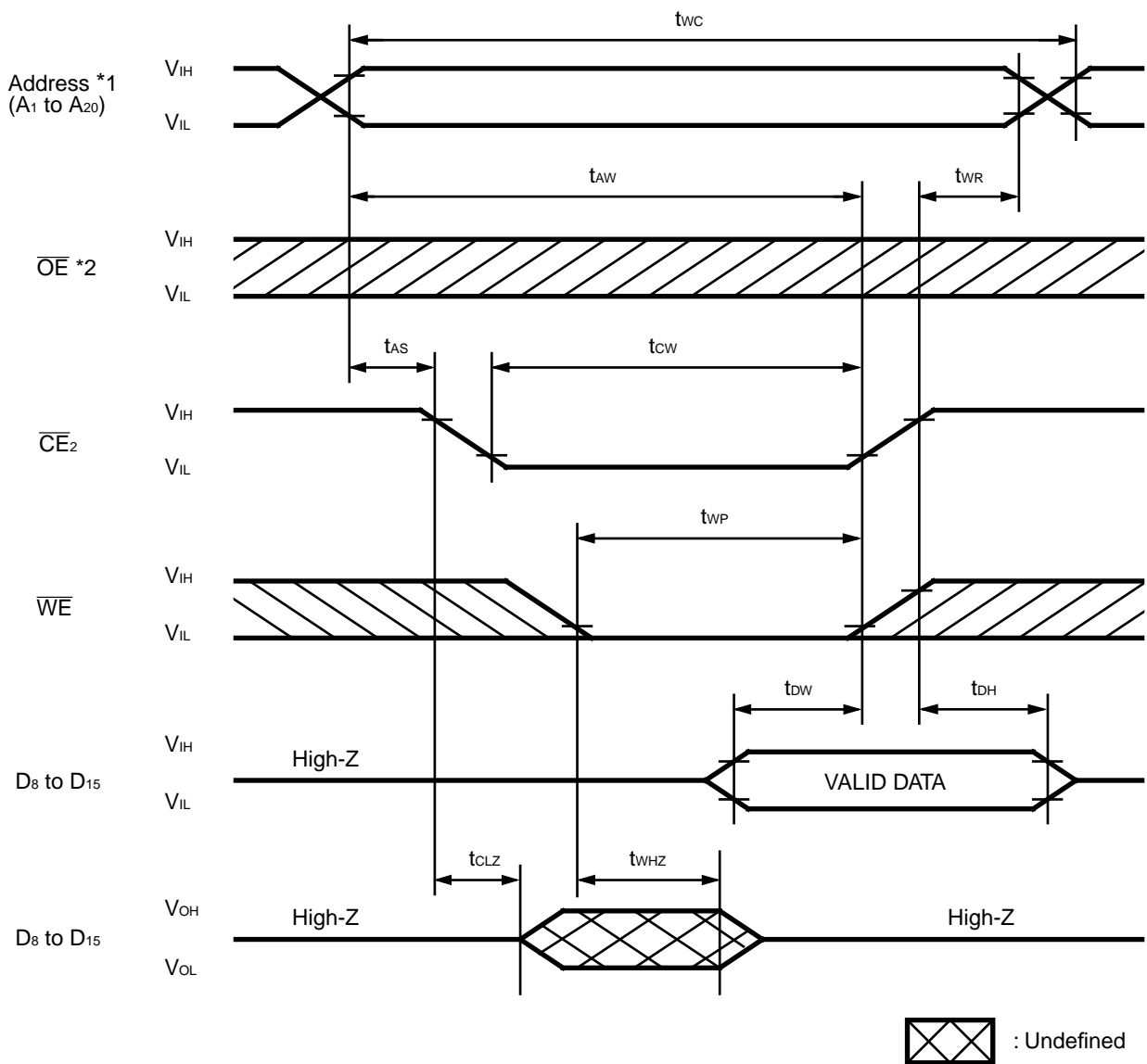
## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )

WRITE CYCLE 4:  $\overline{CE}_2 = V_{IL}$  : × 8-bit Bus Organization



**Note:** \* H-level is recommended for stable operation though the card is operable at L-level.

## MB98A9083x/9093x/9103x/9113x-20

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ ,  $\overline{REG} = V_{IH}$ )WRITE CYCLE 5:  $\overline{CE}_1 = V_{IL}$  : × 8-bit Bus Organization

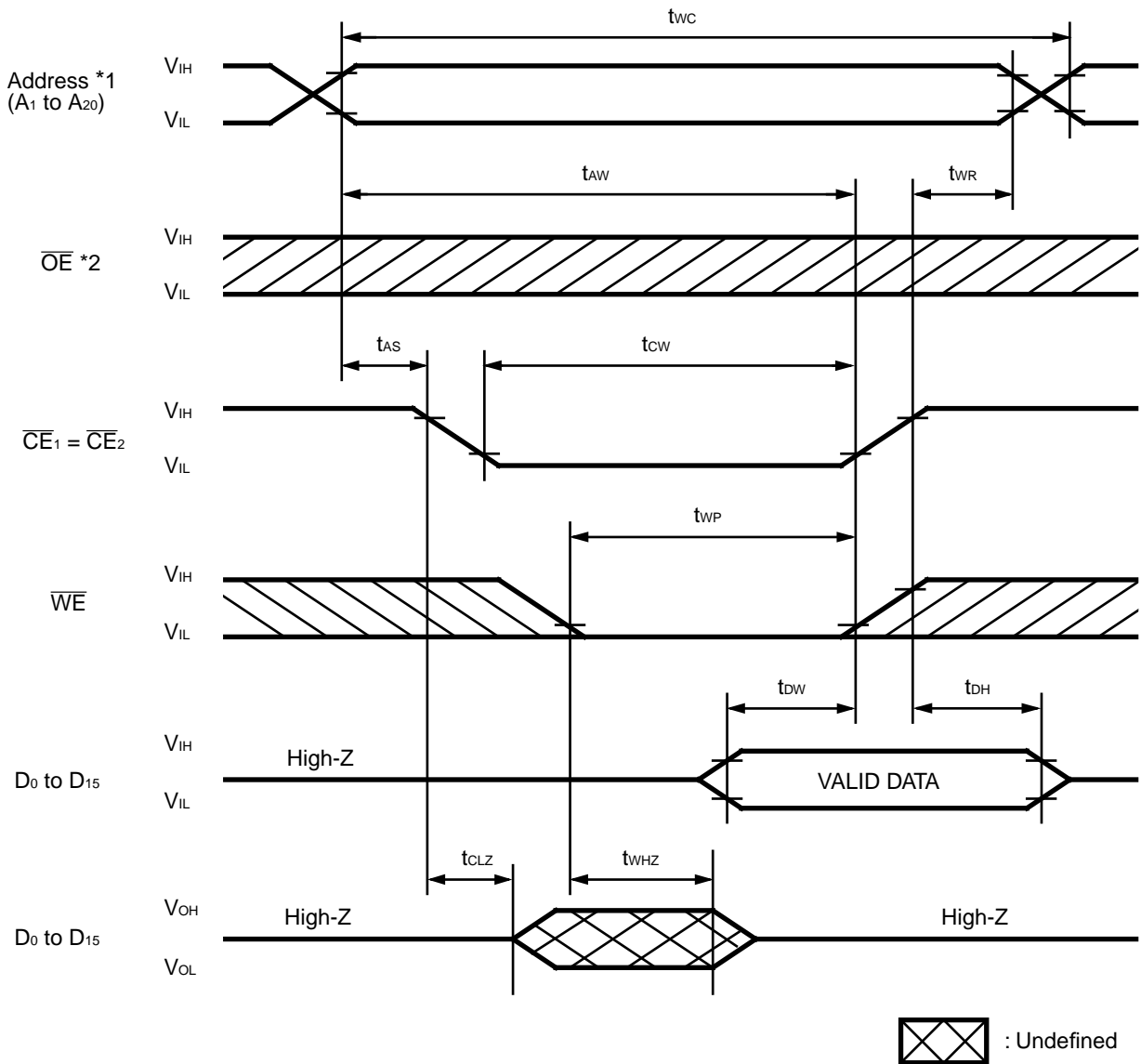
**Notes:** \*1. A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub>.

\*2. H-level is recommended for stable operation though the card is operable at L-level.

# MB98A9083x/9093x/9103x/9113x-20

## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )

WRITE CYCLE 6:  $\overline{CE}_1 = \overline{CE}_2$  : × 16-bit Bus Organization

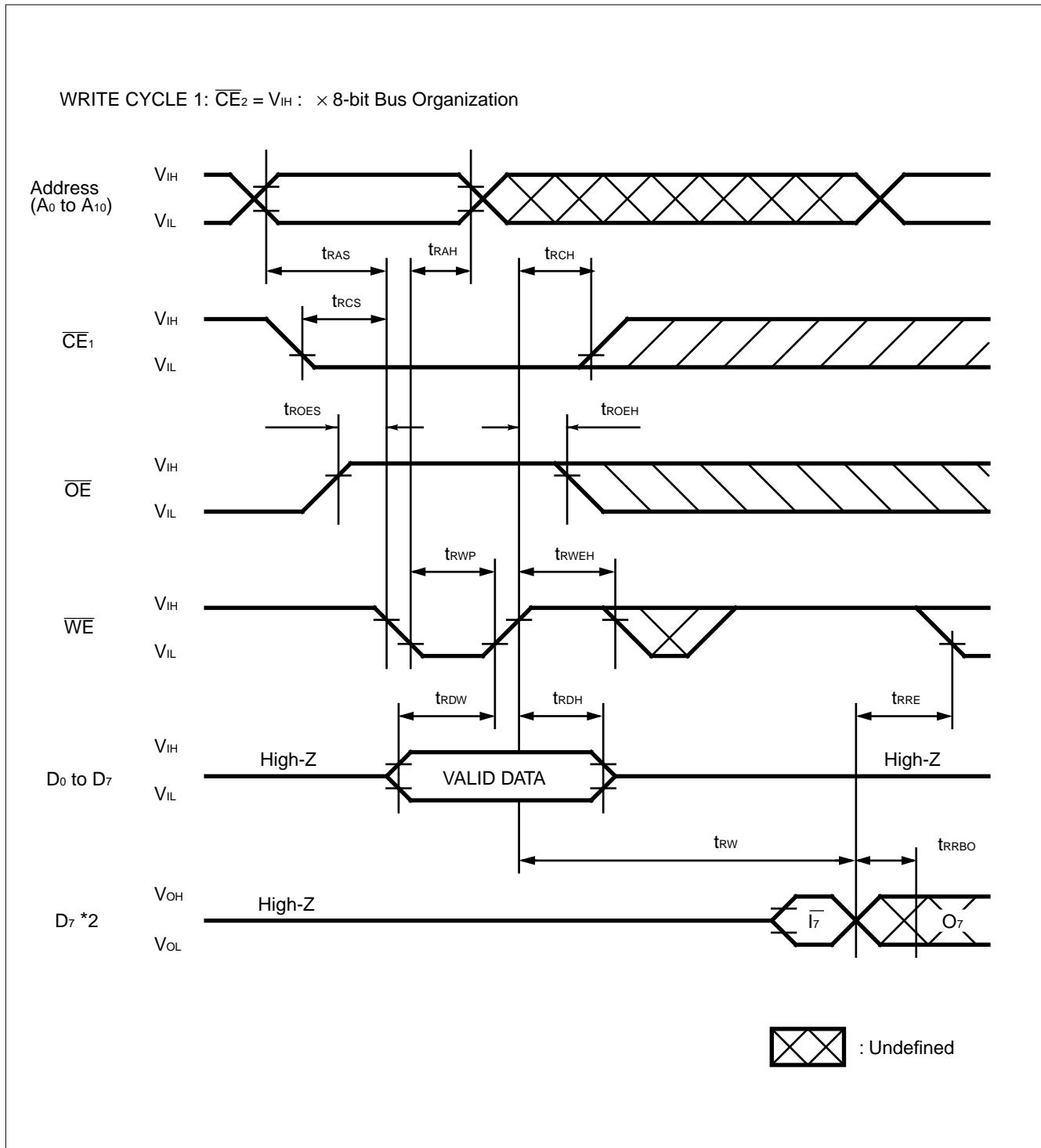


**Notes:** \*1. A<sub>0</sub> = Either V<sub>IH</sub> or V<sub>IL</sub>.

\*2. H-level is recommended for stable operation though the card is operable at L-level.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IL}$ ) \*1



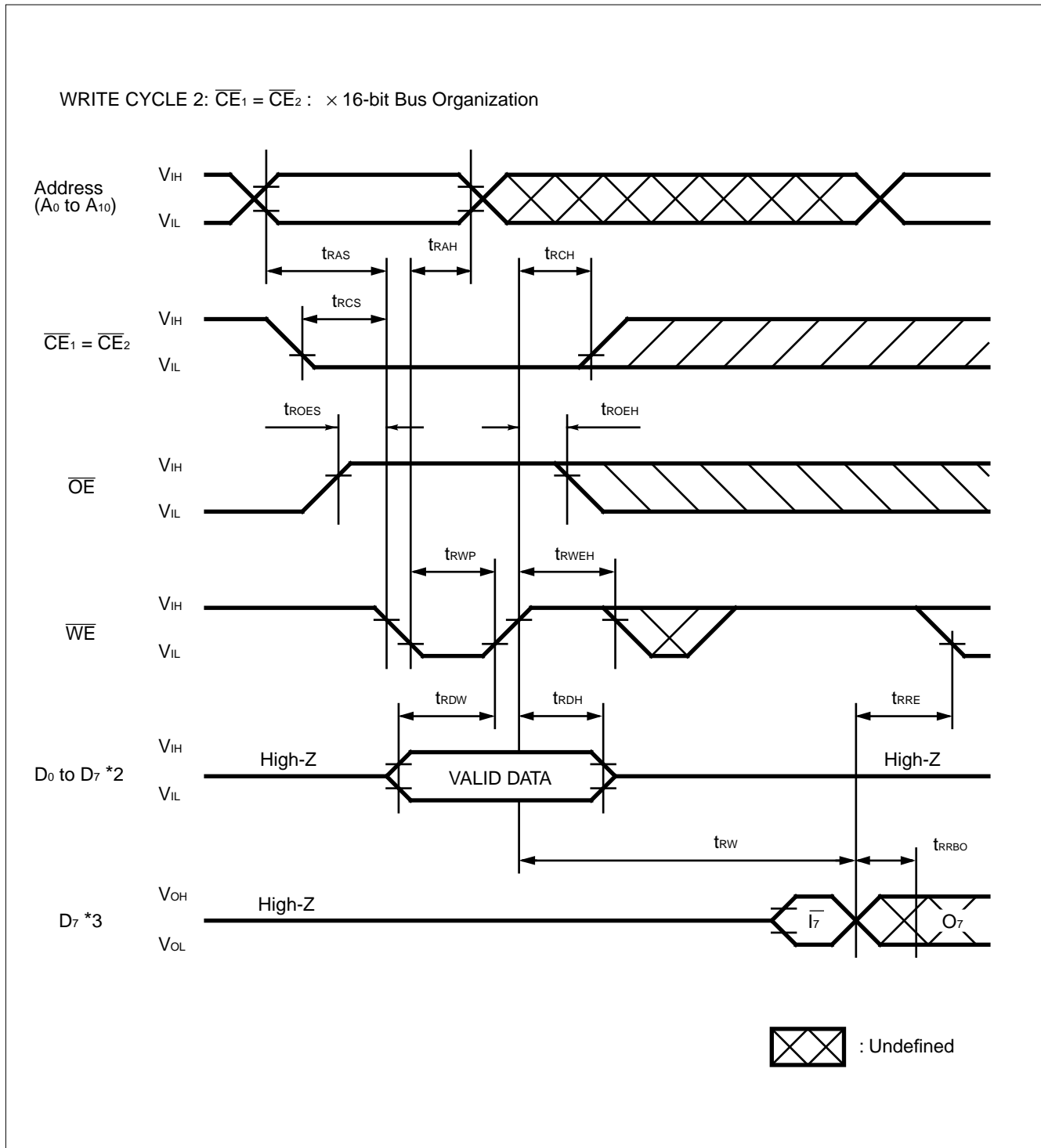
**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. Data polling operation.



# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ = CONTROLLED, $\overline{REG} = V_{IL}$ ) \*1



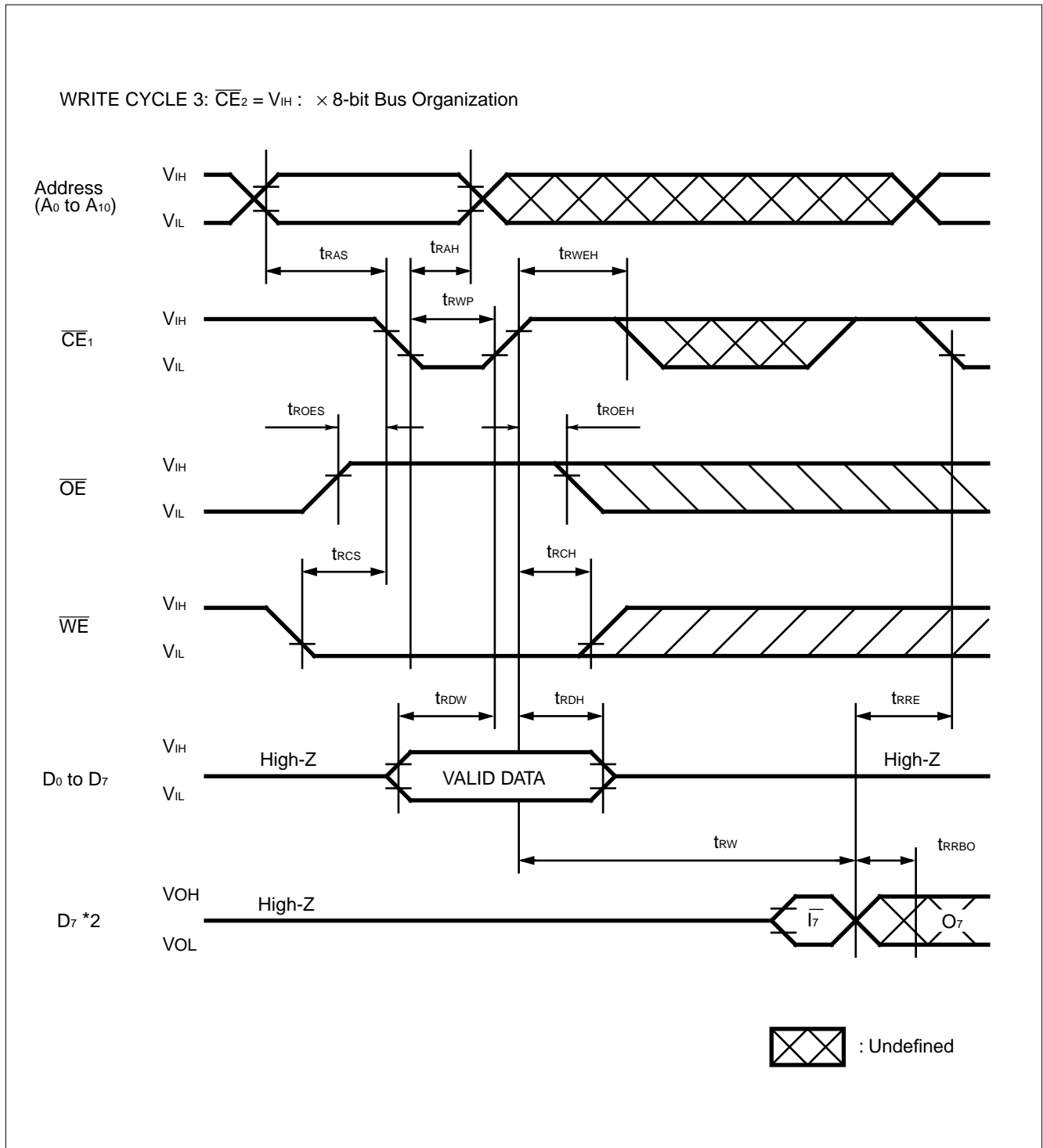
**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. Input levels of terminals  $D_8$  to  $D_{15}$  are not specified.

\*3. Data polling operation.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IL}$ ) \*1



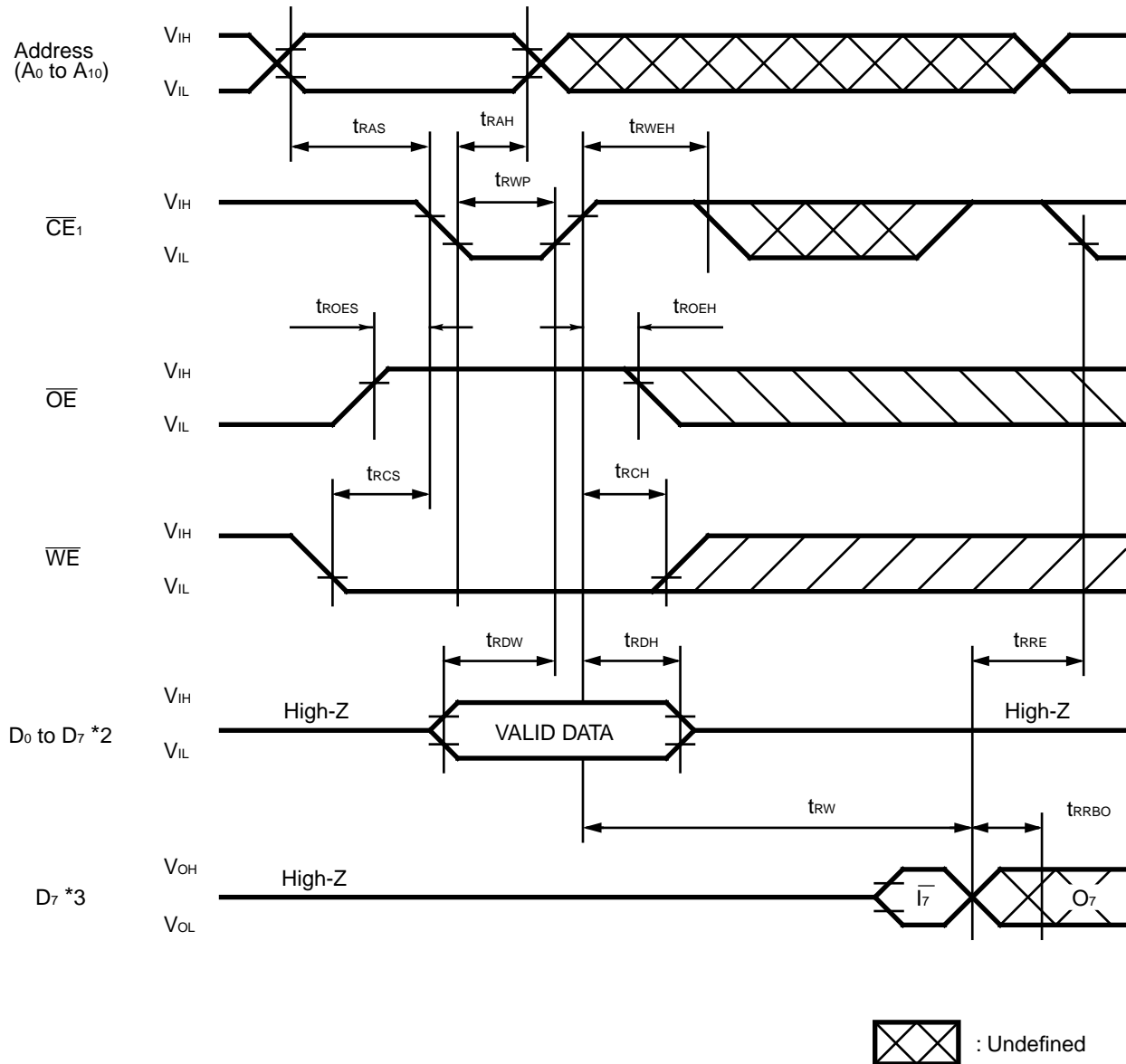
**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. Data polling operation.

# MB98A9083x/9093x/9103x/9113x-20

## ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IL}$ ) \*1

WRITE CYCLE 4:  $\overline{CE}_1 = \overline{CE}_2$ : × 16-bit Bus Organization



**Notes:** \*1. This timing diagram is for MB98A90833, 90933, 91033, and 91133. "FF" data is available on MB98A90832, 90932, 91032, and 91132 only.

\*2. Input levels of terminals D<sub>8</sub> to D<sub>15</sub> are not specified.

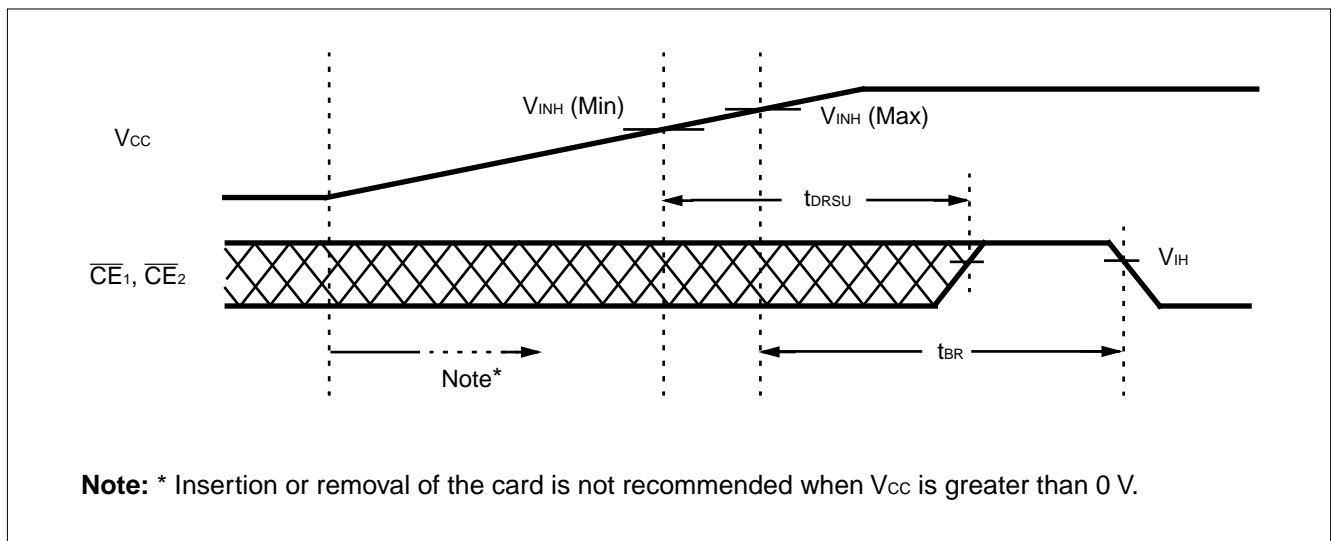
\*3. Data polling operation.

# MB98A9083x/9093x/9103x/9113x-20

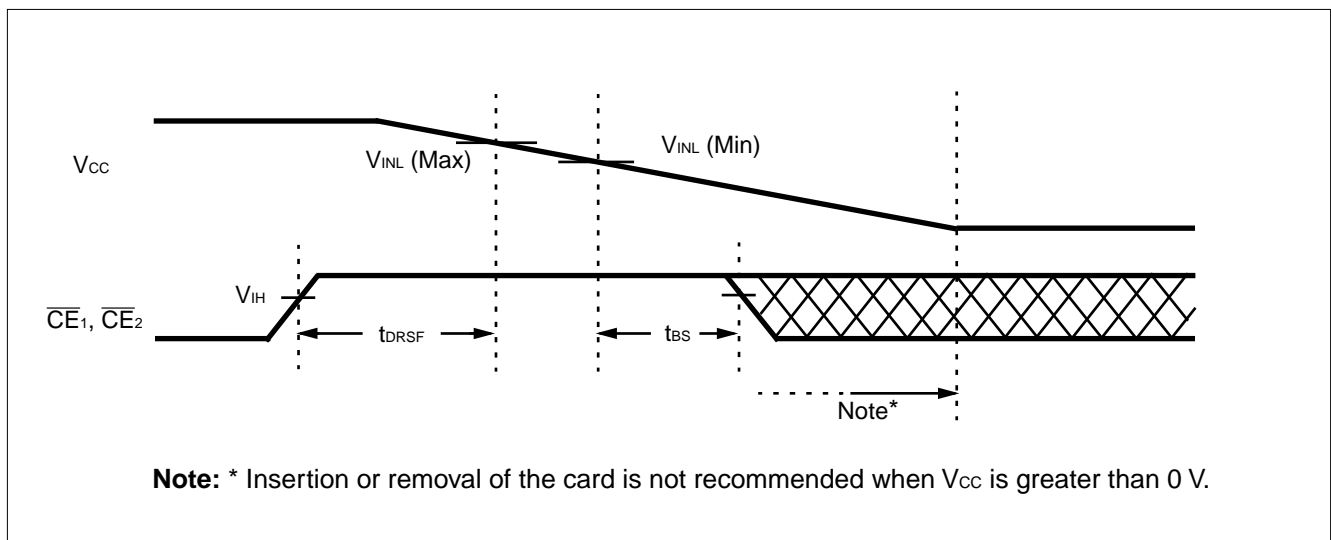
## ■ POWER SUPPLY SEQUENCE CHARACTERISTICS

| Parameter                    | Symbol     | Min. | Typ. | Max. | Unit    |
|------------------------------|------------|------|------|------|---------|
| Detection Rising Voltage     | $V_{INH}$  | 4.2  | 4.3  | 4.4  | V       |
| Detection Falling Voltage    | $V_{INL}$  | 4.1  | 4.2  | 4.3  | V       |
| Battery Backup Recovery Time | $t_{BR}$   | 3.0  | —    | —    | ms      |
| Data Retention Rising Time   | $t_{DRSU}$ | —    | —    | 0.5  | ms      |
| Battery Backup Set Up Time   | $t_{BS}$   | 10   | —    | —    | $\mu$ s |
| Data Retention Falling Time  | $t_{DRSF}$ | 0    | —    | —    | ns      |

### POWER-ON TIMING DIAGRAM



### POWER-OFF TIMING DIAGRAM



# MB98A9083x/9093x/9103x/9113x-20

## ■ UNIQUE FEATURES FOR SRAM CARD

### 1. REPLACEABLE BATTERIES FOR THE SRAM CARD

The battery used in the SRAM Card is a 3.0 V Lithium battery (coin type) with the following specifications:

|           |                         |
|-----------|-------------------------|
| Diameter  | : 20.0 (mm)             |
| Thickness | : 2.5 (mm)              |
| Weight    | : 2.5 (g) Approx.       |
| Type      | : CR2025, or equivalent |

### 2. APPROXIMATE DATA RETENTION TIME WITH BATTERY SUPPORT ONLY

| Part Number | Approx. Data Retention Time * ( $T_A = 20^\circ\text{C}$ ) |
|-------------|--|
| MB98A9083x  | 7 years min. 15 years typ.                                 |
| MB98A9093x  | 4 years min. 8 years typ.                                  |
| MB98A9103x  | 2 years min. 4 years typ.                                  |
| MB98A9113x  | 1 year min. 2 years typ.                                   |

\* Determined by the memory density of the card;  
i.e., greater card density means less battery time.

### 3. REPLACING THE BATTERY IN THE SRAM CARD

- Insert a slender pointed object, such as the end of a paper clip, into the hole on the upper side of the card. (See Fig. 4.)
- Release the battery holder by pressing the paper clip against the catch and pulling the battery holder straight out from the card. (The battery cavity is located at the top of the card. See Fig. 5.) When the battery holder is free from the card the battery will fall out.
- Replace the old battery with a fresh one. Be certain to match battery polarity to the + and – shown on the holder.
- Place the new battery into the holder, squeeze the holder containing the new battery tightly, and reinsert it into the battery cavity.

#### **WARNING**

Battery **MUST** be replaced within 30 minutes\* or data will be lost.

**Note:** \*With condition that the SRAM card had been inserted into application system more than 10 minutes.

Fig. 4 – SRAM CARD DRAWING (TOP VIEW)

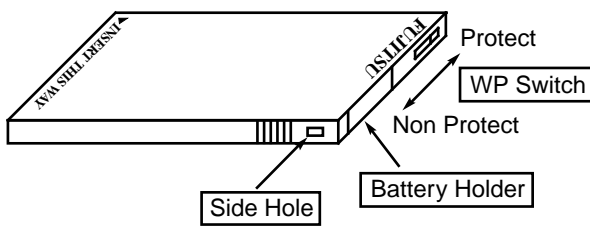
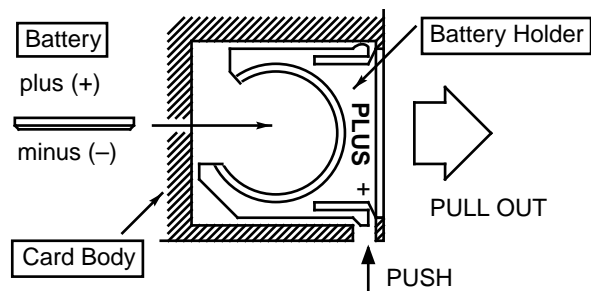


Fig.5 – BATTERY CASE DRAWING (TOP VIEW)



# MB98A9083x/9093x/9103x/9113x-20

## 4. SPECIAL MONITORING PINS

### 4.1 BVD1, BVD2: Voltage Monitoring Pins

These pins monitor the voltage of the battery which must be maintained at 2.65 V or greater for data retention. The condition of the battery is determined by reading the output signals on BVD1 and BVD2.

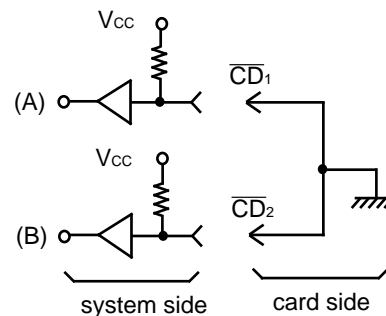
1. When  $BVD1=BVD2=V_{OH}$   
Battery voltage is sufficient to guarantee data retention; i.e., 2.65 V.
2. When  $BVD2=V_{OL}$ ,  $BVD1=V_{OH}$   
Battery voltage is lower than 2.65 V and should be replaced to safeguard data.
3. When  $BVD1=BVD2=V_{OL}$   
Battery voltage is less than 2.37 V: the level is dangerous. There is a possibility that data has not retained.

\*These functions operate over the Recommended Operating Conditions.

### 4.2 $\overline{CD}_1$ , $\overline{CD}_2$ : Card Detection Pins

These pins detect the insertion of the card into the system.  
(See Fig. 6.)

When the memory card has been correctly inserted,  $\overline{CD}_1$  and  $\overline{CD}_2$  are detected by the system.  $\overline{CD}_1$ ,  $\overline{CD}_2$  are tied to ground on the card side as shown in Fig. 6.



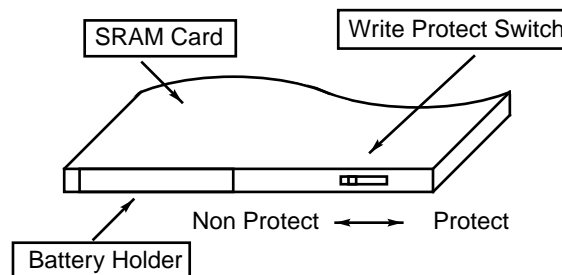
- Fig. 6 -

### 4.3 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 7, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the WE pin low. L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the "Protect" position. H-level is output on the WP pin.



- Fig. 7 -

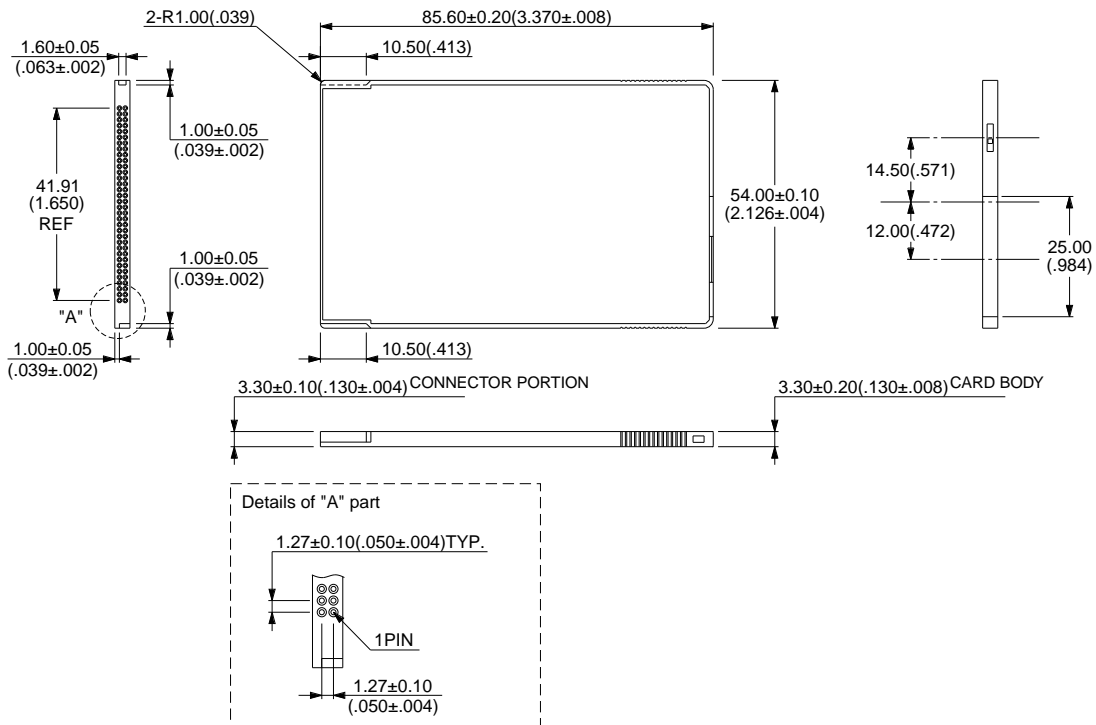
| WP Switch   | WP Pin |
|-------------|--------|
| Protect     | H      |
| Non Protect | L      |

# MB98A9083x/9093x/9103x/9113x-20

## ■ PACKAGE DIMENSIONS

68-PIN MEMORY CARD  
(CASE No.: CRD-68P-M04)

Note: Dimensions conform with PCMCIA/JEIDA. (PC CARD STANDARD 95)



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Dimensions in mm (inches)

## ■ DEVICE HANDLING PRECAUTIONS

This device is composed of fine electronic parts, so take care in handling or keeping it as below.

- The card is made fine, so do not keep it in the high temperature nor high humidity, place line in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken a part. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

# MB98A9083x/9093x/9103x/9113x-20

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