

MEMORY

FLASH MEMORY CARD PCMCIA Rel.2/JEIDA Ver.4 conformable

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

FLASH ERASABLE AND PROGRAMMABLE MEMORY CARD 512 K/1 M/2 M/4 M-BYTE

■ DESCRIPTION

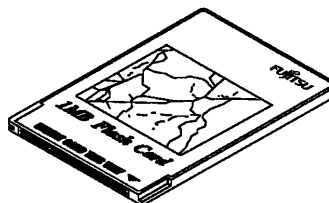
The Fujitsu MB98A809Bx, MB98A810Bx, MB98A811Bx and MB98A812Bx are Flash electrically erasable and programmable (Flash) memory cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, Flash memory cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is a Flash memory card option. (See page 3 for description of the three available options.)

- Credit card size: 85.6 mm (length) × 54.0 mm (width) × 3.3 mm (thick)
- PCMCIA/JEIDA conformed two-piece 68-pin connector (with a two-row built-in receptacle)
- Single +5.0 V $\pm 5\%$ power supply (+12.0 V $\pm 5\%$ V_{PP})
- Command control for Write/Erase operation
- Write protect function

■ PACKAGE



CRD-68P-M17

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■ ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the $\overline{\text{REG}}$ pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported.

REG Pin: Not Contacted

(JEIDA Ver.3 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|-------------|---------------------------|-------------|------------------|-------------|--------------------------------|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A809B1 | 2 M Flash Memory × 2 pcs | 250 ns | — | — | 512 K × 8 bits/256 K × 16 bits |
| MB98A810B1 | 2 M Flash Memory × 4 pcs | 250 ns | — | — | 1 M × 8 bits/512 K × 16 bits |
| MB98A811B1 | 2 M Flash Memory × 8 pcs | 250 ns | — | — | 2 M × 8 bits/1 M × 16 bits |
| MB98A812B1 | 2 M Flash Memory × 16 pcs | 250 ns | — | — | 4 M × 8 bits/2 M × 16 bits |

OPTION 2: Attribute memory in a separate location is not supported.

When $\overline{\text{REG}}$ line is asserted, “FF” is output to the data bus to indicate that attribute data may be stored in main memory.

(PCMCIA Rel.2/JEIDA Ver.4 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|-------------|---------------------------|-------------|------------------|-------------|--------------------------------|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A809B2 | 2 M Flash Memory × 2 pcs | 250 ns | — | — | 512 K × 8 bits/256 K × 16 bits |
| MB98A810B2 | 2 M Flash Memory × 4 pcs | 250 ns | — | — | 1 M × 8 bits/512 K × 16 bits |
| MB98A811B2 | 2 M Flash Memory × 8 pcs | 250 ns | — | — | 2 M × 8 bits/1 M × 16 bits |
| MB98A812B2 | 2 M Flash Memory × 16 pcs | 250 ns | — | — | 4 M × 8 bits/2 M × 16 bits |

OPTION 3: Attribute memory is supported. The data is stored in 16 K-bit EEPROM.

When the $\overline{\text{REG}}$ line is asserted, data stored in EEPROM is output to the data bus.

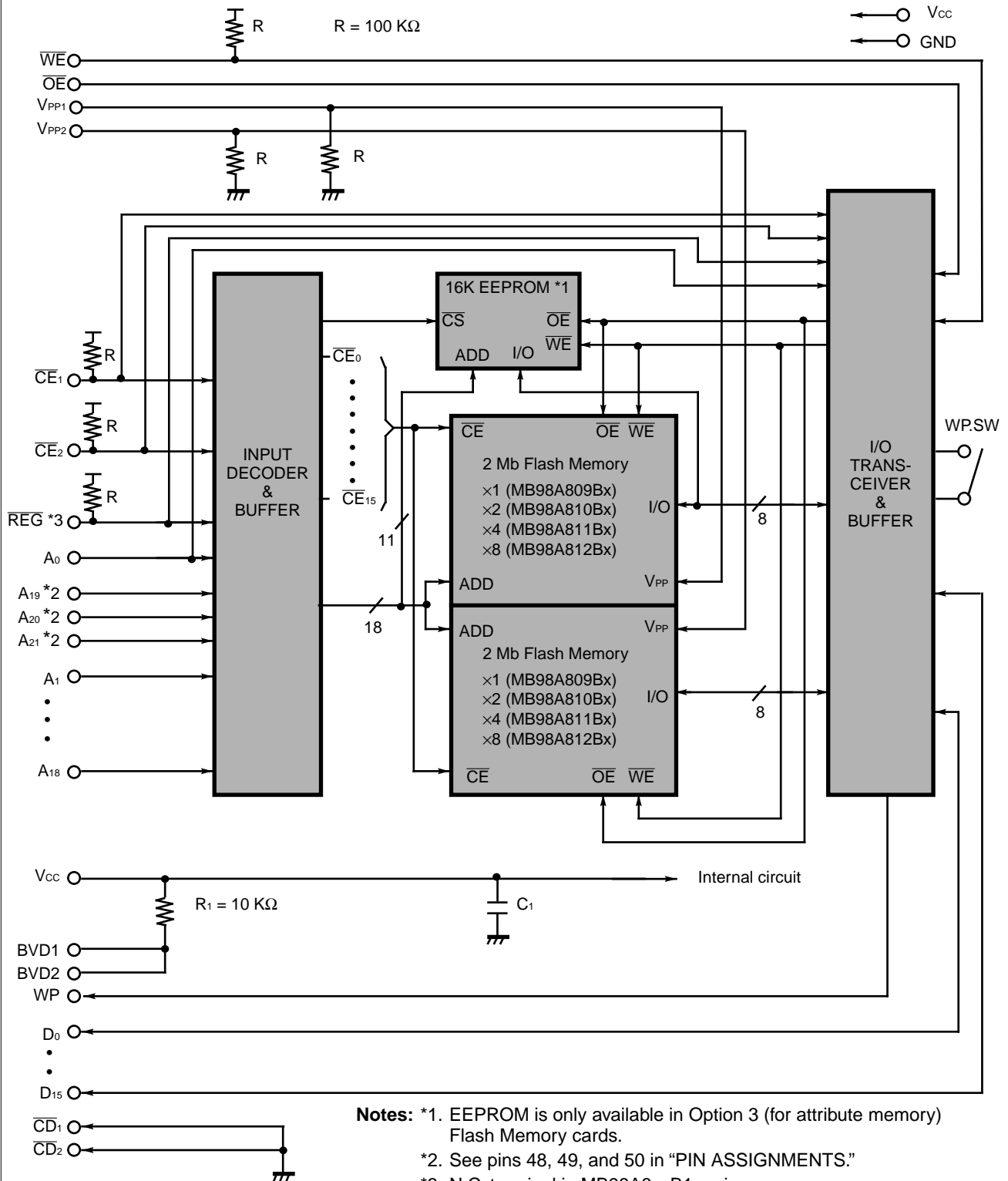
(PCMCIA Rel.2/JEIDA Ver.4 conformable)

| Part Number | Main Memory | | Attribute Memory | | Memory Organization * |
|-------------|---------------------------|-------------|------------------|-------------|--------------------------------|
| | Memory Device | Access Time | Memory Device | Access Time | |
| MB98A809B3 | 2 M Flash Memory × 2 pcs | 250 ns | EEPROM × 1 pcs | 300 ns | 512 K × 8 bits/256 K × 16 bits |
| MB98A810B3 | 2 M Flash Memory × 4 pcs | 250 ns | EEPROM × 1 pcs | 300 ns | 1 M × 8 bits/512 K × 16 bits |
| MB98A811B3 | 2 M Flash Memory × 8 pcs | 250 ns | EEPROM × 1 pcs | 300 ns | 2 M × 8 bits/1 M × 16 bits |
| MB98A812B3 | 2 M Flash Memory × 16 pcs | 250 ns | EEPROM × 1 pcs | 300 ns | 4 M × 8 bits/2 M × 16 bits |

* : To be configured by user.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

Fig. 1 – MB98A809Bx, 810Bx, 811Bx, and 812Bx BLOCK DIAGRAM



- Notes:**
- *1. EEPROM is only available in Option 3 (for attribute memory) Flash Memory cards.
 - *2. See pins 48, 49, and 50 in "PIN ASSIGNMENTS."
 - *3. N.C. terminal in MB98A8xxB1 series.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

■ PIN ASSIGNMENTS

| MB98A809Bx | MB98A810Bx | MB98A811Bx | MB98A812Bx | Pin No. | | MB98A809Bx | MB98A810Bx | MB98A811Bx | MB98A812Bx |
|-------------------|-------------------|-------------------|-------------------|---------|----|-------------------|-------------------|-------------------|-------------------|
| GND | GND | GND | GND | 1 | 35 | GND | GND | GND | GND |
| D ₃ | D ₃ | D ₃ | D ₃ | 2 | 36 | \overline{CD}_1 | \overline{CD}_1 | \overline{CD}_1 | \overline{CD}_1 |
| D ₄ | D ₄ | D ₄ | D ₄ | 3 | 37 | D ₁₁ | D ₁₁ | D ₁₁ | D ₁₁ |
| D ₅ | D ₅ | D ₅ | D ₅ | 4 | 38 | D ₁₂ | D ₁₂ | D ₁₂ | D ₁₂ |
| D ₆ | D ₆ | D ₆ | D ₆ | 5 | 39 | D ₁₃ | D ₁₃ | D ₁₃ | D ₁₃ |
| D ₇ | D ₇ | D ₇ | D ₇ | 6 | 40 | D ₁₄ | D ₁₄ | D ₁₄ | D ₁₄ |
| \overline{CE}_1 | \overline{CE}_1 | \overline{CE}_1 | \overline{CE}_1 | 7 | 41 | D ₁₅ | D ₁₅ | D ₁₅ | D ₁₅ |
| A ₁₀ | A ₁₀ | A ₁₀ | A ₁₀ | 8 | 42 | \overline{CE}_2 | \overline{CE}_2 | \overline{CE}_2 | \overline{CE}_2 |
| \overline{OE} | \overline{OE} | \overline{OE} | \overline{OE} | 9 | 43 | N.C. | N.C. | N.C. | N.C. |
| A ₁₁ | A ₁₁ | A ₁₁ | A ₁₁ | 10 | 44 | N.C. | N.C. | N.C. | N.C. |
| A ₉ | A ₉ | A ₉ | A ₉ | 11 | 45 | N.C. | N.C. | N.C. | N.C. |
| A ₈ | A ₈ | A ₈ | A ₈ | 12 | 46 | A ₁₇ | A ₁₇ | A ₁₇ | A ₁₇ |
| A ₁₃ | A ₁₃ | A ₁₃ | A ₁₃ | 13 | 47 | A ₁₈ | A ₁₈ | A ₁₈ | A ₁₈ |
| A ₁₄ | A ₁₄ | A ₁₄ | A ₁₄ | 14 | 48 | N.C. | A ₁₉ | A ₁₉ | A ₁₉ |
| \overline{WE} | \overline{WE} | \overline{WE} | \overline{WE} | 15 | 49 | N.C. | N.C. | A ₂₀ | A ₂₀ |
| N.C. | N.C. | N.C. | N.C. | 16 | 50 | N.C. | N.C. | N.C. | A ₂₁ |
| V _{CC} | V _{CC} | V _{CC} | V _{CC} | 17 | 51 | V _{CC} | V _{CC} | V _{CC} | V _{CC} |
| V _{PP1} | V _{PP1} | V _{PP1} | V _{PP1} | 18 | 52 | V _{PP2} | V _{PP2} | V _{PP2} | V _{PP2} |
| A ₁₆ | A ₁₆ | A ₁₆ | A ₁₆ | 19 | 53 | N.C. | N.C. | N.C. | N.C. |
| A ₁₅ | A ₁₅ | A ₁₅ | A ₁₅ | 20 | 54 | N.C. | N.C. | N.C. | N.C. |
| A ₁₂ | A ₁₂ | A ₁₂ | A ₁₂ | 21 | 55 | N.C. | N.C. | N.C. | N.C. |
| A ₇ | A ₇ | A ₇ | A ₇ | 22 | 56 | N.C. | N.C. | N.C. | N.C. |
| A ₆ | A ₆ | A ₆ | A ₆ | 23 | 57 | N.C. | N.C. | N.C. | N.C. |
| A ₅ | A ₅ | A ₅ | A ₅ | 24 | 58 | N.C. | N.C. | N.C. | N.C. |
| A ₄ | A ₄ | A ₄ | A ₄ | 25 | 59 | N.C. | N.C. | N.C. | N.C. |
| A ₃ | A ₃ | A ₃ | A ₃ | 26 | 60 | N.C. | N.C. | N.C. | N.C. |
| A ₂ | A ₂ | A ₂ | A ₂ | 27 | 61 | REG/N.C.* | REG/N.C.* | REG/N.C.* | REG/N.C.* |
| A ₁ | A ₁ | A ₁ | A ₁ | 28 | 62 | BVD2 | BVD2 | BVD2 | BVD2 |
| A ₀ | A ₀ | A ₀ | A ₀ | 29 | 63 | BVD1 | BVD1 | BVD1 | BVD1 |
| D ₀ | D ₀ | D ₀ | D ₀ | 30 | 64 | D ₈ | D ₈ | D ₈ | D ₈ |
| D ₁ | D ₁ | D ₁ | D ₁ | 31 | 65 | D ₉ | D ₉ | D ₉ | D ₉ |
| D ₂ | D ₂ | D ₂ | D ₂ | 32 | 66 | D ₁₀ | D ₁₀ | D ₁₀ | D ₁₀ |
| WP | WP | WP | WP | 33 | 67 | \overline{CD}_2 | \overline{CD}_2 | \overline{CD}_2 | \overline{CD}_2 |
| GND | GND | GND | GND | 34 | 68 | GND | GND | GND | GND |

* : N.C. terminal in MB98A8xxB1 series.

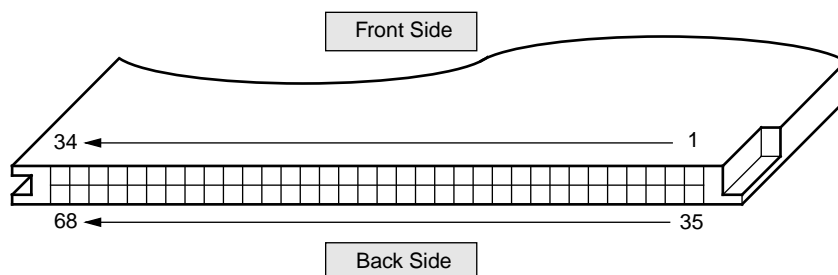
MB98A809Bx-/810Bx-/811Bx-/812Bx-25

■ PIN DESCRIPTIONS

| Symbol | Pin Name | Input/Output | Function |
|------------------------------------|----------------------------|--------------|--|
| A ₀ to A ₂₁ | Address Input | Input | Address Inputs, A ₀ to A ₂₁ . |
| D ₀ to D ₁₅ | Data Input/Output | Input/Output | Data Inputs/Outputs. This data bus size (8-bit or 16-bit) is selected with \overline{CE}_1 and \overline{CE}_2 . |
| \overline{CE}_1 | Card Enable for Lower Byte | Input | Active Low. - Lower byte (D ₀ to D ₇) is selected for read/write/erase function of flash memory cards. |
| \overline{CE}_2 | Card Enable for Upper Byte | Input | Active Low. - Upper byte (D ₈ to D ₁₅) is selected for read/write / erase function of flash memory cards. |
| \overline{REG} | Attribute Memory Select | Input | Active Low. - Attribute memory is selected for read/write function of identification data of flash memory cards. (N.C. or "FF" data or attribute data.) |
| \overline{OE} | Output Enable | Input | Active Low. - Output enable for flash memory cards. |
| \overline{WE} | Write Enable | Input | Active Low. - Write enable for flash memory cards. |
| V _{PP1} | Programming Voltage 1 | Input | Programming voltage for lower byte. |
| V _{PP2} | Programming Voltage 2 | Input | Programming voltage for upper byte. |
| $\overline{CD}_1, \overline{CD}_2$ | Card Detect | Output | These pins detect if the card has been correctly inserted. Both pins are tied to GND internally. |
| WP | Write Protect | Output | Write controller for flash memory cards. This pin outputs the Protect/Non Protect status of "WP Switch". |
| BVD1, BVD2 | Battery Voltage Detect | Output | Both pins are tied to V _{CC} internally. |
| V _{CC} | Power Supply | — | Power Supply Voltage. (+5.0 V ±5%) |
| GND | Ground | — | System Ground. |
| N.C. | Non Connection | — | |

■ PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



MB98A809Bx-/810Bx-/811Bx-/812Bx-25

FUNCTIONAL TRUTH TABLE

MAIN MEMORY FUNCTION *1

Read Function ($\overline{REG} = V_{IH}$)

| \overline{CE}_2 | \overline{CE}_1 | A ₀ | \overline{OE} | \overline{WE} | WP *2 | V _{PP2} | V _{PP1} | Mode | Data Input/Output | | WP SW |
|-------------------|-------------------|----------------|-----------------|-----------------|-------|------------------|------------------|----------------|-----------------------------------|----------------------------------|---------|
| | | | | | | | | | D ₈ to D ₁₅ | D ₀ to D ₇ | |
| H | H | X | X | X | X | V _{PPL} | V _{PPL} | Standby | High-Z | | P or NP |
| H | L | L | L | H | X | V _{PPL} | V _{PPL} | Read (×8) | High-Z | D _{OUT} (Lower Byte) | P or NP |
| H | L | H | L | H | X | V _{PPL} | V _{PPL} | Read (×8) | High-Z | D _{OUT} (Upper Byte) | P or NP |
| L | H | X | L | H | X | V _{PPL} | V _{PPL} | Read (×8) | D _{OUT} (Upper Byte) | High-Z | P or NP |
| L | L | X | L | H | X | V _{PPL} | V _{PPL} | Read (×16) | D _{OUT} | | P or NP |
| X | X | X | H | H | X | V _{PPL} | V _{PPL} | Output Disable | High-Z | | P or NP |

Erase/Write/Verify Function ($\overline{REG} = V_{IH}$)

| \overline{CE}_2 | \overline{CE}_1 | A ₀ | \overline{OE} | \overline{WE} | WP *2 | V _{PP2} | V _{PP1} | Mode | Data Input/Output | | WP SW |
|-------------------|-------------------|----------------|-----------------|-----------------|-------|---------------------|---------------------|----------------|-----------------------------------|----------------------------------|---------|
| | | | | | | | | | D ₈ to D ₁₅ | D ₀ to D ₇ | |
| H | H | X | X | X | X | V _{PPH} | V _{PPH} | Standby | High-Z | | P or NP |
| H | L | L | L | H | L | V _{PPL} *3 | V _{PPH} | Read (×8) | High-Z | D _{OUT} | NP |
| H | L | H | L | H | L | V _{PPH} | V _{PPL} *3 | Read (×8) | High-Z | D _{OUT} | NP |
| H | L | L | H | L | L | V _{PPL} *3 | V _{PPH} | Write (×8) | High-Z | D _{IN} | NP |
| H | L | H | H | L | L | V _{PPH} | V _{PPL} *3 | Write (×8) | High-Z | D _{IN} | NP |
| L | H | X | L | H | L | V _{PPH} | V _{PPL} *3 | Read (×8) | D _{OUT} | High-Z | NP |
| L | H | X | H | L | L | V _{PPH} | V _{PPL} *3 | Write (×8) | D _{IN} | High-Z | NP |
| L | L | X | L | H | L | V _{PPH} | V _{PPH} | Read (×16) | D _{OUT} | | NP |
| L | L | X | H | L | L | V _{PPH} | V _{PPH} | Write (×16) | D _{IN} | | NP |
| X | X | X | H | H | L | V _{PPH} | V _{PPH} | Output Disable | High-Z | | NP |

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}, WP SW = Write Protect Switch, P = Protect, NP = Non Protect

*2. L-level is output when WPSW = NP. H-level is output when WPSW = P.

*3. V_{PPL} is recommended though it is functionable at V_{PPH}.

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ATTRIBUTE MEMORY FUNCTION *1 ($\overline{\text{REG}} = V_{\text{IL}}$) *2

| $\overline{\text{CE}}_2$ | $\overline{\text{CE}}_1$ | A_0 | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | WP | Mode | Data Input/Output | | WP SW |
|--------------------------|--------------------------|-------|------------------------|------------------------|----|----------------|-----------------------------------|-------------------------------------|-------|
| | | | | | | | D ₁₅ to D ₈ | D ₇ to D ₀ | |
| H | H | X | X | X | L | Standby | High-Z | | NP |
| H | L | L | L | H | L | Read (×8) | High-Z | D _{OUT} *3 (Lower Byte) | NP |
| H | L | H | L | H | L | Read (×8) | High-Z | H | NP |
| H | L | L | H | L | L | Write (×8) | High-Z | D _{IN} (Lower Byte) | NP |
| H | L | H | H | L | L | Write (×8) | High-Z | X | NP |
| L | H | X | L | H | L | Read (×8) | H | High-Z | NP |
| L | H | X | H | L | L | Write (×8) | High-Z | High-Z | NP |
| L | L | X | L | H | L | Read (×16) | H | D _{OUT} *3 (Lower Byte) | NP |
| L | L | X | H | L | L | Write (×16) | X | D _{IN} (Lower Byte) | NP |
| X | X | X | H | H | L | Output Disable | High-Z | | NP |

| | | | | | | | | | |
|---|---|---|---|---|---|----------------|--------|-------------------------------------|---|
| H | H | X | X | X | H | Standby | High-Z | | P |
| H | L | L | L | H | H | Read (×8) | High-Z | D _{OUT} *3 (Lower Byte) | P |
| H | L | H | L | H | H | Read (×8) | High-Z | H | P |
| H | L | L | H | L | H | Output Disable | High-Z | | P |
| H | L | H | H | L | H | Output Disable | High-Z | | P |
| L | H | X | L | H | H | Read (×8) | H | High-Z | P |
| L | H | X | H | L | H | Output Disable | High-Z | | P |
| L | L | X | L | H | H | Read (×16) | H | D _{OUT} *3 (Lower Byte) | P |
| L | L | X | H | L | H | Output Disable | High-Z | | P |
| X | X | X | H | H | H | Output Disable | High-Z | | P |

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}, WP SW = Write Protect Switch, P = Protect, NP = Non Protect

*2. N.C. for MB98A809B1, 810B1, 811B1, and 812B1.

*3. H-level is output for MB98A809B2, 810B2, 811B2, and 812B2.

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■ WRITE/ERASE CHIP DECODING INFORMATION

| Bus Organization | \overline{CE}_2 | \overline{CE}_1 | A ₂₀ | A ₁₉ | A ₁₈ | A ₀ | Decode Chips | | | | |
|------------------|-------------------|-------------------|-----------------|-----------------|-----------------|----------------|----------------|---|------------------|---------|---------|
| 8-bit Bus | H | L | L | L | L | L | Chip 0 | | | | |
| | | | | | H | H | Chip 1 | | | | |
| | | | | | L | L | Chip 2 | | | | |
| | | | | H | H | Chip 3 | | | | | |
| | | | | L | L | Chip 4 | | | | | |
| | | | | H | H | Chip 5 | | | | | |
| | | | H | L | L | L | L | L | Chip 6 | | |
| | | | | | | | H | H | Chip 7 | | |
| | | | | | | | L | L | Chip 8 | | |
| | | | | H | L | L | L | H | H | Chip 9 | |
| | | | | | | | | L | L | Chip 10 | |
| | | | | | | | | H | H | Chip 11 | |
| | | | | | H | L | L | L | L | L | Chip 12 |
| | | | | | | | | | H | H | Chip 13 |
| | | | | | | | | | L | L | Chip 14 |
| | L | H | L | L | L | L | Chip 15 | | | | |
| | | | | | H | H | Chip 1 | | | | |
| | | | | | L | L | Chip 3 | | | | |
| | | | | H | L | L | H | H | Chip 5 | | |
| | | | | | | | L | L | Chip 7 | | |
| | | | | | | | H | H | Chip 9 | | |
| | | | H | L | L | L | L | L | Chip 11 | | |
| | | | | | | | H | H | Chip 13 | | |
| | | | | | | | L | L | Chip 15 | | |
| 16-bit Bus | L | L | L | L | L | X | Chip 0, Chip 1 | | | | |
| | | | | | H | | Chip 2, Chip 3 | | | | |
| | | | | | L | | Chip 4, Chip 5 | | | | |
| | | | | H | L | | L | H | Chip 6, Chip 7 | | |
| | | | | | | | | L | Chip 8, Chip 9 | | |
| | | | | | | | | H | Chip 10, Chip 11 | | |
| | | | H | L | L | | L | L | Chip 12, Chip 13 | | |
| | | | | | | | | H | Chip 14, Chip 15 | | |
| | | | | | | | | L | | | |

Note: H = V_{IH}, L = V_{IL}, X = Either V_{IH} or V_{IL}

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■ COMMAND DEFINITION TABLE

Command Table for 8-bit Mode

| Command | Bus Cycle Required | First Bus Cycle | | | Second Bus Cycle | | |
|------------------------------|--------------------|-----------------|------------|---------|------------------|------------|---------|
| | | Operation *1 | Address *2 | Data *3 | Operation *1 | Address *2 | Data *3 |
| Read Memory | 1 | Write | RA | 00H | — | — | — |
| Read Intelligent ID Codes *4 | 3 | Write | IA | 90H | Read | — | — |
| Set Up Erase/Erase *5 | 2 | Write | ZA | 20H | Write | ZA | 20H |
| Erase Verify *5 | 2 | Write | EA | A0H | Read | EA | EVD |
| Set Up Write/Write *6 | 2 | Write | WA | 40H | Write | WA | WD |
| Write Verify *6 | 2 | Write | WA | C0H | Read | WA | WVD |
| Reset *7 *8 | 2 | Write | ZA | FFH | Write | ZA | FFH |

Command Table for 16-bit Mode

| Command | Bus Cycle Required | First Bus Cycle | | | Second Bus Cycle | | |
|------------------------------|--------------------|-----------------|------------|---------|------------------|------------|---------|
| | | Operation *1 | Address *2 | Data *3 | Operation *1 | Address *2 | Data *3 |
| Read Memory | 1 | Write | RA | 0000H | — | — | — |
| Read Intelligent ID Codes *4 | 3 | Write | IA | 9090H | Read | — | — |
| Set Up Erase/Erase *5 | 2 | Write | ZA | 2020H | Write | ZA | 2020H |
| Erase Verify *5 | 2 | Write | EA | A0A0H | Read | EA | EVD |
| Set Up Write/Write *6 | 2 | Write | WA | 4040H | Write | WA | WD |
| Write Verify *6 | 2 | Write | WA | C0C0H | Read | WA | WVD |
| Reset *7 *8 | 2 | Write | ZA | FFFFH | Write | ZA | FFFFH |

Notes: *1. Bus operations are defined in "FUNCTIONAL TRUTH TABLE".

*2. IA = Identifier address: 00H for manufacturer code, 01H for device code.

EA = Address of memory location to be read during erase verify.

RA = Read Address

WA = Address of memory location to be written.

ZA = Address of 256 K-Byte zones involved in erase operation.

Addresses are latched on the falling edge of the Write Enable pulse.

*3. ID = Data read from location IA during device identification.

Manufacturer = 31H for 8-bit, 3131H for 16-bit/Device = BDH for 8-bit, BDBDH for 16-bit

EVD = Data read from location EA during erase verify.

WD = Data to be programmed at location WA. Data is latched on the rising edge of Write Enable.

WVD = Data read from location WA during write verify. WA is latched on the Write command.

*4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.

*5. "ERASE FLOWCHART" in Fig.6, Fig.7 and Fig.8 illustrate the Erase Algorithm.

*6. "WRITE FLOWCHART" in Fig.4 and Fig.5 illustrate the Write Algorithm.

*7. The second bus cycle must be followed by the desired command register write.

*8. The Reset command operates on a zone basis. To reset the entire card requires reset write cycles to each zone.

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■ ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

8-BIT BUS ORGANIZATION ($\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IH}$)

| A ₂₁ to A ₀ | | | | | | \overline{CE}_2 | \overline{CE}_1 | D ₁₅ to D ₈ | D ₇ to D ₀ |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 00 | 0000 | 0000 | 0000 | 0000 | 0000 | H | L | ----- | 0 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 0001 | H | L | ----- | 1 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 0010 | H | L | ----- | 2 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 0011 | H | L | ----- | 3 Add. |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 11 | 1111 | 1111 | 1111 | 1111 | 1100 | H | L | ----- | 4,194,300 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 1101 | H | L | ----- | 4,194,301 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 1110 | H | L | ----- | 4,194,302 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 1111 | H | L | ----- | 4,194,303 Add. |

8-BIT BUS ORGANIZATION ($\overline{CE}_1 = V_{IH}$, $\overline{CE}_2 = V_{IL}$) *2

| A ₂₁ to A ₀ | | | | | | \overline{CE}_2 | \overline{CE}_1 | D ₁₅ to D ₈ | D ₇ to D ₀ |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 00 | 0000 | 0000 | 0000 | 0000 | 000X | L | H | 1 Add. | ----- |
| 00 | 0000 | 0000 | 0000 | 0000 | 001X | L | H | 3 Add. | ----- |
| 00 | 0000 | 0000 | 0000 | 0000 | 010X | L | H | 5 Add. | ----- |
| 00 | 0000 | 0000 | 0000 | 0000 | 011X | L | H | 7 Add. | ----- |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 11 | 1111 | 1111 | 1111 | 1111 | 100X | L | H | 4,194,297 Add. | ----- |
| 11 | 1111 | 1111 | 1111 | 1111 | 101X | L | H | 4,194,299 Add. | ----- |
| 11 | 1111 | 1111 | 1111 | 1111 | 110X | L | H | 4,194,301 Add. | ----- |
| 11 | 1111 | 1111 | 1111 | 1111 | 111X | L | H | 4,194,303 Add. | ----- |

16-BIT BUS ORGANIZATION ($\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IL}$)

| A ₂₁ to A ₀ | | | | | | \overline{CE}_2 | \overline{CE}_1 | D ₁₅ to D ₈ | D ₇ to D ₀ |
|-----------------------------------|------|------|------|------|------|-------------------|-------------------|-----------------------------------|----------------------------------|
| 00 | 0000 | 0000 | 0000 | 0000 | 000X | L | L | 1 Add. | 0 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 001X | L | L | 3 Add. | 2 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 010X | L | L | 5 Add. | 4 Add. |
| 00 | 0000 | 0000 | 0000 | 0000 | 011X | L | L | 7 Add. | 6 Add. |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ | ↓ ↓ | ↓ ↓ |
| 11 | 1111 | 1111 | 1111 | 1111 | 100X | L | L | 4,194,297 Add. | 4,194,296 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 101X | L | L | 4,194,299 Add. | 4,194,298 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 110X | L | L | 4,194,301 Add. | 4,194,300 Add. |
| 11 | 1111 | 1111 | 1111 | 1111 | 111X | L | L | 4,194,303 Add. | 4,194,302 Add. |

Notes: *1. H = V_{IH}, L = V_{IL}, X = Either 0 or 1.

*2. Even addresses are not available in this mode.

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■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Note | Symbol | Value | Unit |
|---|------|--------------------|------------------------|------|
| Supply Voltage | | V_{CC} | -0.5 to +6.0 | V |
| Input Voltage | | V_{IN} | -0.5 to $V_{CC} + 0.5$ | V |
| Output Voltage | | V_{OUT} | -0.5 to $V_{CC} + 0.5$ | V |
| Programming Voltage | *1 | V_{PP1}, V_{PP2} | -2.0 to +14.0 | V |
| Storage Temperature at turning on the power | | T_{BIAS} | -10 to 70 | °C |
| Ambient Temperature | | T_A | 0 to +60 | °C |
| Storage Temperature | | T_{STG} | -30 to +70 | °C |

Note: *1. Minimum DC input voltage is -0.5 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------|----------|------|------|------|------|
| V_{CC} Supply Voltage | V_{CC} | 4.75 | 5.0 | 5.25 | V |
| Ground | GND | — | 0 | — | V |
| Ambient Temperature | T_A | 0 | — | +55 | °C |

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{\text{IN}} = V_{\text{I/O}} = \text{GND}$)

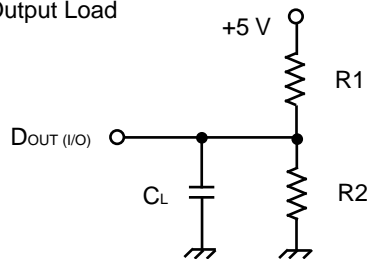
| Parameter | Notes | Symbol | Min. | Max. | Unit |
|-------------------|-------|------------------|------|------|------|
| Input Capacitance | *1 | C_{IN} | — | 50 | pF |
| I/O Capacitance | *2 | $C_{\text{I/O}}$ | — | 50 | pF |

Notes: *1. This value does not apply to $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, $\overline{\text{WE}}$ and $\overline{\text{REG}}$.

*2. This value does not apply to $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$, BVD1 and BVD2.

Fig. 3 – AC TEST CONDITIONS

• Output Load



- Input Pulse Levels: 0.6 V to 2.6 V
 - Input Pulse Rise and Fall Times: 5 ns (Transient between 0.8 V and 2.4 V)
 - Timing Reference Levels
Input: $V_{\text{IL}} = 0.8\text{ V}$, $V_{\text{IH}} = 2.4\text{ V}$
Output: $V_{\text{OL}} = 0.8\text{ V}$, $V_{\text{OH}} = 2.0\text{ V}$
- * Including jig and stray capacitance

| | R1 | R2 | CL | Parameter Measured |
|---------|----------------|--------------|--------|---|
| Load I | 1.8 k Ω | 990 Ω | 100 pF | All parameters except t_{CLZ} , t_{OLZ} , t_{EHQZ} , t_{DF} , t_{RCLZ} , t_{ROLZ} , t_{RCHZ} and t_{ROHZ} |
| Load II | 1.8 k Ω | 990 Ω | 5 pF | t_{CLZ} , t_{OLZ} , t_{EHQZ} , t_{DF} , t_{RCLZ} , t_{ROLZ} , t_{RCHZ} and t_{ROHZ} |

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

■ DC CHARACTERISTICS

| Parameter | Notes | Symbol | Condition | Value | | | Unit |
|--|-------|-----------|--|-------|-----------|----------------|---------|
| | | | | Min. | Typ. | Max. | |
| Input Leakage Current | *1 | I_{LI} | $V_{CC} = V_{CC\ max}$ $V_{IN} = 0\ V\ or\ V_{CC}$ | — | ± 1.0 | ± 20 | μA |
| Output Leakage Current | *2 | I_{LO} | $V_{CC} = V_{CC\ max}$ $V_{IN} = 0\ V\ or\ V_{CC}$ | — | ± 1.0 | ± 20 | μA |
| V_{CC} Standby Current | | I_{SB1} | $V_{CC} = V_{CC\ max}$ $\overline{CE}_1 = \overline{CE}_2 = V_{CC} - 0.2\ V$ | — | 0.9 | 1.7 | mA |
| | | I_{SB2} | $V_{CC} = V_{CC\ max}$ $\overline{CE}_1 = \overline{CE}_2 = V_{IH}$ | — | 7.0 | 140. | mA |
| V_{CC} Active Read Current | | I_{CC1} | $V_{CC} = V_{CC\ max}$ $\overline{CE}_1 = \overline{CE}_2 = V_{IL}$ cyc. = 250 ns, $I_{OUT} = 0\ mA$ | — | 70 | 100 | mA |
| V_{CC} Write Current | | I_{CC2} | Write in progress | — | 2.0 | 20 | mA |
| V_{CC} Erase Current | | I_{CC3} | Erase in progress | — | 10 | 30 | mA |
| V_{PP} Leakage Current | *3 | I_{PPS} | $V_{PP} \leq V_{CC}$ | — | — | 250 | μA |
| V_{PP} Read Current or Standby Current | *3 | I_{PP1} | $V_{PP} > V_{CC}$ | — | 0.9 | 1.8 | mA |
| | | | $V_{PP} \leq V_{CC}$ | — | — | 250 | mA |
| V_{PP} Write Current | *3 | I_{PP2} | $V_{PP} = V_{PPH}$ Write in progress | — | 9 | 30 | mA |
| V_{PP} Erase Current | *3 | I_{PP3} | $V_{PP} = V_{PPH}$ Erase in progress | — | 7 | 30 | mA |
| Input Low Voltage | | V_{IL} | — | -0.3 | — | 0.8 | V |
| Input High Voltage | | V_{IH} | — | 2.4 | — | $V_{CC} + 0.3$ | V |
| Output Low Voltage | | V_{OL} | $I_{OL} = 3.2\ mA$, $V_{CC} = V_{CC\ min}$ | — | — | 0.4 | V |
| Output High Voltage | *4 | V_{OH} | $I_{OH} = -2.0\ mA$, $V_{CC} = V_{CC\ min}$ | 3.8 | — | — | V |
| V_{PP} during Read-Only Operation | *5 | V_{PPL} | — | 0 | — | 6.5 | V |
| V_{PP} during Write/Erase Operation | | V_{PPH} | — | 11.4 | — | 12.6 | V |

Notes: *1. This value does not apply to \overline{CE}_1 , \overline{CE}_2 , \overline{WE} and \overline{REG} .

*2. This value does not apply to BVD1, BVD2, \overline{CD}_1 and \overline{CD}_2 .

*3. This value apply to V_{PP1} and V_{PP2} .

*4. This value does not apply to BVD1 and BVD2.

*5. Write/Erase are inhibited when $V_{PP} = V_{PPL}$.

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■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE *1

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---|-------|-------------------|------|------|------|
| Read Cycle Time | | t _{RC} | 250 | — | ns |
| Card Enable Access Time | | t _{CE} | — | 250 | ns |
| Address Access Time | | t _{ACC} | — | 250 | ns |
| Output Enable Access Time | | t _{OE} | — | 120 | ns |
| Card Enable to Output in Low-Z | *2 | t _{CLZ} | 5 | — | ns |
| Card Disable to Output in High-Z | *2 | t _{EHQZ} | — | 60 | ns |
| Output Enable to Output in Low-Z | *2 | t _{OLZ} | 5 | — | ns |
| Output Disable to Output in High-Z | *2 | t _{DF} | — | 60 | ns |
| Output Hold from Address, \overline{CE} , or \overline{OE} Change | *3 | t _{OH} | 5 | — | ns |

ATTRIBUTE MEMORY READ CYCLE *1*4

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|---------------------------------|-------|-------------------|------|------|------|
| Read Cycle Time | | t _{RRC} | 300 | — | ns |
| Address Access Time | | t _{RAA} | — | 300 | ns |
| Card Enable Access Time | | t _{RCE} | — | 300 | ns |
| Output Enable Access Time | | t _{ROE} | — | 150 | ns |
| Output Hold from Address Change | | t _{ROH} | 5 | — | ns |
| Card Enable to Output Low-Z | *2 | t _{RCLZ} | 5 | — | ns |
| Output Enable to Output Low-Z | *2 | t _{ROLZ} | 5 | — | ns |
| Card Enable to Output High-Z | *2 | t _{RCHZ} | — | 60 | ns |
| Output Enable to Output High-Z | *2 | t _{ROHZ} | — | 60 | ns |

Notes: *1. Rise/Fall time < 5 ns.

*2. Transition is measured at the point of ± 500 mV from steady state voltage. This parameter is specified using Load II in Fig.3.

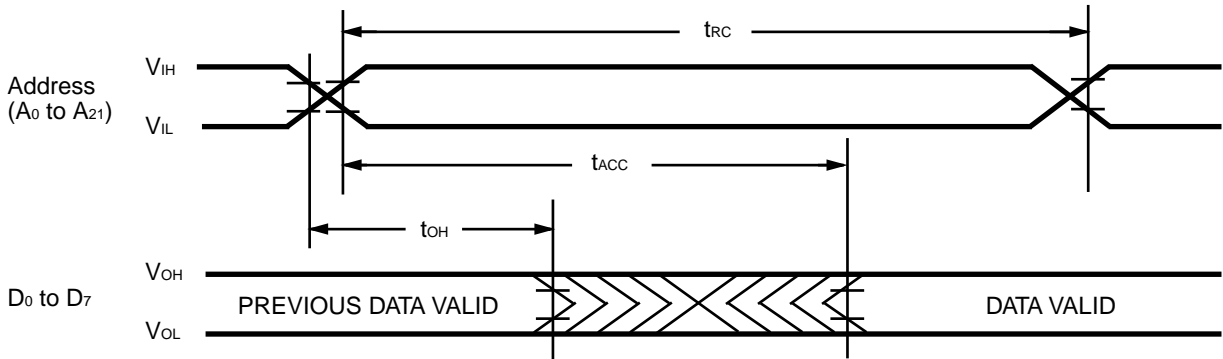
*3. This parameter is specified from the rising edge of \overline{OE} , \overline{CE}_1 and \overline{CE}_2 , whichever occurs first.

*4. This parameter is for MB98A809B3, 810B3, 811B3, and 812B3.

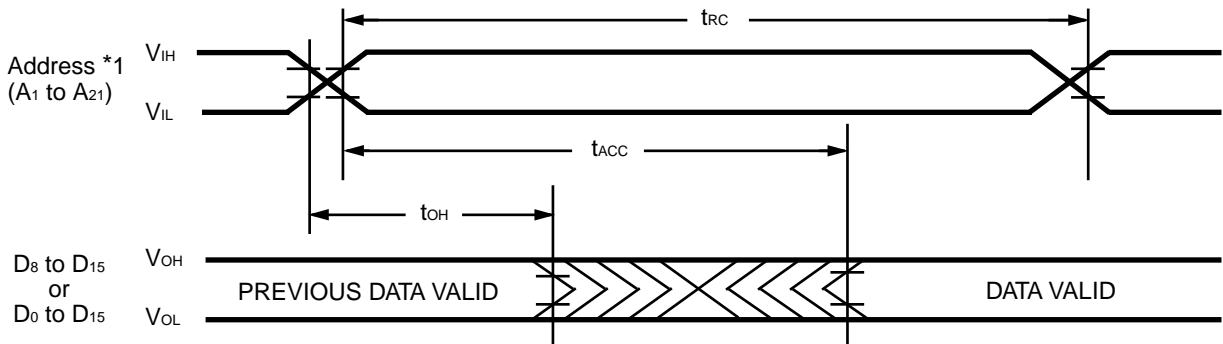
MB98A809Bx-/810Bx-/811Bx-/812Bx-25


MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IH}$)

READ CYCLE 1: $\overline{CE}_1 = \overline{OE} = V_{IL}$, $\overline{CE}_2 = V_{IH}$: × 8-bit Bus Organization



READ CYCLE 2: $\overline{CE}_1 = V_{IH}$, $\overline{CE}_2 = \overline{OE} = V_{IL}$: × 8-bit Bus Organization
 $\overline{CE}_1 = \overline{CE}_2 = \overline{OE} = V_{IL}$: × 16-bit Bus Organization



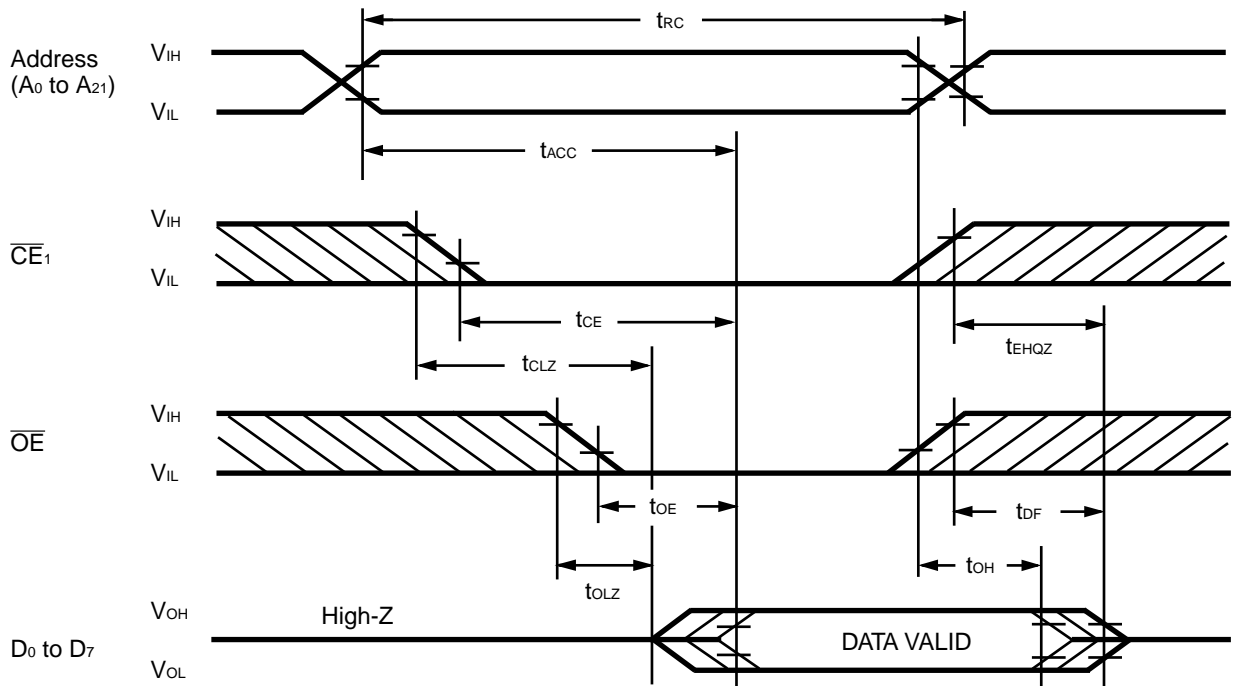
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Note: *1. A₀ = Either V_{IH} or V_{IL}.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IH}$)

READ CYCLE 3: $\overline{CE}_2 = V_{IH}$: × 8-bit Bus Organization

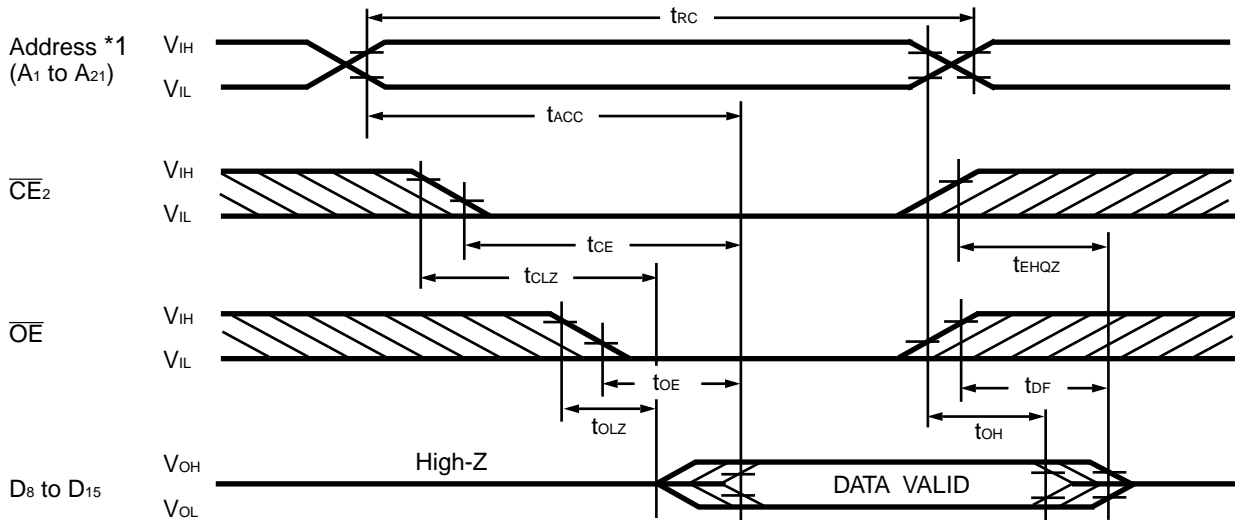


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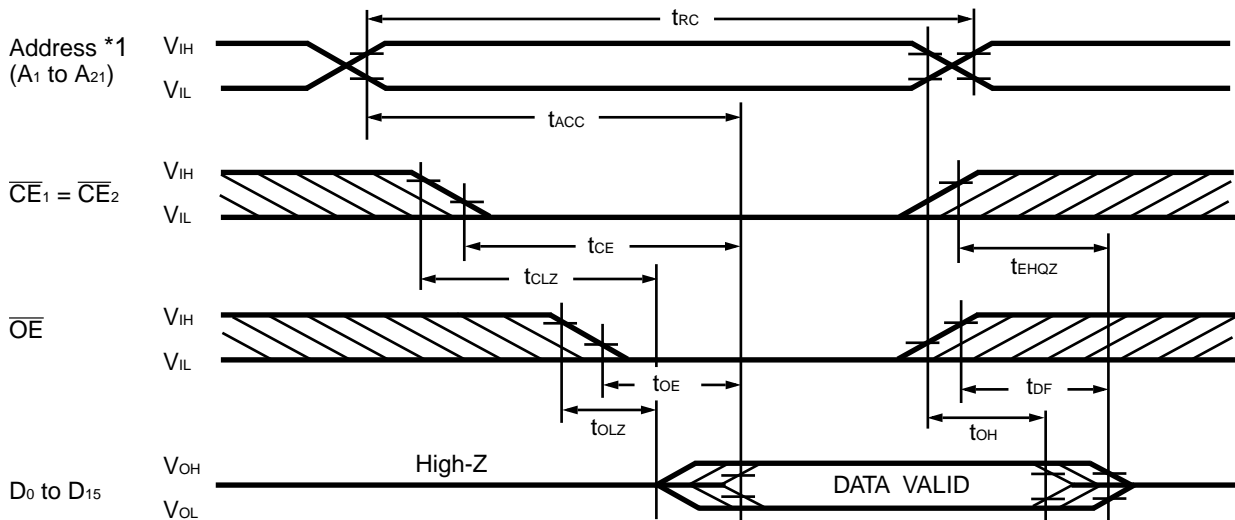
MB98A809Bx-/810Bx-/811Bx-/812Bx-25


MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IH}$)

READ CYCLE 4: $\overline{CE}_1 = V_{IH}$: × 8-bit Bus Organization



READ CYCLE 5: $\overline{CE}_1 = \overline{CE}_2 = V_{IL}$: × 16-bit Bus Organization



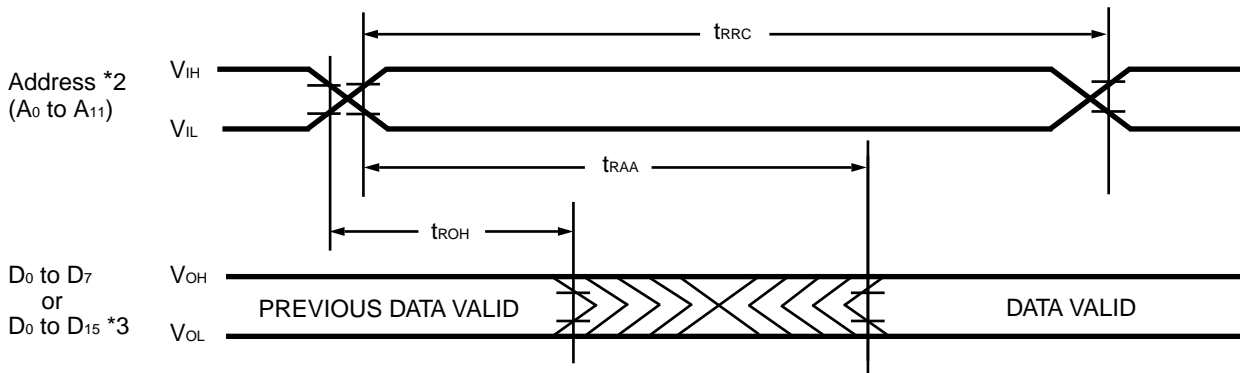
 : Undefined

Note: *1. $A_0 =$ Either V_{IL} or V_{IH} .

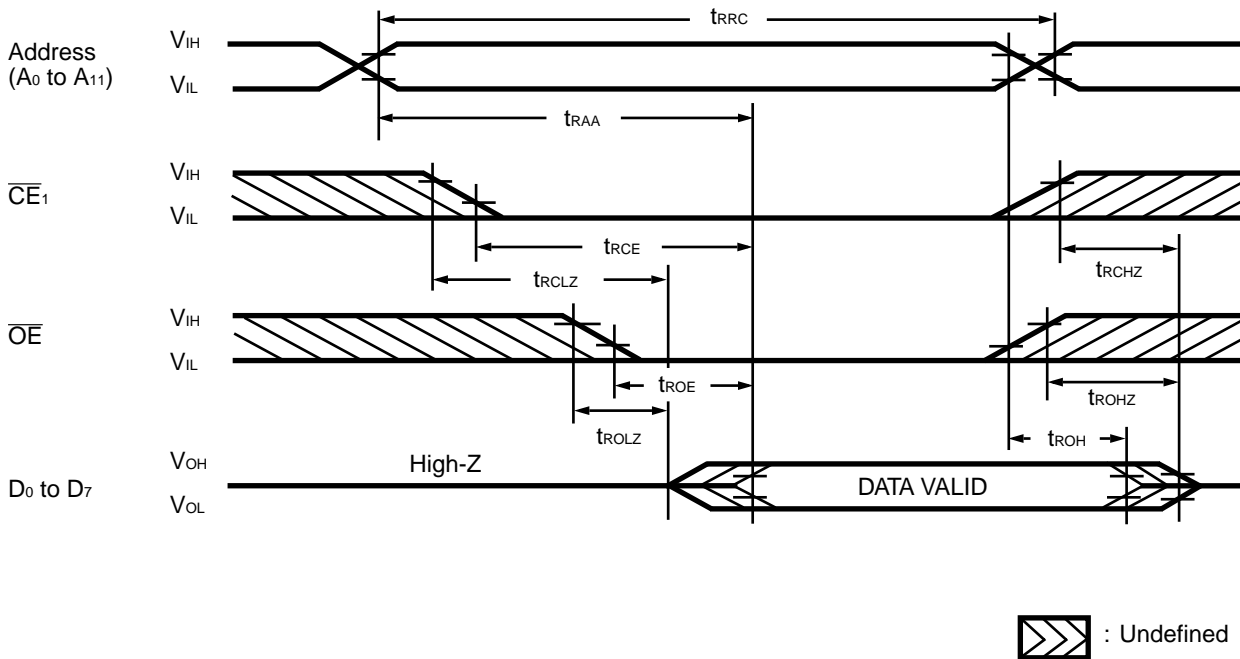
MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IL}$) *1

READ CYCLE 1: $\overline{CE}_1 = \overline{OE} = V_{IL}$, $\overline{CE}_2 = V_{IH}$: × 8-bit Bus Organization
 $\overline{CE}_1 = \overline{CE}_2 = \overline{OE} = V_{IL}$: × 16-bit Bus Organization



READ CYCLE 2: $\overline{CE}_2 = V_{IH}$: × 8-bit Bus Organization



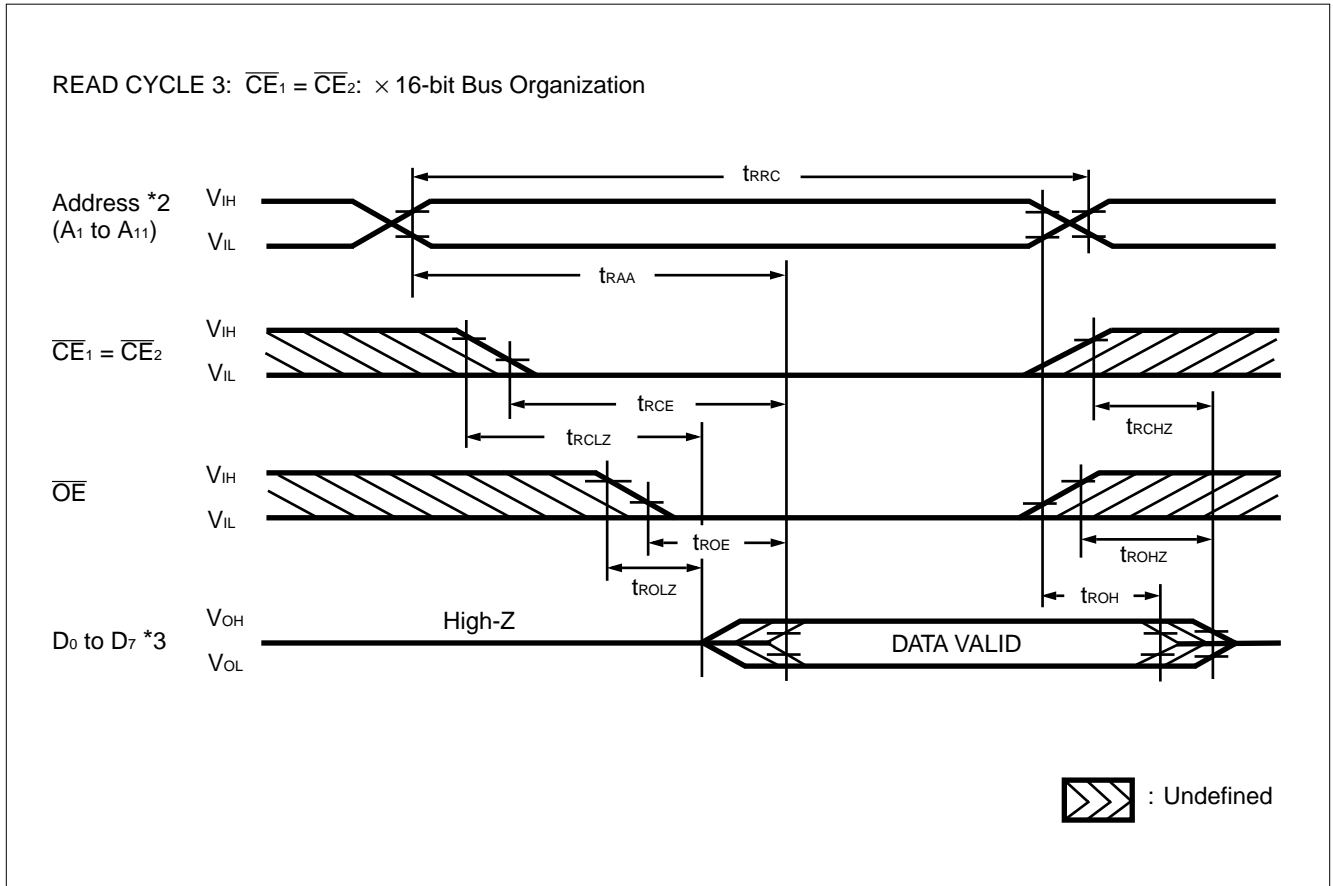
Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

*2. A₀ = Either V_{IH} or V_{IL} during 16 bits bus organization.

*3. H-level is output from D₈ to D₁₅.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE} = V_{IH}$, $\overline{REG} = V_{IL}$) *1



Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

*2. A₀ = Either V_{IH} or V_{IL}.

*3. H-level is output from D₈ to D₁₅.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY WRITE/ERASE CYCLE *1

| Parameter | Notes | Symbol | Min. | Max. | Unit |
|--|-------|--------------------|------|------|------|
| Write Cycle Time | | t _{WC} | 250 | — | ns |
| Address Set Up Time | | t _{AS} | 0 | — | ns |
| Address Hold Time | | t _{AH} | 100 | — | ns |
| Data Set Up Time | | t _{DS} | 80 | — | ns |
| Data Hold Time | | t _{DH} | 30 | — | ns |
| Write Recovery Time before Read | | t _{WHGL} | 6 | — | μs |
| Read Recovery Time before Write | | t _{GHWL} | 0 | — | μs |
| Card Enable Set Up Time before Write | | t _{CS} | 40 | — | ns |
| Card Enable Hold Time | | t _{CH} | 0 | — | ns |
| Write Enable Pulse Width | | t _{WP} | 100 | — | ns |
| Write Enable Pulse Width High | | t _{WPH} | 60 | — | ns |
| Write Enable Set Up Time | | t _{WS} | 0 | — | ns |
| Write Enable Hold Time | | t _{WH} | 0 | — | ns |
| Card Enable Pulse Width | | t _{CP} | 140 | — | ns |
| Card Enable Pulse Width High | | t _{CPH} | 60 | — | ns |
| Duration of Write Operation | *3 | t _{WHWH1} | 10 | — | μs |
| Duration of Erase Operation | *3 | t _{WHWH2} | 9.5 | — | ms |
| V _{PP} Set Up Time to Chip Enable Low | | t _{VPEL} | 1.0 | — | μs |

Notes: *1. Read timing parameters during Write/Erase operations are the same as during read only operations. Refer to AC characteristics for Main Memory Read Cycle.

*2. Rise/Fall time ≤ 5 ns.

*3. The integrated stop timer terminates the Write/Erase operations, thereby eliminating the need for a maximum specification.

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MAIN MEMORY WRITE/ERASE PERFORMANCE *1

| Rating | Notes | Min. | Typ. | Max. | Unit |
|-------------------|-------|---------|---------|-------|-------|
| Chip Erase Time | *1 | — | 2.0 *2 | 30 | Sec. |
| Chip Write Time | | — | 4.0 *2 | 25 *3 | Sec. |
| Write/Erase Cycle | | 100,000 | 100,000 | — | Cycle |

Notes: *1. Excludes 00H writing prior to Erasure.

*2. $T_A = 25^{\circ}\text{C}$, $V_{PP} = 12\text{ V}$, 100,000 Cycles.

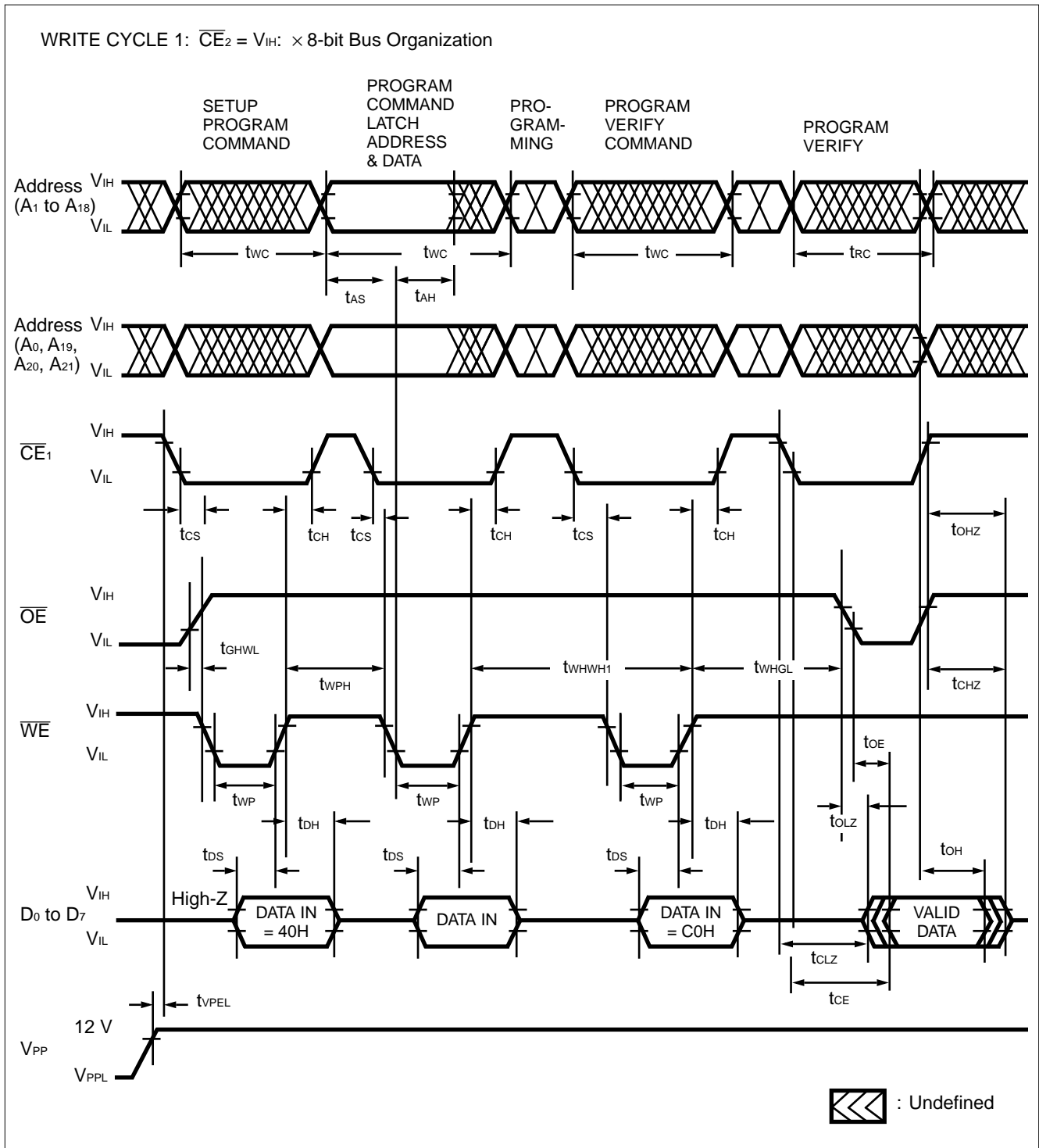
ATTRIBUTE MEMORY WRITE CYCLE *1

| Parameter | Symbol | Min. | Max. | Unit |
|-----------------------------|------------|-------|------|-------|
| Write Cycle Time | t_{RWR} | — | 10 | ms |
| Address Set Up Time | t_{RAS} | 20 | — | ns |
| Card Enable Set Up Time | t_{RCS} | 0 | — | ns |
| Output Enable Set Up Time | t_{ROES} | 20 | — | ns |
| Write Pulse Width | t_{RWP} | 100 | — | ns |
| Address Hold Time | t_{RAH} | 50 | — | ns |
| Data Set Up Time | t_{RDS} | 50 | — | ns |
| Data Hold Time | t_{RDH} | 20 | — | ns |
| Card Enable Hold Time | t_{RCH} | 0 | — | ns |
| Output Enable Hold Time | t_{ROEH} | 20 | — | ns |
| Write Recovery Time | t_{RRE} | 50 | — | ns |
| End of Write to Output Time | t_{RRBO} | — | 100 | ns |
| Number of Write per Byte | N | 10000 | — | Times |
| Write Enable Hold Time | t_{RWEH} | 10 | — | ns |

Note: *1. This parameter is for MB98A809B3, 810B3, 811B3, and 812B3.

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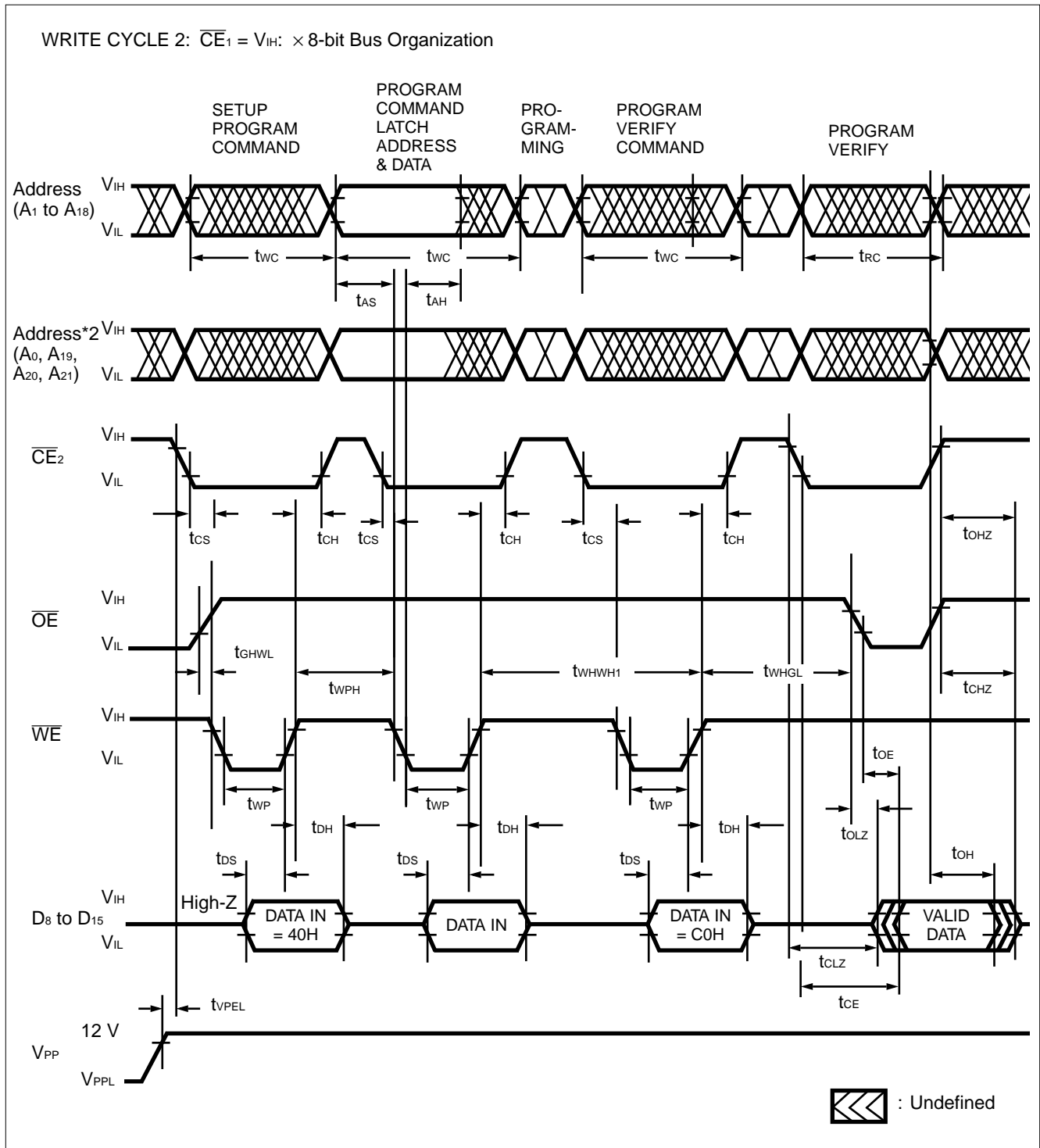
MAIN MEMORY WRITE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1



Note: *1. A₀, A₁₉, A₂₀ and A₂₁ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1

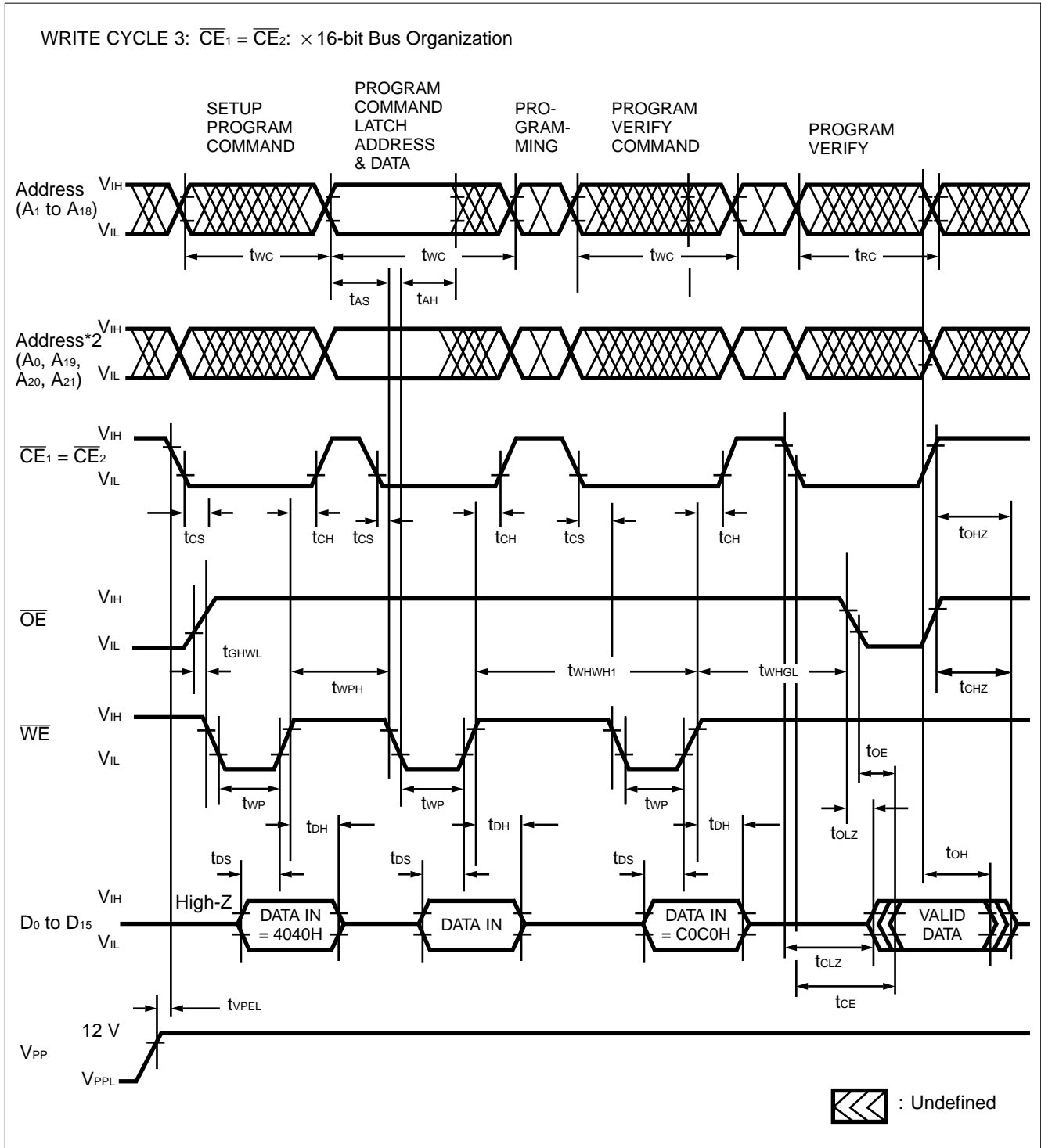


Notes: *1. A_0, A_{19}, A_{20} and A_{21} have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. $A_0 = \text{Either } V_{IL} \text{ or } V_{IH}$.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1

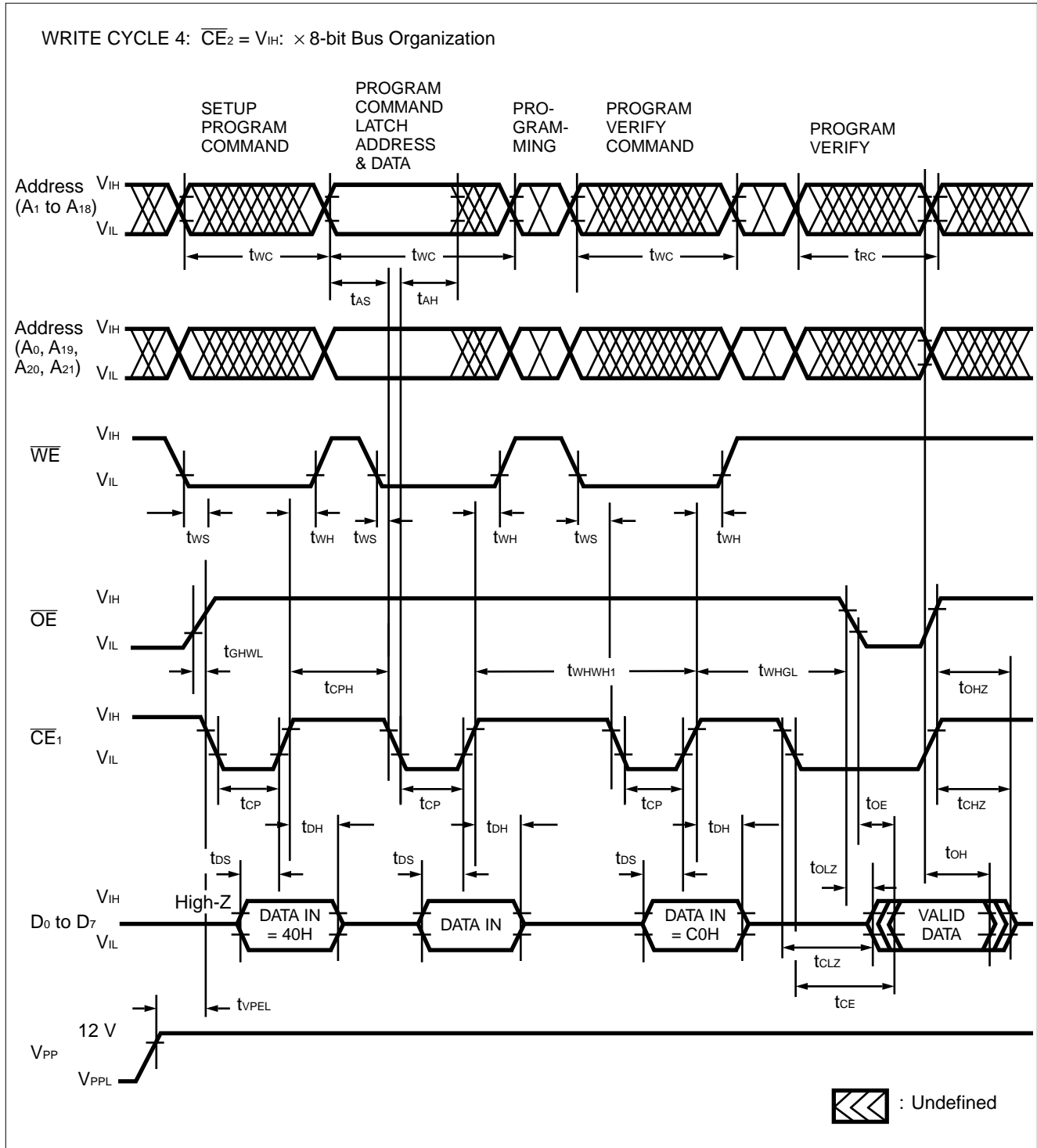


Notes: *1. A₀, A₁₉, A₂₀ and A₂₁ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. A₀ = Either V_{IL} or V_{IH}.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

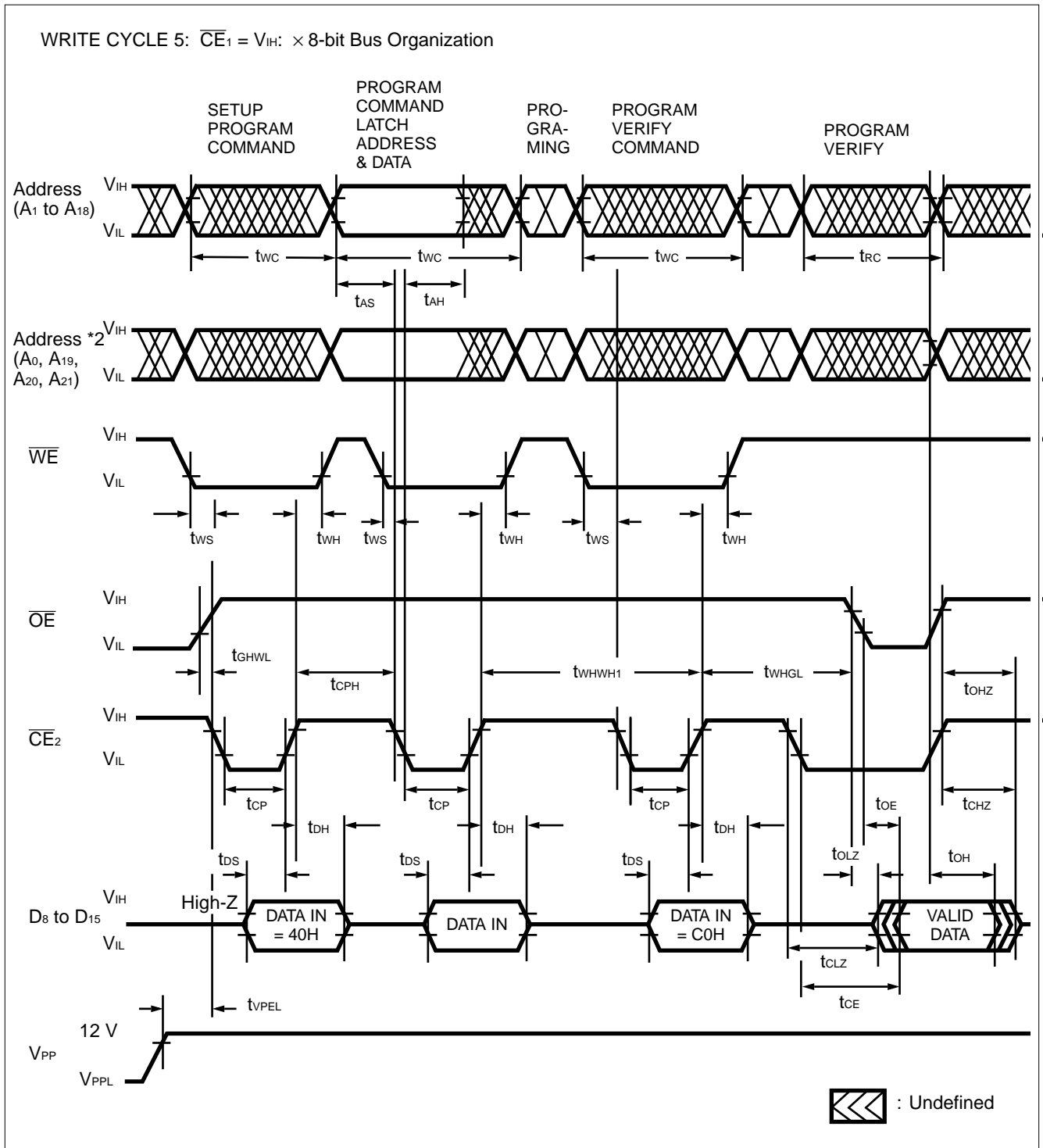
MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE} = \text{CONTROLLED}$) *1



Note: *1. A₀, A₁₉, A₂₀ and A₂₁ have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE} = \text{CONTROLLED}$) *1

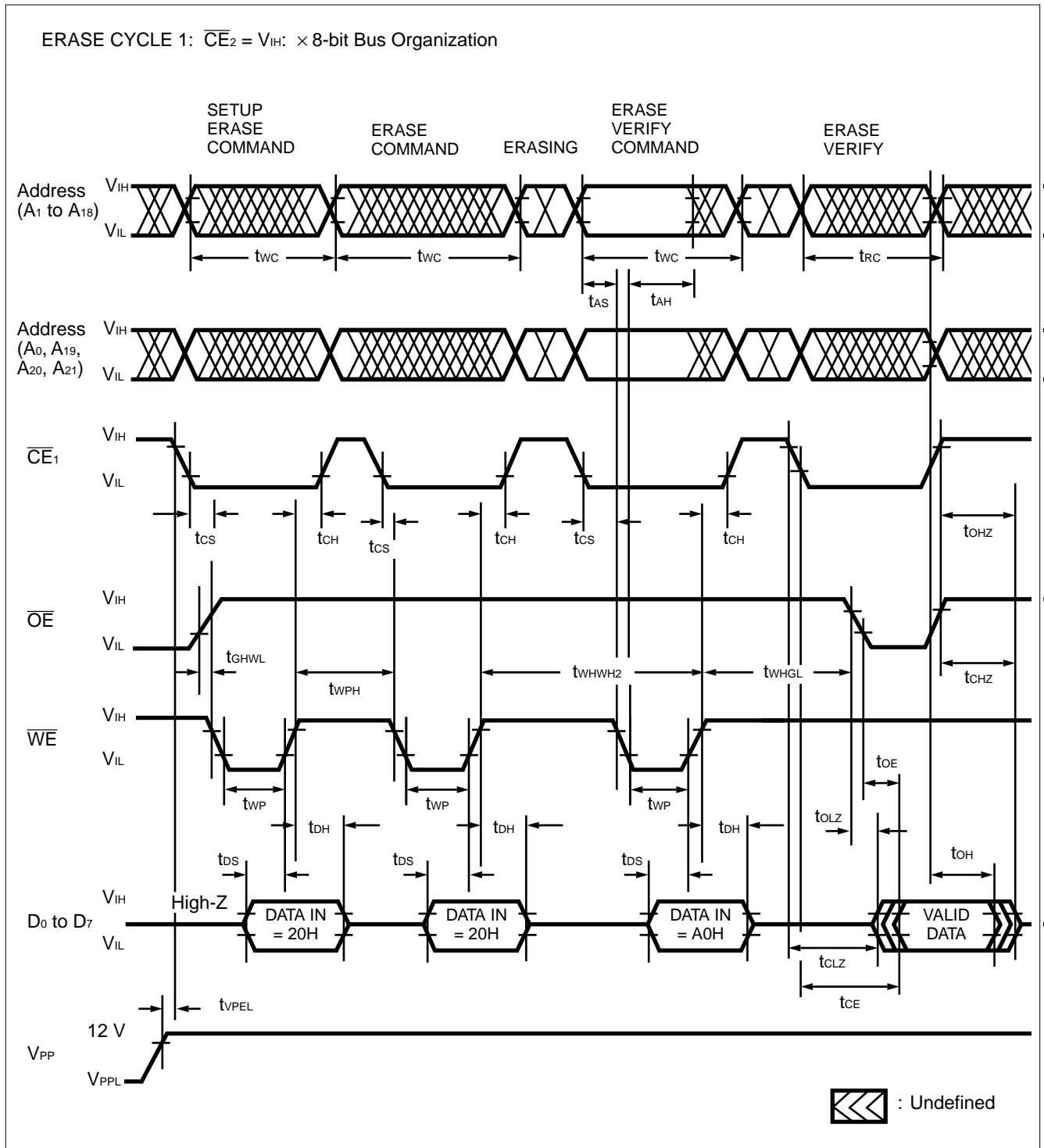


Notes: *1. A_0 , A_{19} , A_{20} and A_{21} have to be fixed during programming command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. $A_0 = \text{Either } V_{IL} \text{ or } V_{IH}$.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

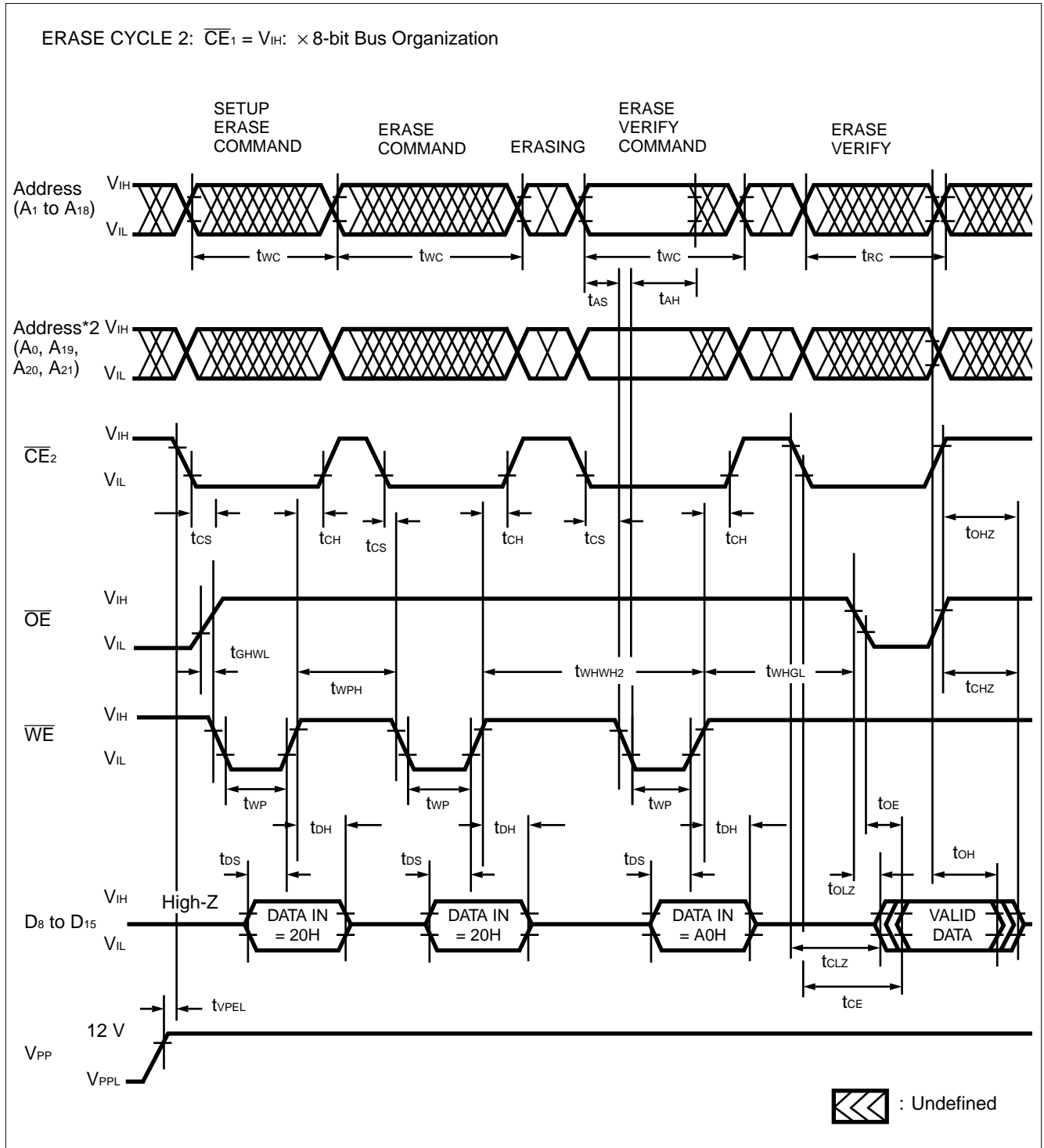
MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1



Note: *1. A₀, A₁₉, A₂₀ and A₂₁ have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

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MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1

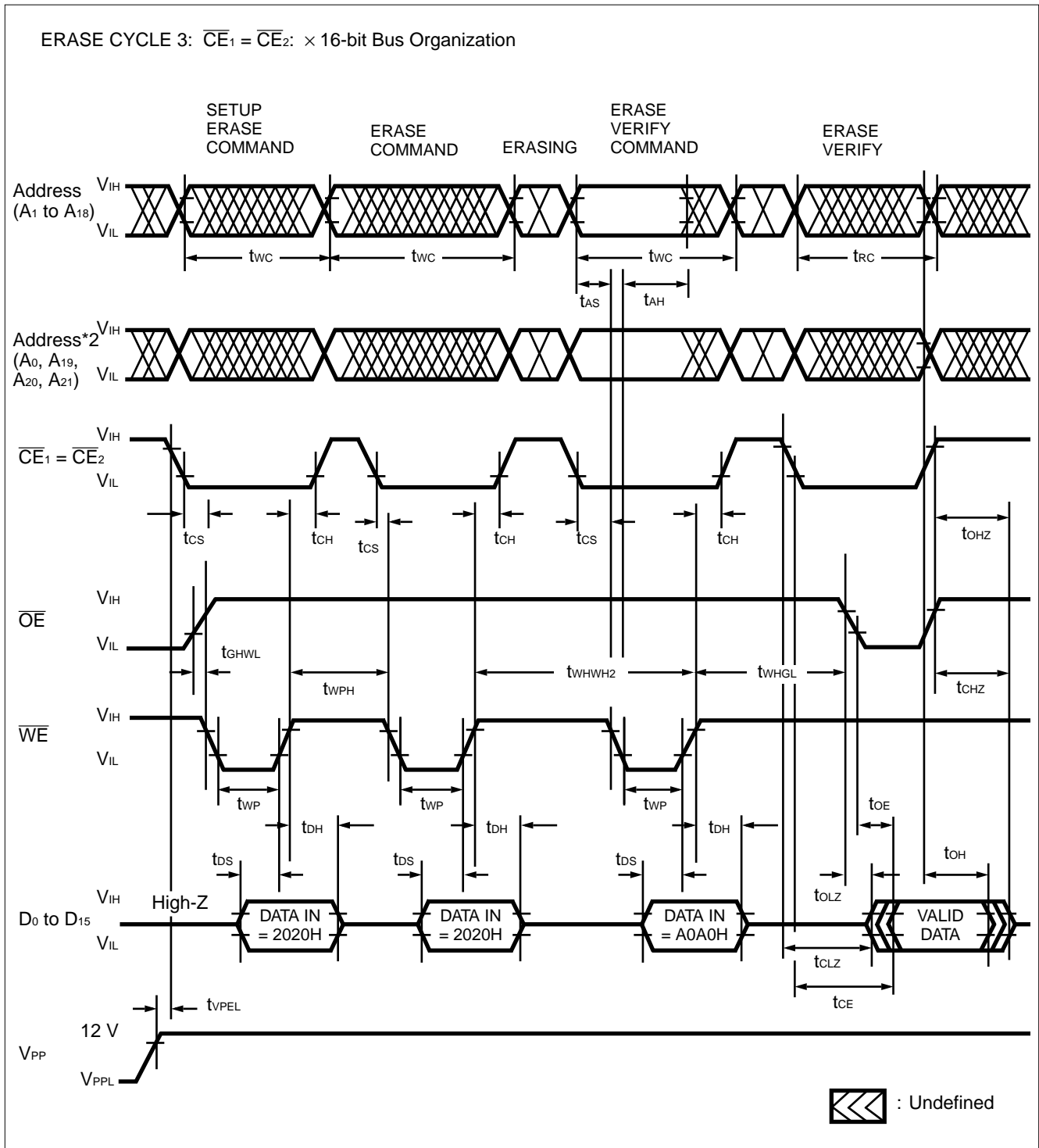


Notes: *1. A_0 , A_{19} , A_{20} and A_{21} have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. $A_0 = \text{Either } V_{IL} \text{ or } V_{IH}$.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED) *1

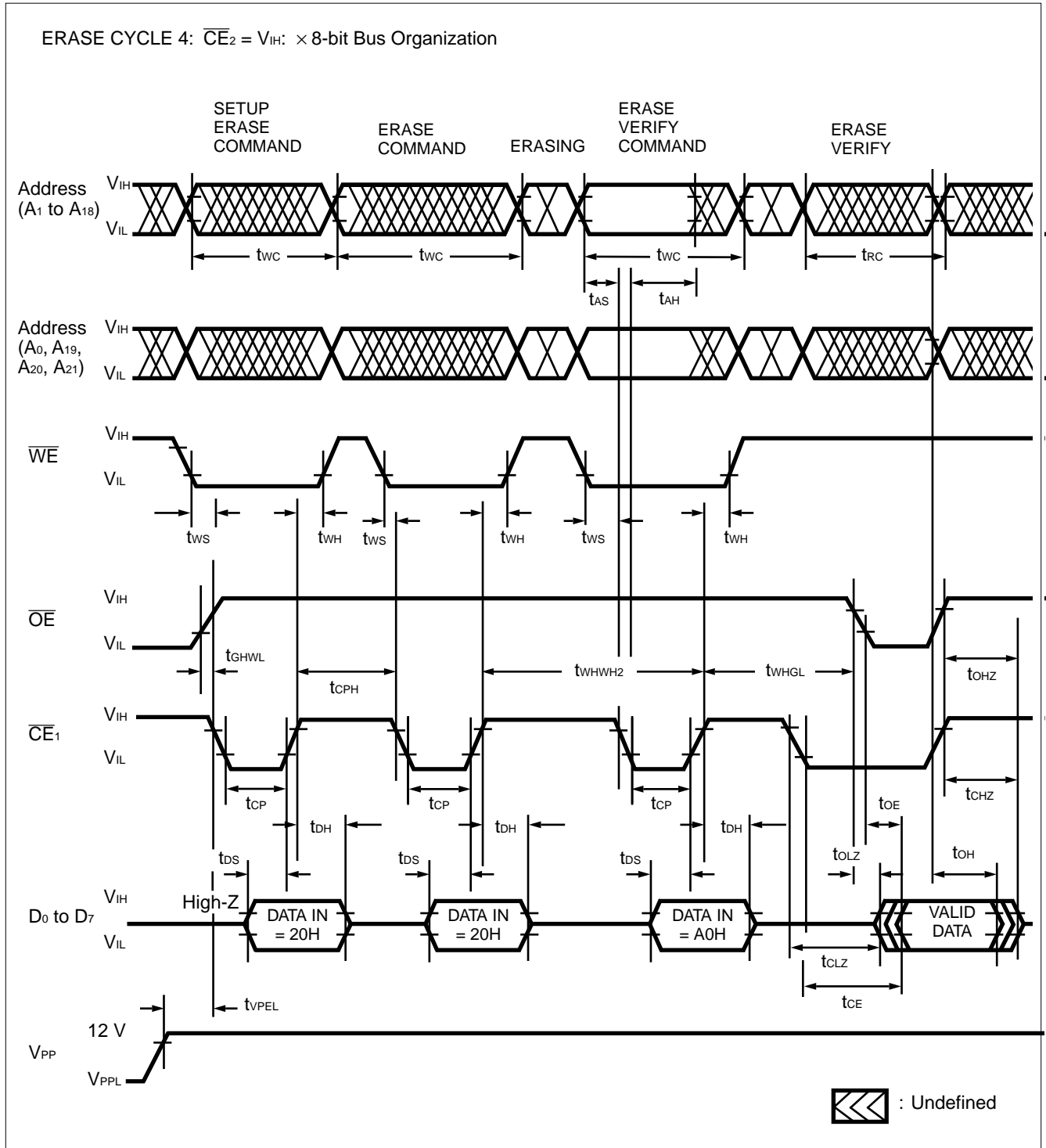


Notes: *1. A_0 , A_{19} , A_{20} and A_{21} have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. A_0 = Either V_{IL} or V_{IH} .

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

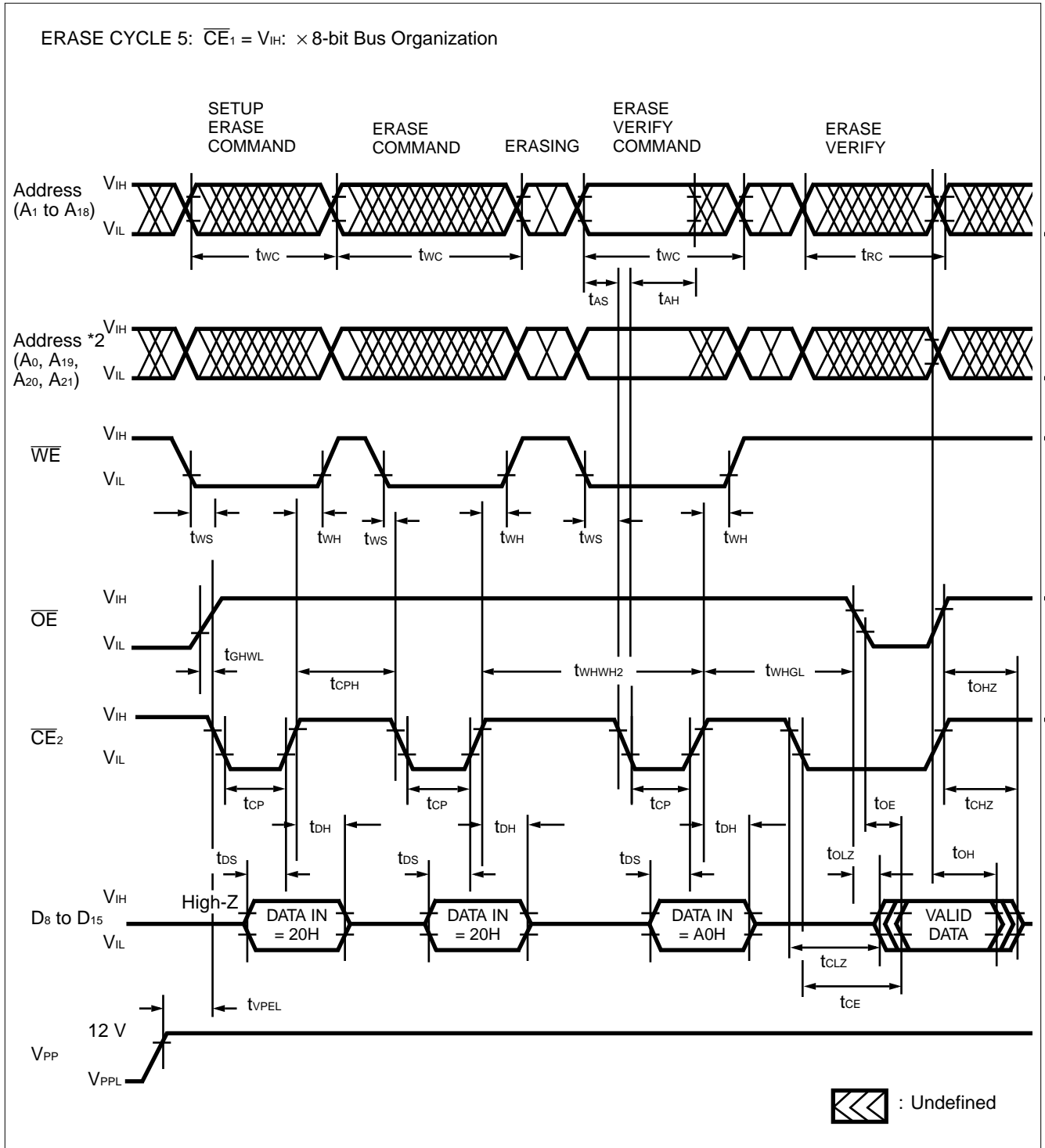
MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{CE} = CONTROLLED) *1



Note: *1. A_0 , A_{19} , A_{20} and A_{21} have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{CE} = CONTROLLED) *1

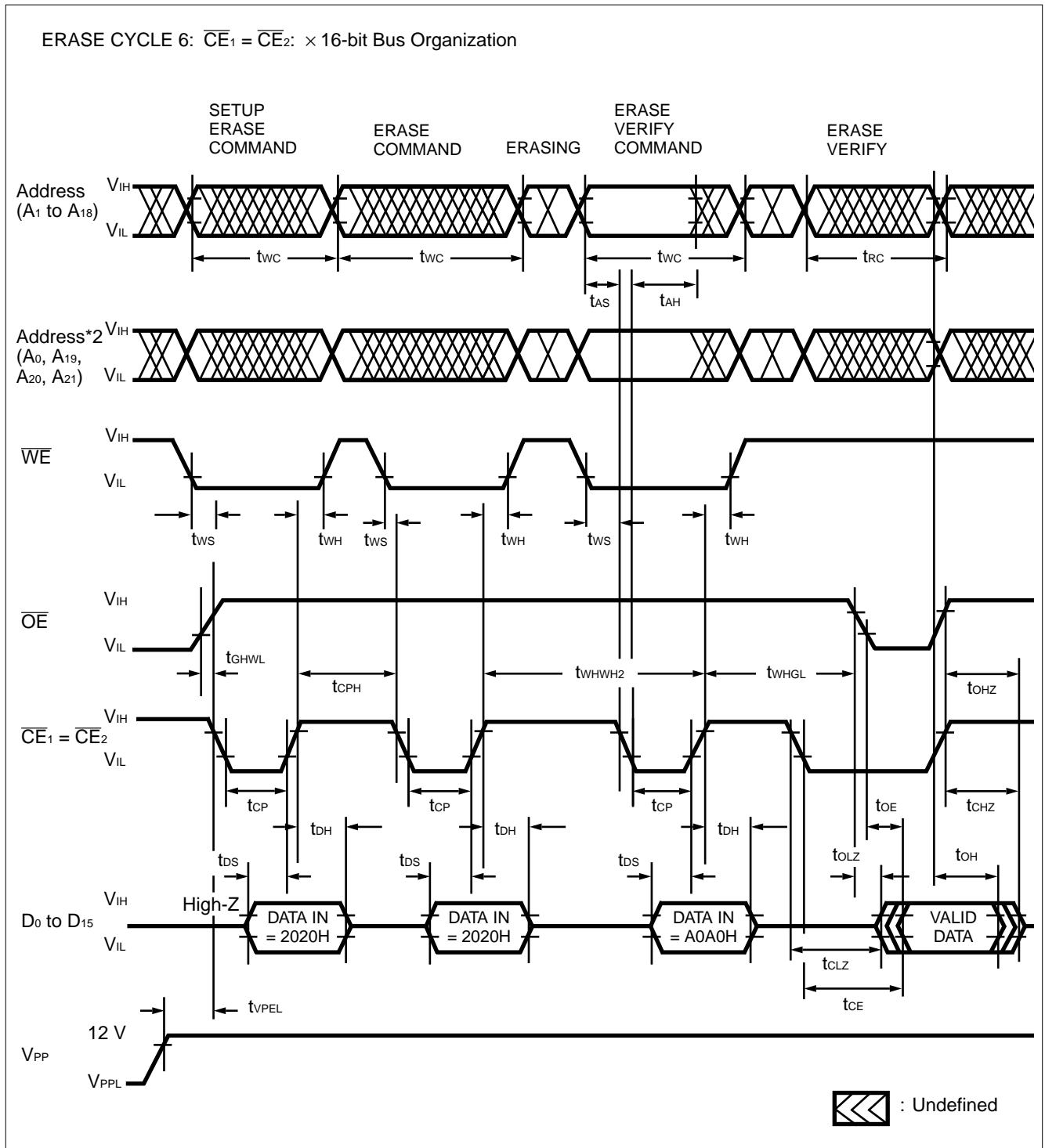


Notes: *1. A_0, A_{19}, A_{20} and A_{21} have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. $A_0 = \text{Either } V_{IL} \text{ or } V_{IH}$.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

MAIN MEMORY ERASE CYCLE TIMING DIAGRAM (\overline{CE} = CONTROLLED) *1

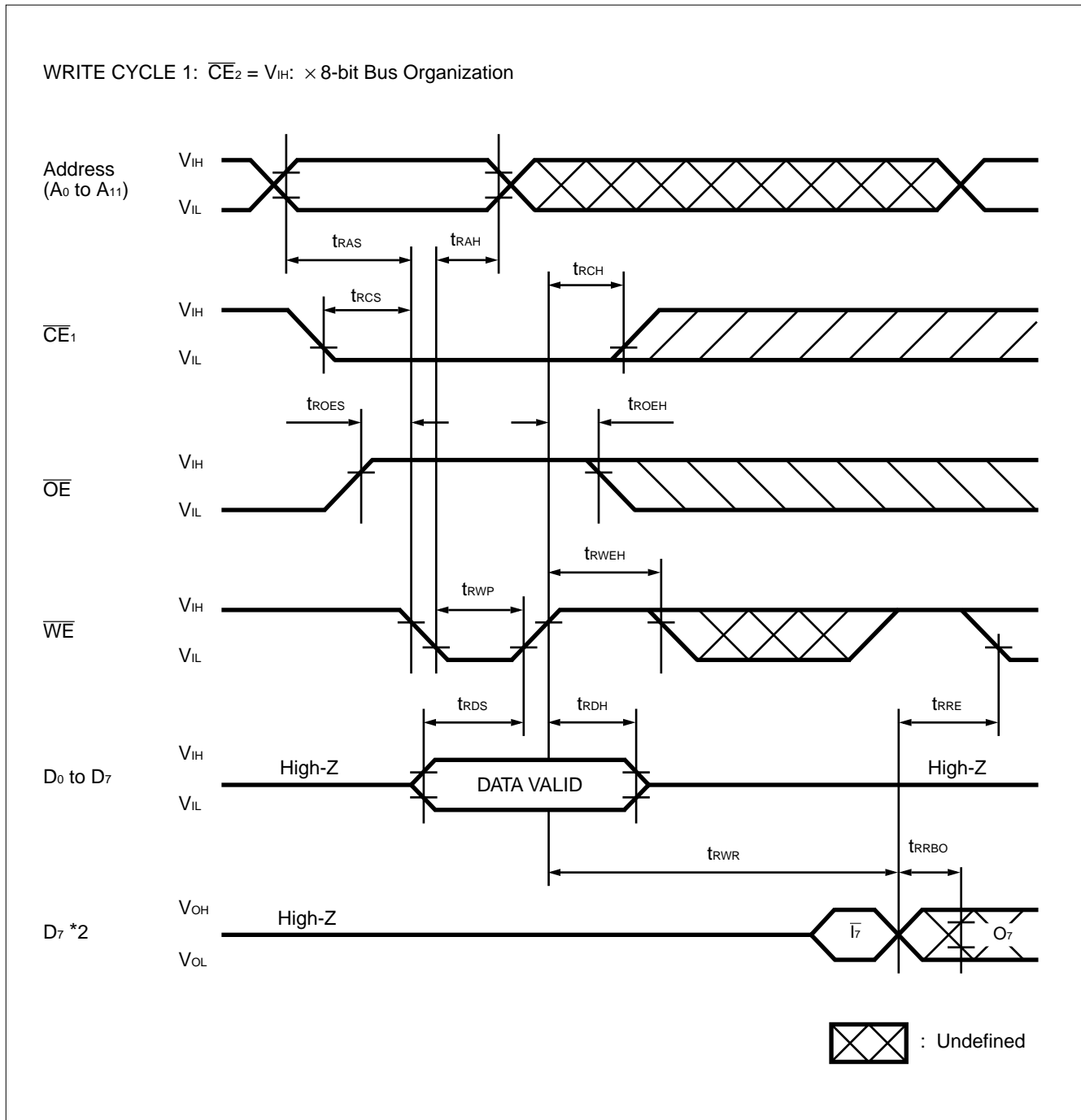


Notes: *1. A₀, A₁₉, A₂₀ and A₂₁ have to be fixed during erase command input because these addresses are chip decoding addresses. Refer to the WRITE/ERASE CHIP DECODING INFORMATION.

*2. A₀ = Either V_{IL} or V_{IH}.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE} = \text{CONTROLLED}$, $\overline{REG} = V_{IL}$) *1

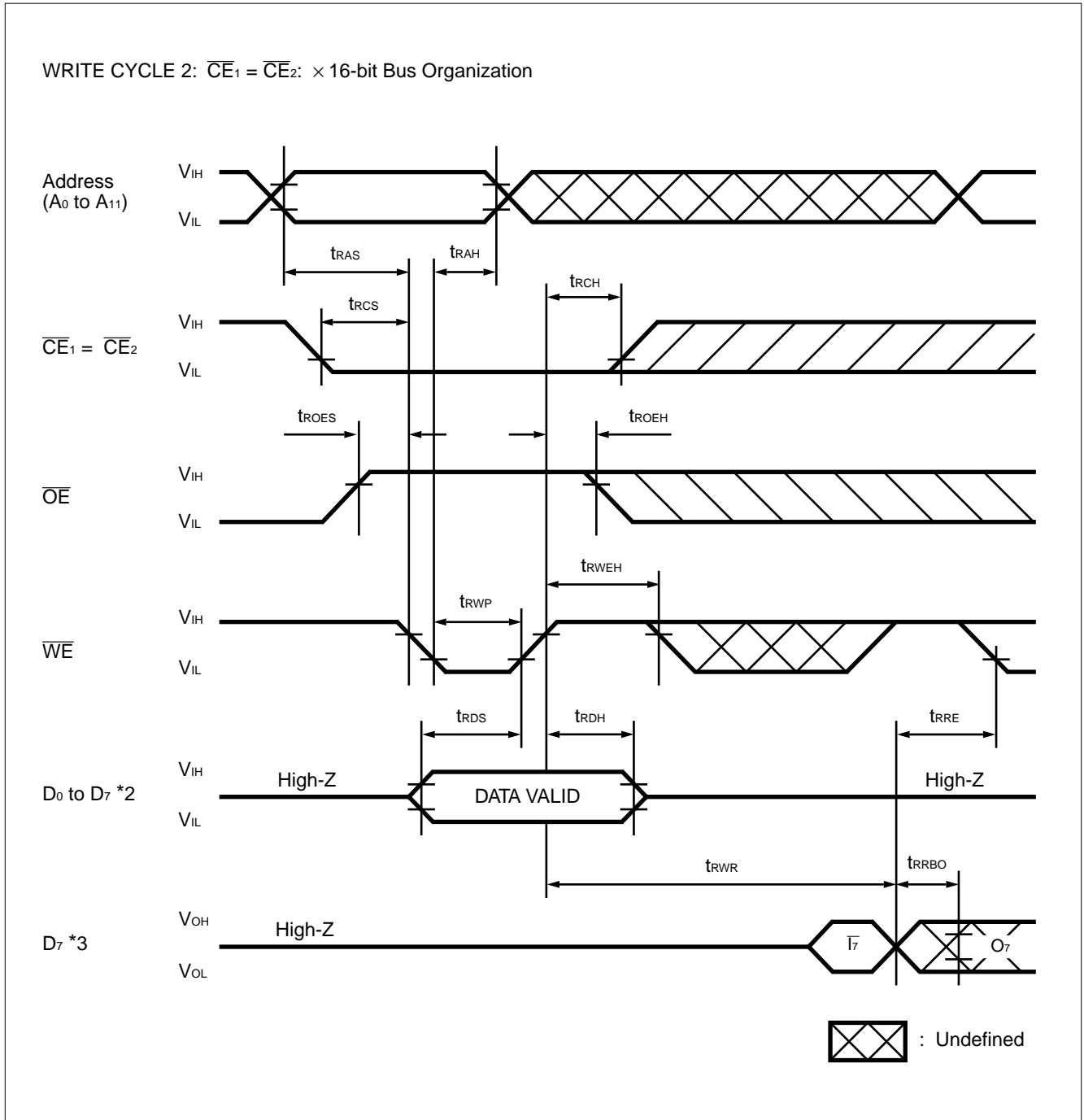


Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

*2. Data polling operation.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM (\overline{WE} = CONTROLLED, \overline{REG} = V_{IL}) *1



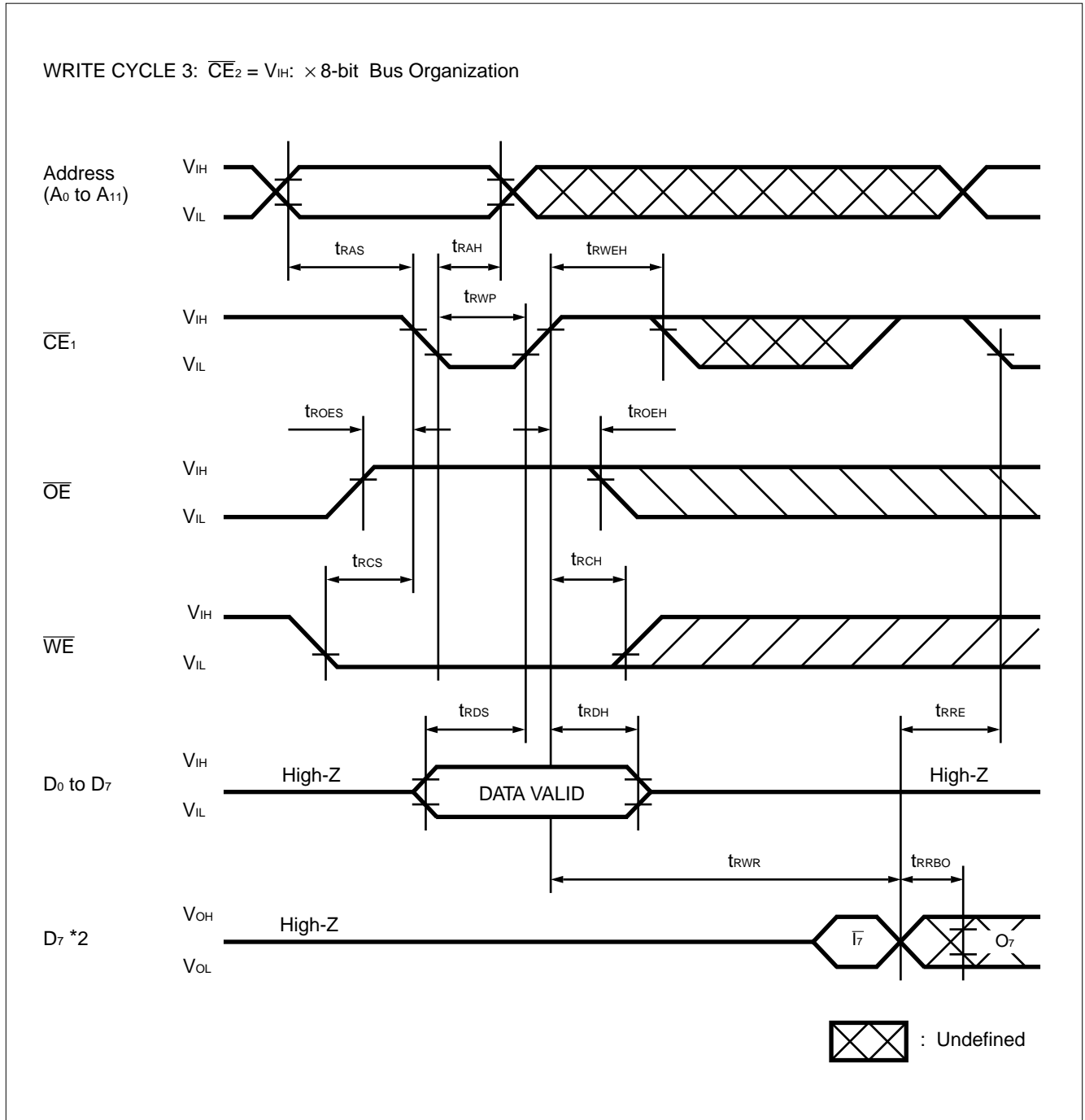
Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

*2. H-level or L-level is output from D₈ to D₁₅.

*3. Data polling operation.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE} = \text{CONTROLLED}$, $\overline{REG} = V_{IL}$) *1

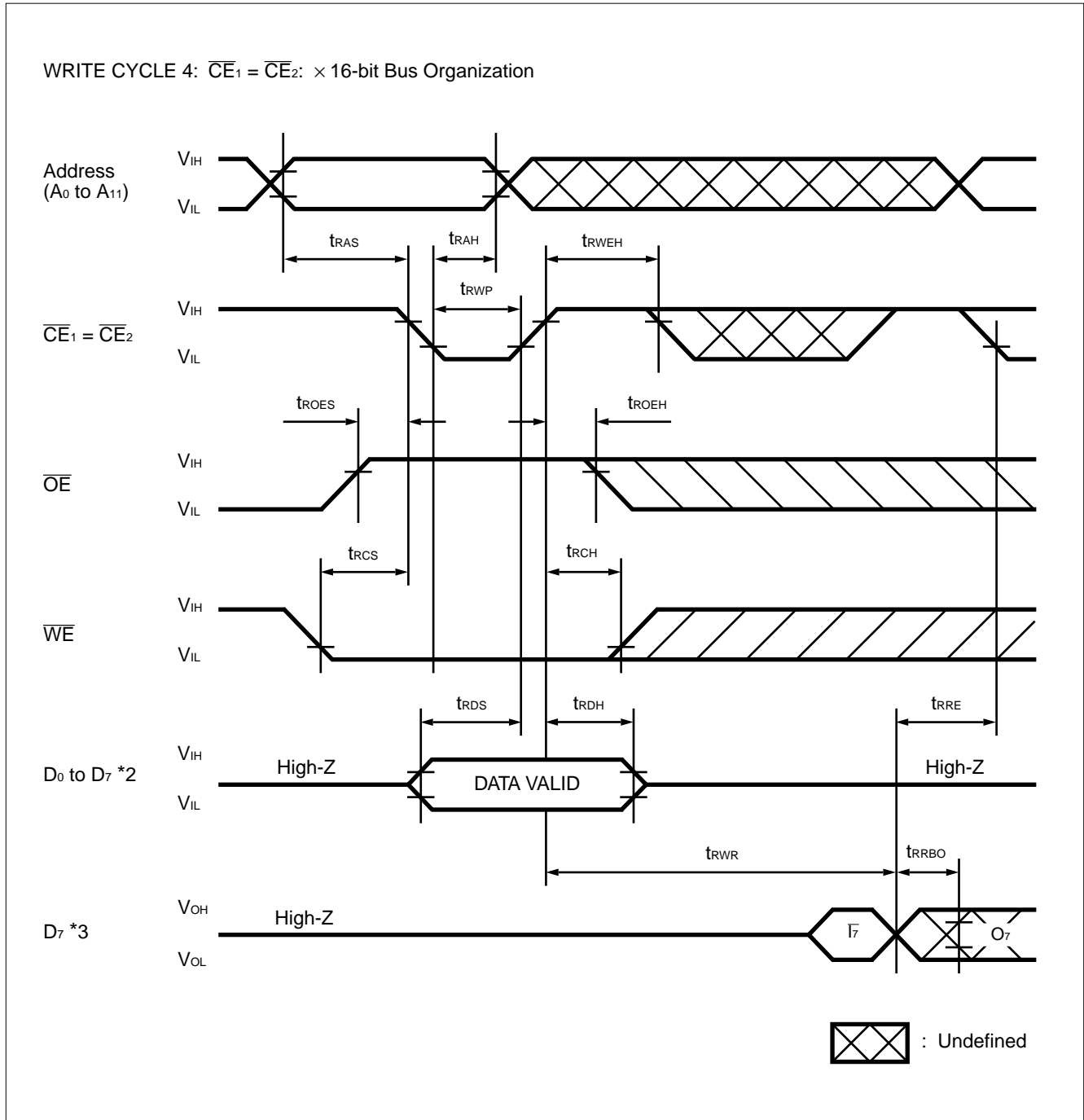


Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

*2. Data polling operation.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE} = \text{CONTROLLED}$, $\overline{REG} = V_{IL}$) *1



Notes: *1. This timing diagram is for MB98A809B3, 810B3, 811B3, and 812B3. "FF" data is available on MB98A809B2, 810B2, 811B2, and 812B2 only.

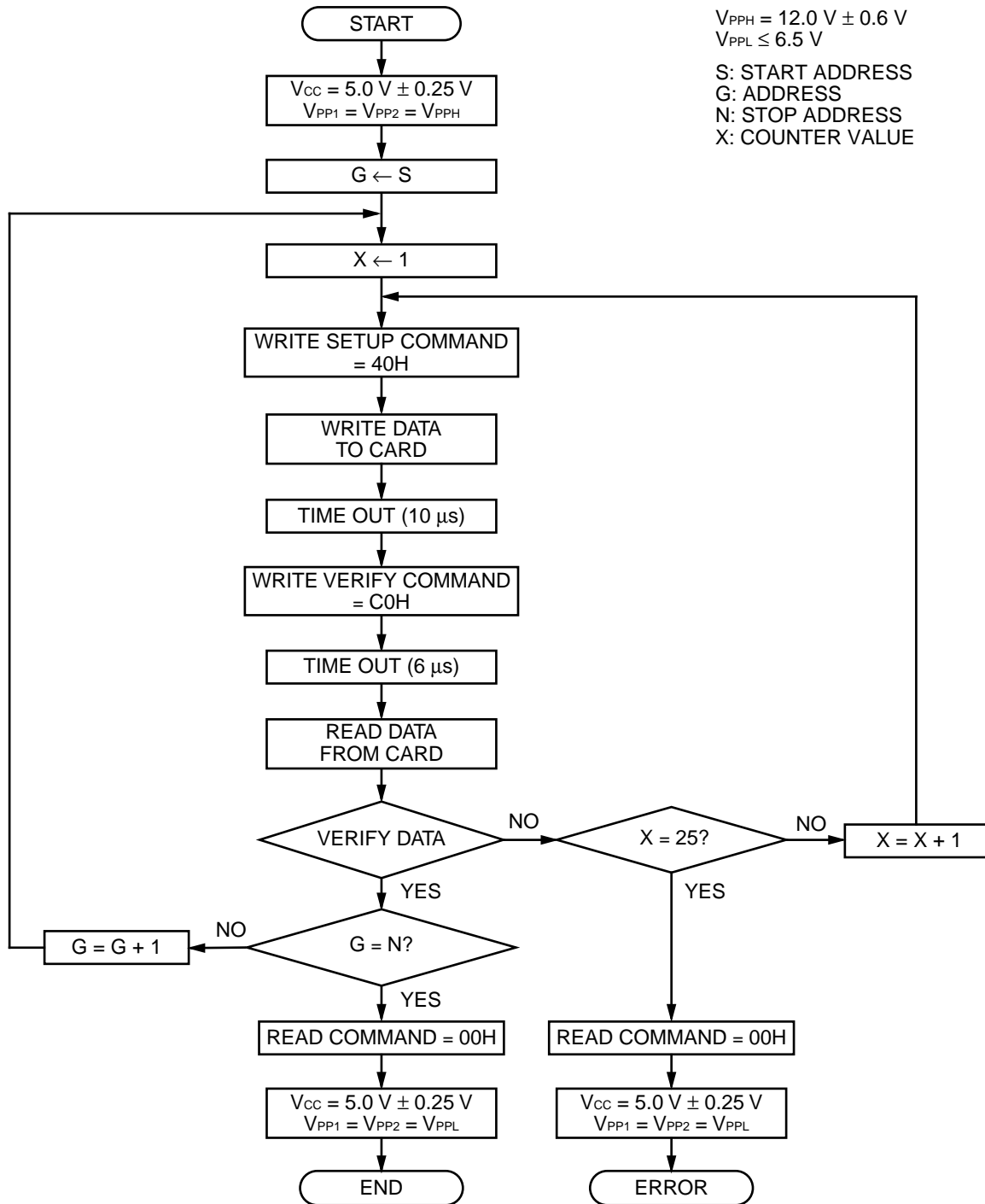
*2. H-level or L-level is output from D₈ to D₁₅.

*3. Data polling operation.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

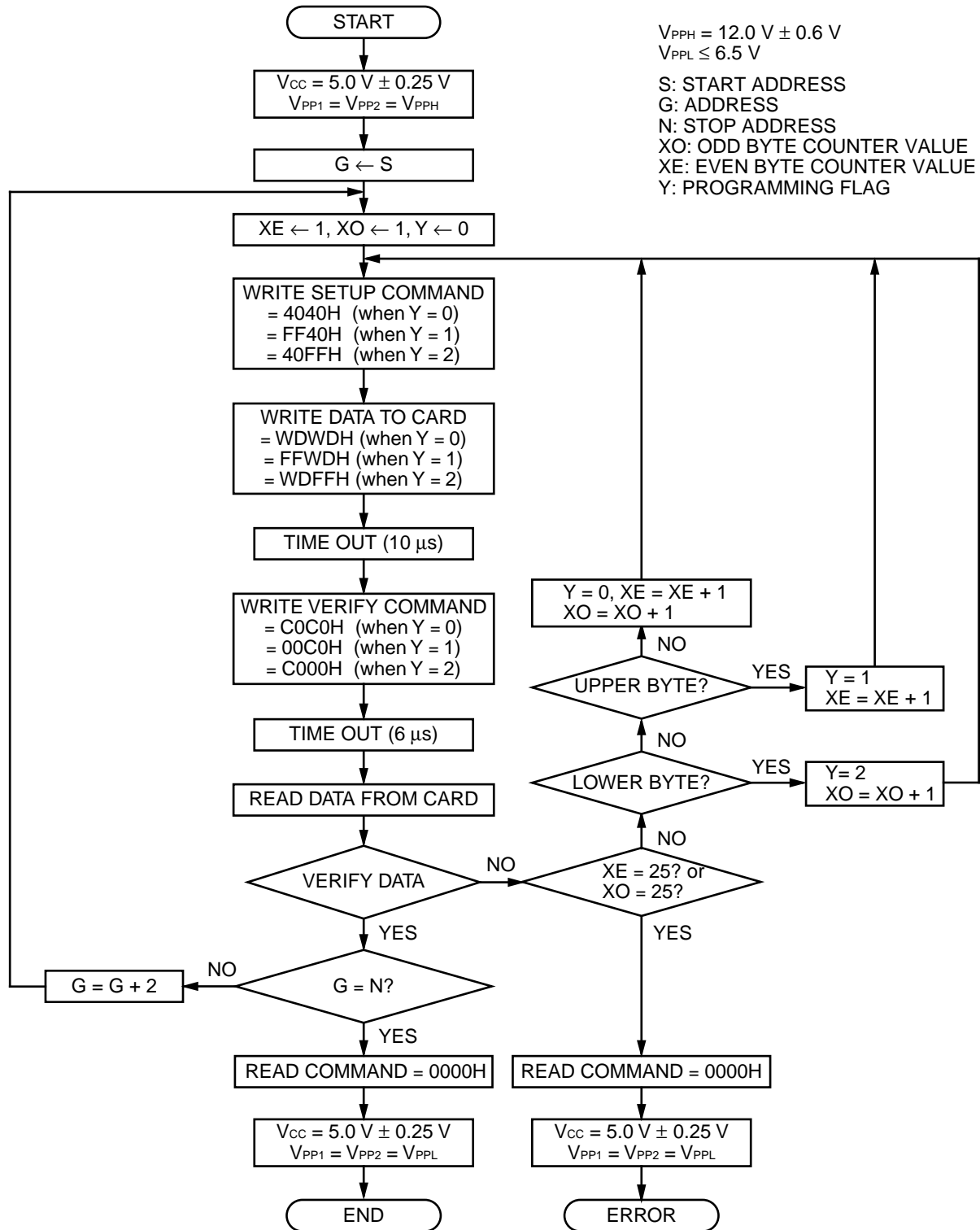
■ WRITE/ERASE INFORMATION

Fig. 4 – WRITE FLOWCHART FOR 8-BIT ORGANIZATION



MB98A809Bx-/810Bx-/811Bx-/812Bx-25

Fig. 5 – WRITE FLOWCHART FOR 16-BIT ORGANIZATION

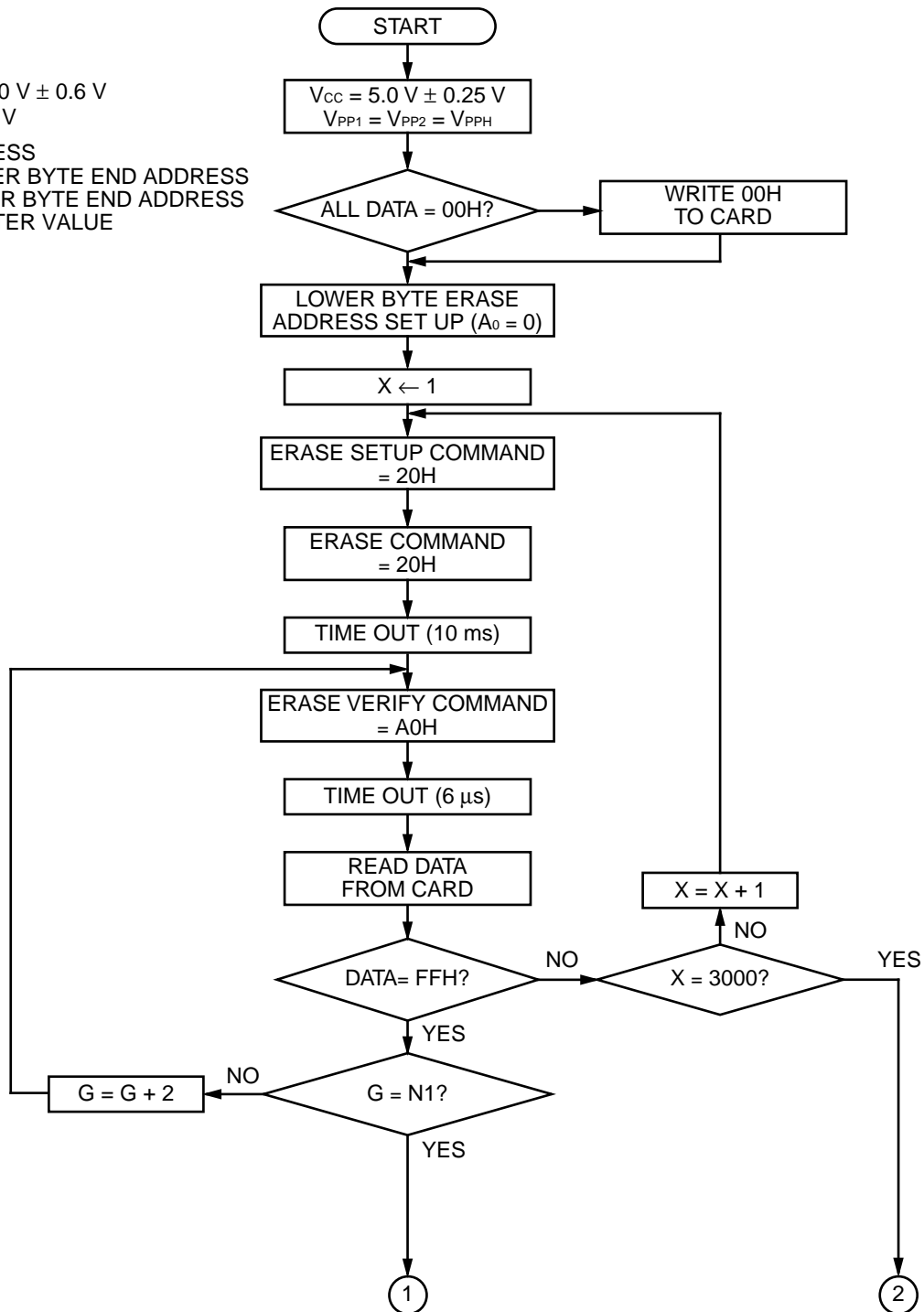


MB98A809Bx-/810Bx-/811Bx-/812Bx-25

Fig. 6 – ERASE FLOWCHART FOR 8-BIT ORGANIZATION

$V_{PPH} = 12.0\text{ V} \pm 0.6\text{ V}$
 $V_{PPL} \leq 6.5\text{ V}$

G: ADDRESS
 N1: LOWER BYTE END ADDRESS
 N2: UPPER BYTE END ADDRESS
 X: COUNTER VALUE



(Continued on page 41.)

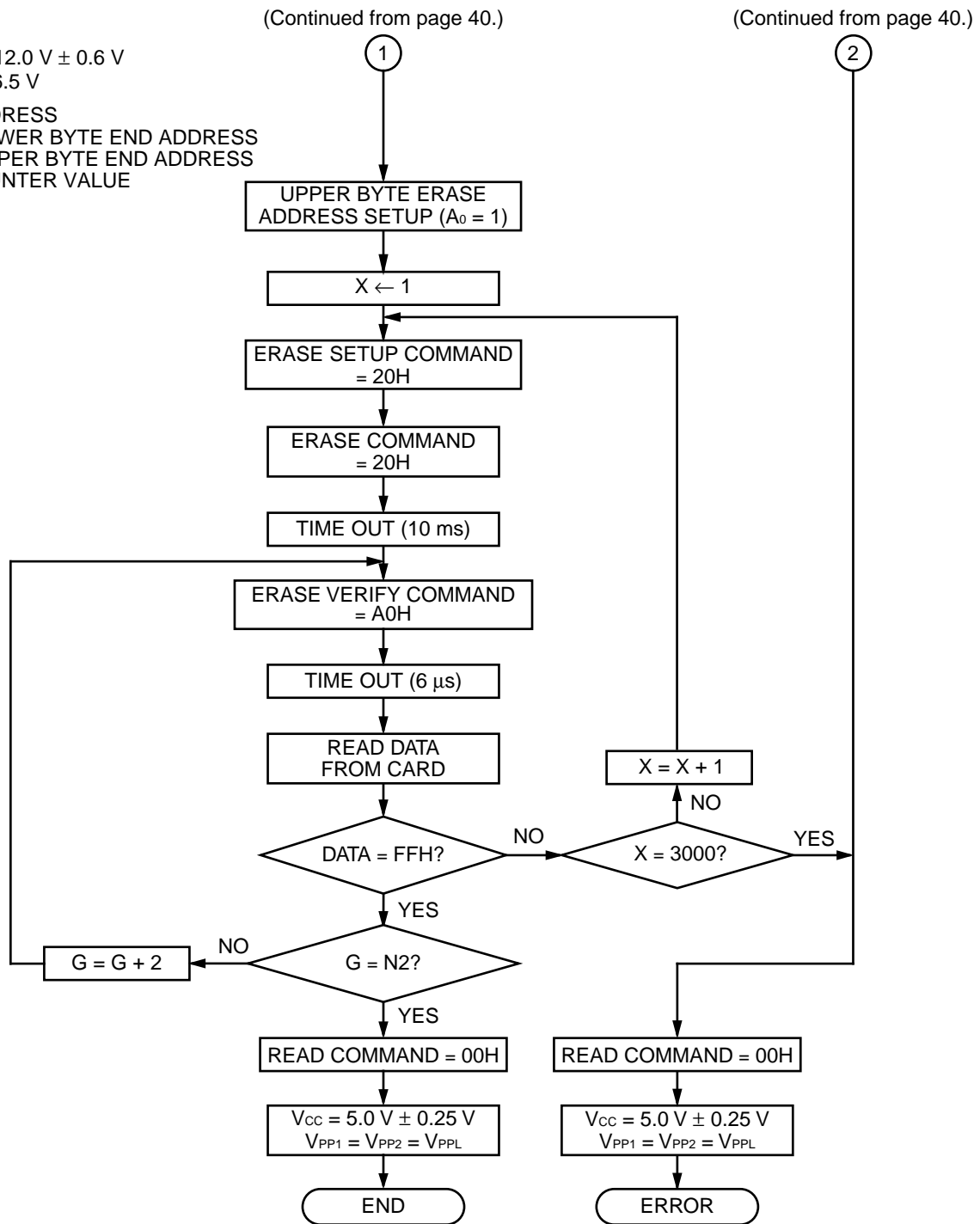
(Continued on page 41.)

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

Fig. 7 – ERASE FLOWCHART FOR 8-BIT ORGANIZATION (Continued)

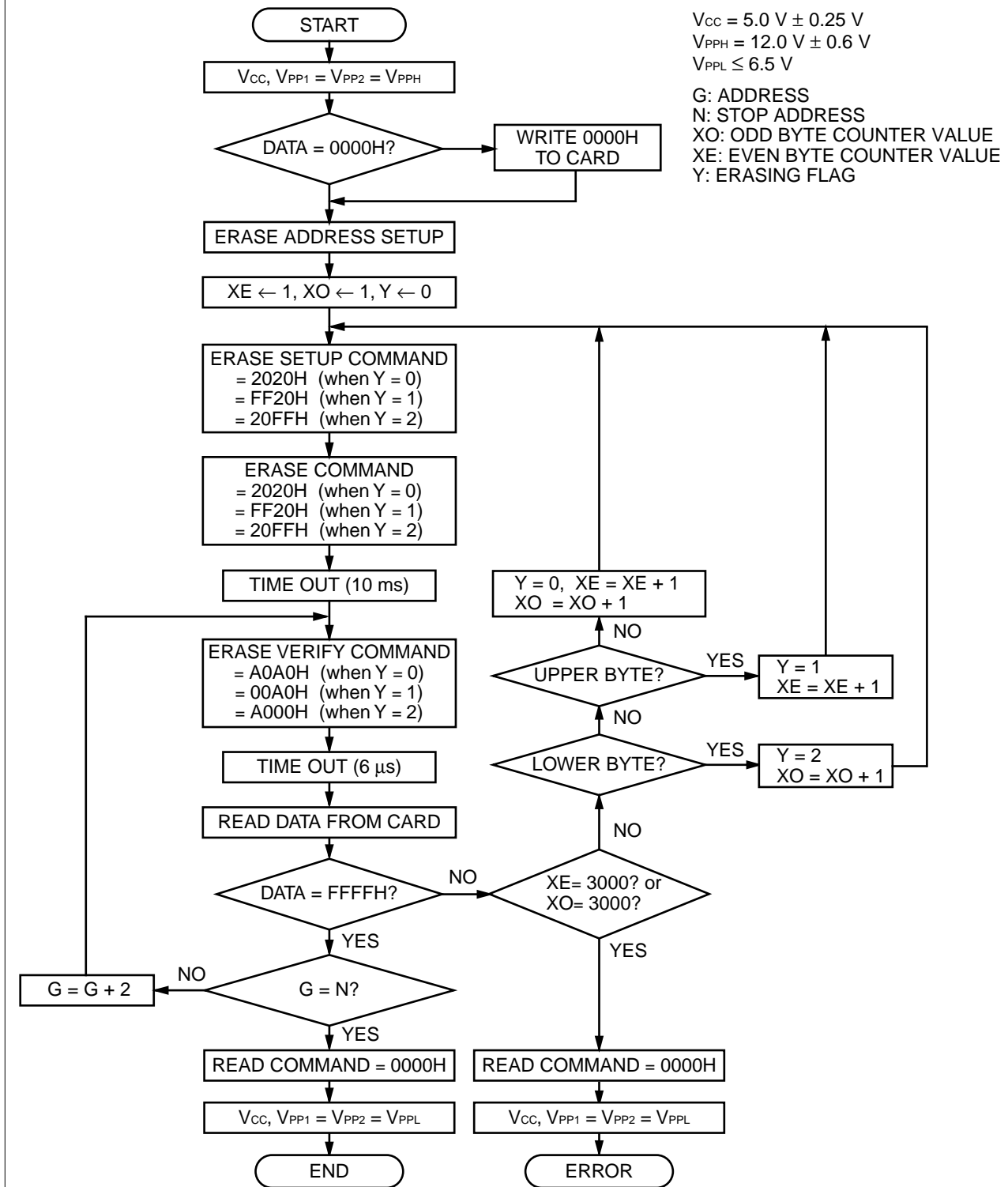
$V_{PPH} = 12.0\text{ V} \pm 0.6\text{ V}$
 $V_{PPL} \leq 6.5\text{ V}$

G: ADDRESS
 N1: LOWER BYTE END ADDRESS
 N2: UPPER BYTE END ADDRESS
 X: COUNTER VALUE



MB98A809Bx-/810Bx-/811Bx-/812Bx-25

Fig. 8 – ERASE FLOWCHART FOR 16-BIT ORGANIZATION



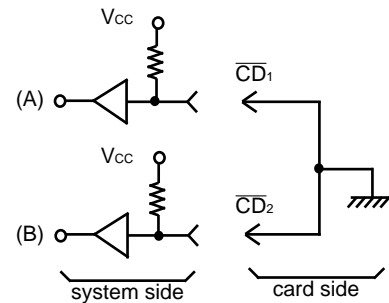
MB98A809Bx-/810Bx-/811Bx-/812Bx-25

■ UNIQUE FEATURES FOR FLASH MEMORY CARD

1. SPECIAL MONITORING PINS

1.1 \overline{CD}_1 , \overline{CD}_2 : Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 9.)
When the memory card has been correctly inserted, \overline{CD}_1 and \overline{CD}_2 are detected by the system. \overline{CD}_1 , \overline{CD}_2 are tied to ground on the card side as shown in Fig. 9.



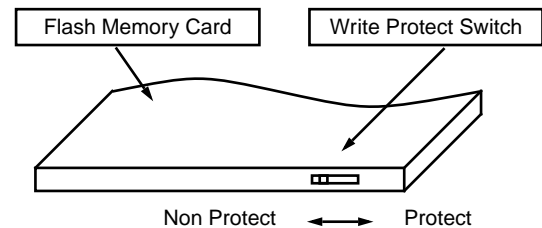
– Fig. 9 –

1.2 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 10, the Flash memory card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the “Non Protect” position and the \overline{WE} pin low. L-level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the “Protect” position. H-level is output on the WP pin.



– Fig. 10 –

| WP Switch | WP (output) |
|-------------|-------------|
| Protect | H |
| Non Protect | L |

■ DEVICE HANDLING PRECAUTIONS

This device is composed of fine electronic parts, so take care in handling or keeping it as below.

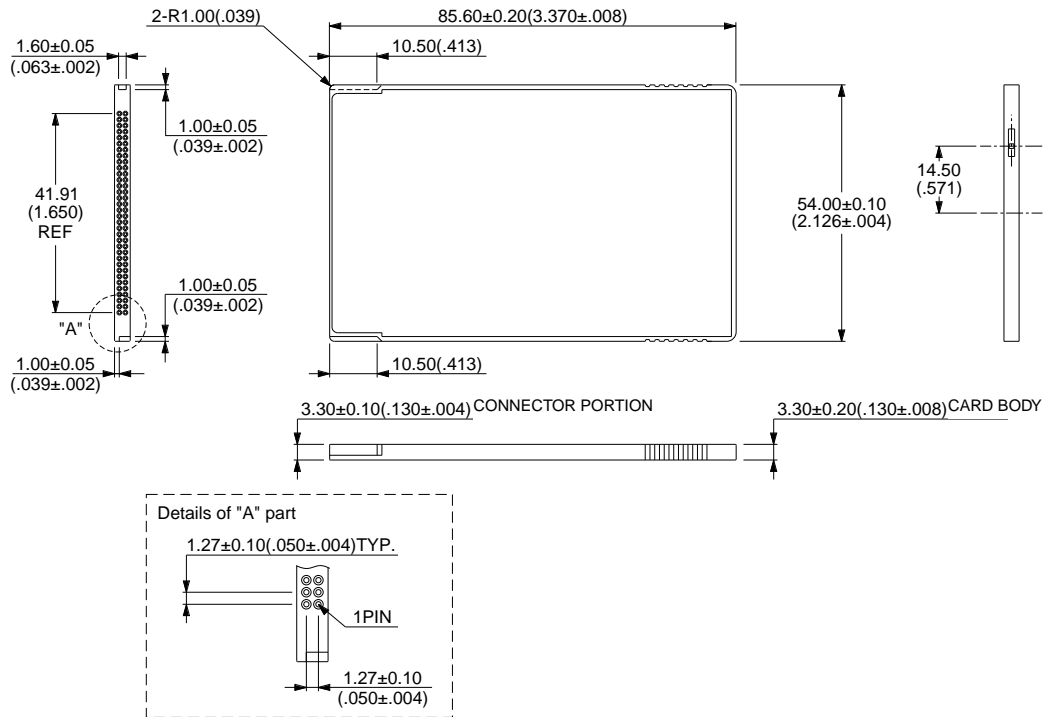
- The card is made fine, so do not keep it in the high temperature nor high humidity, place like in the direct sunshine nor near the heater.
- The card should not be bent, scratched, dropped nor be shocked violently.
- This device should never be taken apart. It could destroy the card or your personal computer hardware.
- To help you handle this device safely, request us the device specifications when purchasing this device.

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

■ PACKAGE DIMENSIONS

68-PIN MEMORY CARD (CASE No.: CRD-68P-M17)

Dimensions conform with PCMCIA/JEIDA (PC CARD STANDARD 95)



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Dimensions in mm (inches)

MB98A809Bx-/810Bx-/811Bx-/812Bx-25

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