FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12518-7E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89170/170A/170L Series

MB89173/P173/174A/P175A/PV170A
MB89173L/174L

■ OUTLINE

The MB89170/170A/170L series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a great variety of peripheral functions such as timers, a serial interface, a DTMF generator, and external interrupts, making it suitable for circuit control such as required in telephones.

*: F²MC stands for FUJITSU Flexible Microcontroller.

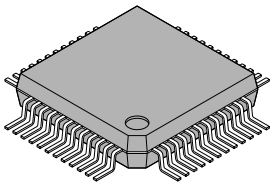
■ FEATURES

- F²MC-8L family CPU core
- Maximum memory space: 64 Kbytes
- Minimum execution time/interrupt processing time
  MB89170 series: 1.1 µs/10 µs (at 3.58 MHz oscillation)
  MB89170A/170L series: 0.6 µs/5.4 µs (at 7.16 MHz oscillation)
- Dual-clock control system (MB89170/170A series only)
- I/O ports: max. 37 ports
- 21-bit timebase counter
- Watch prescaler (MB89170/170A series only)
- Watchdog timer
- 8/16-bit timer/counter: 1 channel

(Continued)

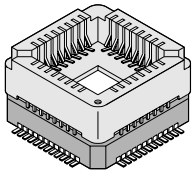
■ PACKAGE

48-pin Plastic QFP



(FPT-48P-M16)

48-pin Ceramic MQFP



(MQP-48C-P01)

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- 8-bit serial I/O: 1 channel
- DTMF generator (MB89170/170A series only)
  Selectable oscillation frequency (MB89170A series only)
- External interrupt 1: 3 channels
  Three channels are independent and capable of using for wake-up from low-power consumption modes (with an edge detection function).
- External interrupt 2 (wake-up): 8 channels
  Eight channels are independent and capable of using for wake-up from low-power consumption modes (with an “L” level detection function).
- Low-power consumption modes(stop mode, sleep mode, watch mode, and subclock mode)
- CMOS technology

■ PRODUCT LINEUP

Part number / Item	MB89173	MB89P173	MB89174A	MB89P175A	MB89PV170A
Classification	Mass-produced product (mask ROM product)	One-time PROM product (EPROM product)	Mass-produced product (mask ROM product)	One-time PROM product (EPROM product)	Piggyback/ evaluation product (for evaluation and development)
ROM size	8 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	12 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	384 × 8 bits		512 × 8 bits		1 K × 8 bits
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits				
	Minimum execution time: 1.1 to 17.6 µs at 3.58 MHz, 61 µs at 32.768 kHz Interrupt processing time: 10 to 160 µs at 3.58 MHz, 562.5 µs at 32.768 kHz		Minimum instruction execution time: 0.6 to 9.6 µs at 7.16 MHz, 61 µs at 32.768 kHz Interrupt processing time: 5.4 to 86.4 µs at 7.16 MHz, 562.5 µs at 32.768 kHz		
Ports	Output ports (N-ch open-drain): 5 Output ports (CMOS): 8 I/O ports (CMOS): 24 (16 ports also serve as peripherals.) Total: 37				
8/16-bit timer/ counter	8 bits × 2 ch or 16 bits × 1 ch, capable of rectangular wave output One clock selectable from four operation clocks (one external shift clock, three internal shift clocks: 2.2 µs, 35.2 µs, 563.2 µs; when operating at 3.58 MHz)				
8-bit serial I/O	8 bits LSB/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 2.2 µs, 8.8 µs, 35.2 µs; when operating at 3.58 MHz)				
DTMF generator	All ITU-T (the old name: CCITT) tones selectable as output Fixed to oscillation frequency(3.58 MHz)		All ITU-T (the old name: CCITT) tones selectable as output Selectable oscillation frequency(3.58 MHz or 7.16 MHz)		
External interrupt 1	3 independent channels (selectable edge, interrupt vector, source flag) Rising/falling/both edges selectable Used also for wake-up from the watch/stop/sleep mode. (Edge detection is also permitted in the watch/stop mode.)				
External interrupt 2 (wake-up)	8 independent channels (“L” level interrupt) Used also for wake-up from the watch/stop/sleep mode. (Edge detection is also permitted in the watch/stop mode.)				
Standby mode	Sleep mode, stop mode, watch mode, and subclock mode				
Process	CMOS				
Operating voltage*	2.2 V to 6.0 V	2.7 V to 6.0 V	2.2 V to 6.0 V	2.7 V to 6.0 V	
EPROM for use					MBM27C256A -20TVM

* : Varies with conditions such as the operating frequency and the assurance range for the DTMF generator.(See “■ Electrical Characteristics.”)

MB89170/170A Series

Part number / Item	MB89173L	MB89P174L
Classification	Mass-produced product (mask ROM product)	
ROM size	8 K × 8 bits (internal mask ROM)	12 K × 8 bits (internal mask ROM)
RAM size	384 × 8 bits	512 × 8 bits
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits	
	Minimum instruction execution time: 0.6 to 9.6 µs at 7.16 MHz, 61 µs at 32.768 kHz Interrupt processing time: 5.4 to 86.4 µs at 7.16 MHz, 562.5 µs at 32.768 kHz	
Ports	Output ports (N-ch open-drain): 5 Output ports (CMOS): 8 I/O ports (CMOS): 24 (16 ports also serve as peripherals.) Total: 37	
8/16-bit timer/ counter	8 bits × 2 ch or 16 bits × 1 ch, capable of rectangular wave output One clock selectable from four operation clocks (one external shift clock, three internal shift clocks: 2.2 µs, 35.2 µs, 563.2 µs; when operating at 3.58 MHz)	
8-bit serial I/O	8 bits LSB/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 2.2 µs, 8.8 µs, 35.2 µs; when operating at 3.58 MHz)	
DTMF generator	—	
External interrupt 1	3 independent channels (selectable edge, interrupt vector, source flag) Rising/falling/both edges selectable Used also for wake-up from the stop/sleep mode.	
External interrupt 2 (wake-up)	8 independent channels (“L” level interrupt) Used also for wake-up from the stop/sleep mode.	
Standby mode	Sleep mode, stop mode	
Process	CMOS	
Operating voltage*	2.2 V to 6.0 V	
EPROM for use		

* : Varies with conditions such as the operating frequency and the assurance range for the DTMF generator.(See “■ Electrical Characteristics.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89173 MB89P173 MB89174A MB89P175A MB89173L MB89174L	MB89PV170A
FPT-48P-M16	○	×
MQP-48C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used.

2. Current Consumption

In the case of the MB89PV170A, added is the current consumed by the EPROM which is connected to the top socket.

3. Mask Options

Functions that can be selected as options and how to designate these options vary with the product.

Before using options, check "■ Mask Options."

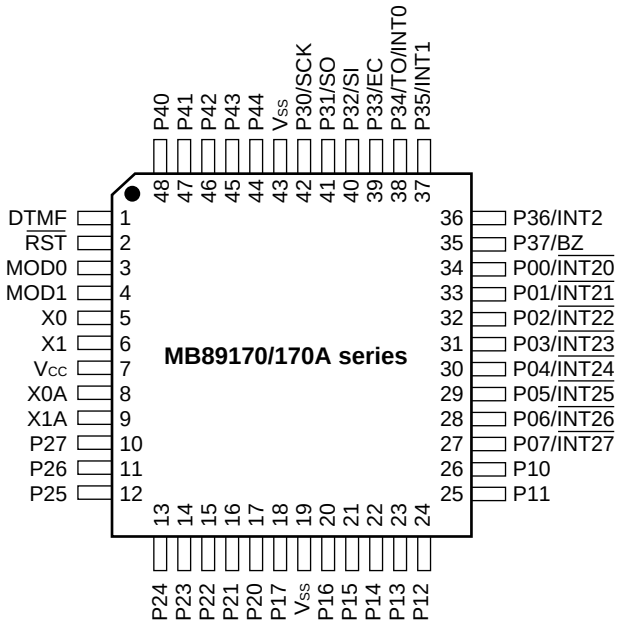
Take particular care on the following points:

- Pull-up resistor option cannot be set for P40 to P44 on the MB89P175A.
- Each option is fixed on the MB89PV170A.

MB89170/170A Series

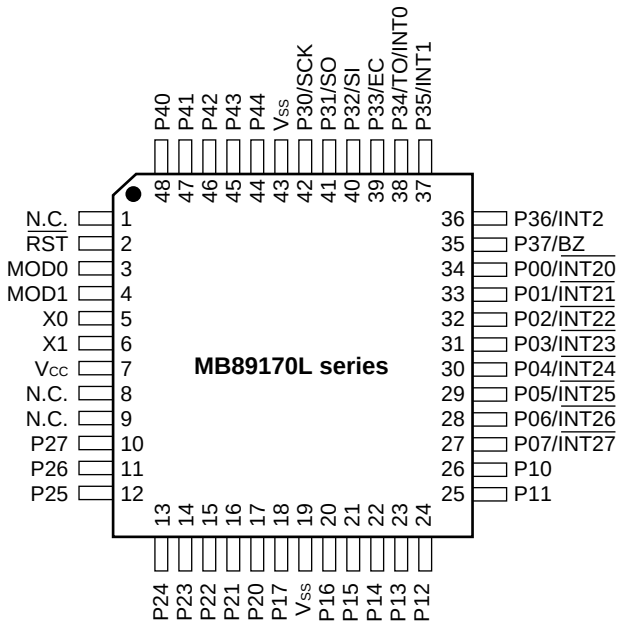
■ PIN ASSIGNMENT

(Top view)

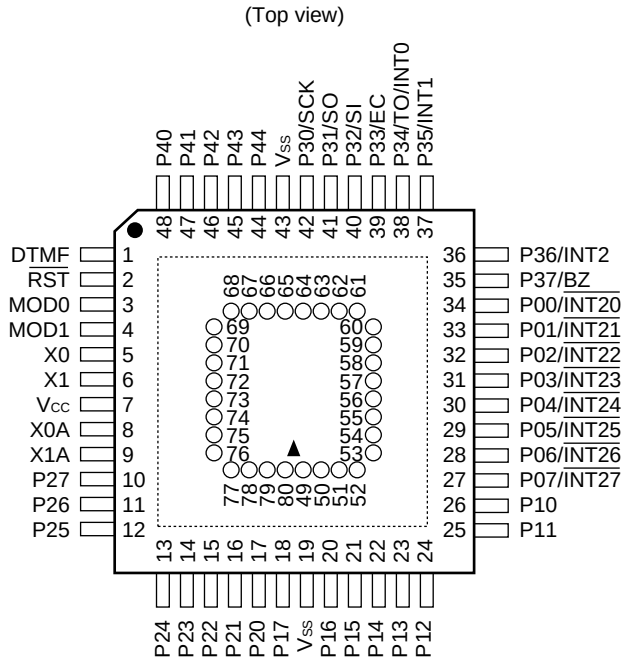


(FPT-48P-M16)

(TOP VIEW)



(FPT-48P-M16)



(MQP-48C-P01)

- **Pin assignment on package top (MB89PV170A only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V_{PP}	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no. QFP*1 MQFP*2	Pin name	Circuit type	Function
5	X0	A	Main clock crystal oscillator pins
6	X1		
8	X0A	B	Subclock oscillation pins (32.768 kHz)
9	X1A		
3	MOD0	C	Operation mode selecting pins Connect directly to V_{CC} or V_{SS}.
4	MOD1		
2	$\overline{RST}$	D	Reset I/O pin This pin is of an N-ch open-drain output type with pull-up resistor and of hysteresis input type. "L" is output from this pin by an internal reset source (optional function). The internal circuit is initialized by the input of "L".
34 to 27	P00/$\overline{INT20}$ to P07/$\overline{INT27}$	E	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt input is a hysteresis input.
26 to 20, 18	P10 to P17	F	General-purpose I/O ports
17 to 10	P20 to P27	H	General-purpose output ports
42	P30/SCK	G	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O. This port is of hysteresis input type.
41	P31/SO	G	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O. This port is of hysteresis input type.
40	P32/SI	G	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is of hysteresis input type.
39	P33/EC	G	General-purpose I/O port Also serves as an external clock input for a 8-bit timer/counter. This port is of hysteresis input type.
38	P34/TO/INT0	G	General-purpose I/O port Also serves as the overflow output for the 8-bit timer/counter and an external interrupt 1 input. This port is of hysteresis input type.
36, 37	P36/INT2, P35/INT1	G	General-purpose I/O ports Also serve as an external interrupt 1 input. These ports are of hysteresis input type.

(Continued)

*1: FPT-48P-M16
*2: MQP-48C-P01

Notes: On the MB89170L series, DTMF pin (Pin No.:1), X0A pin (Pin No.:8) and X1A pin (Pin No.:9) are N.C. pins.

(Continued)

Pin no. QFP*1 MQFP*2	Pin name	Circuit type	Function
35	P37/BZ	G	General-purpose I/O port Also serves as a buzzer output. This port is of hysteresis input type.
48 to 44	P40 to P44	I	N-ch open-drain output ports
1	DTMF	J	DTMF signal output pin
7	V_{CC}	—	Power supply pin
19, 43	V_{SS}	—	Power supply (GND) pin

*1: FPT-48P-M16
*2: MQP-48C-P01

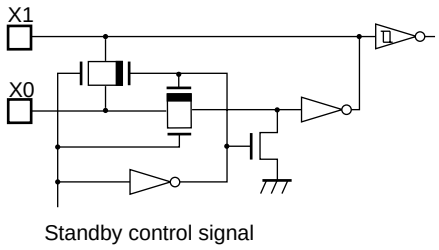
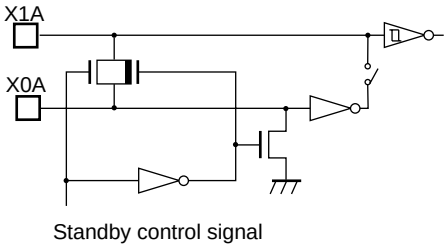
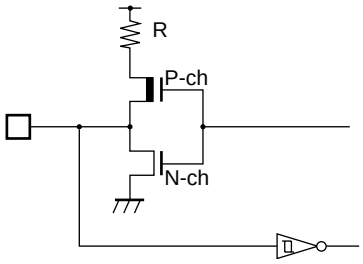
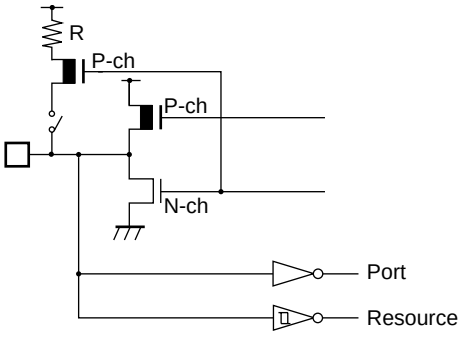
Notes: On the MB89170L series, DTMF pin (Pin No.:1), X0A pin (Pin No.:8) and X1A pin (Pin No.:9) are N.C. pins.

- **External EPROM pins (the MB89PV170A only)**

Pin no. MQFP*	Pin name	I/O	Function
49	V_{PP}	O	"H" level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
61 62 63	O1 O2 O3	I	Data input pins
64	V_{SS}	O	Power supply (GND) pin
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins
70	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
71	A10	O	Address output pin
73	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins
80	V_{CC}	O	EPROM power supply pin
56 57 72 74	N.C.	—	Internally connected pin Be sure to leave them open.

* : MQP-48C-P01

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main clock • Oscillation feedback resistor of approximately 1 MΩ/5 V
B		Subclock • Oscillation feedback resistor of approximately 4.5 MΩ/5 V • When single clock mode is selected, the switch is open.
C		
D		• Output pull-up resistor (P-ch) of approximately 50 kΩ/5 V • Hysteresis input
E		• CMOS output • CMOS input • Hysteresis input • Pull-up resistor optional

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MB89170/170A Series

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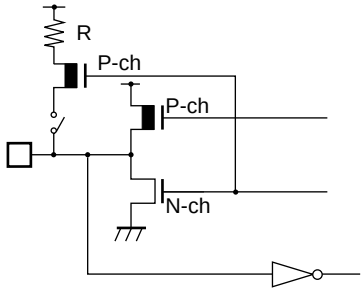
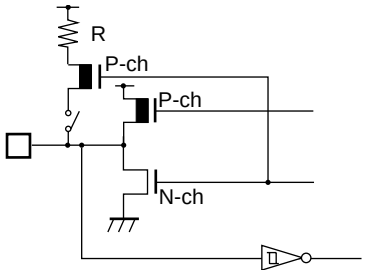
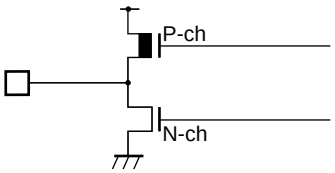
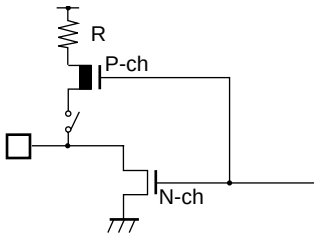
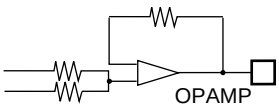
Type	Circuit	Remarks
F		• CMOS output • CMOS input • Pull-up resistor optional
G		• CMOS output • Hysteresis input • Pull-up resistor optional
H		• CMOS output
I		• N-ch open-drain output • Pull-up resistor optional
J		• DTMF analog output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between V_{CC} to V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damaged elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down registor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although operating is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P173 AND MB89P175A

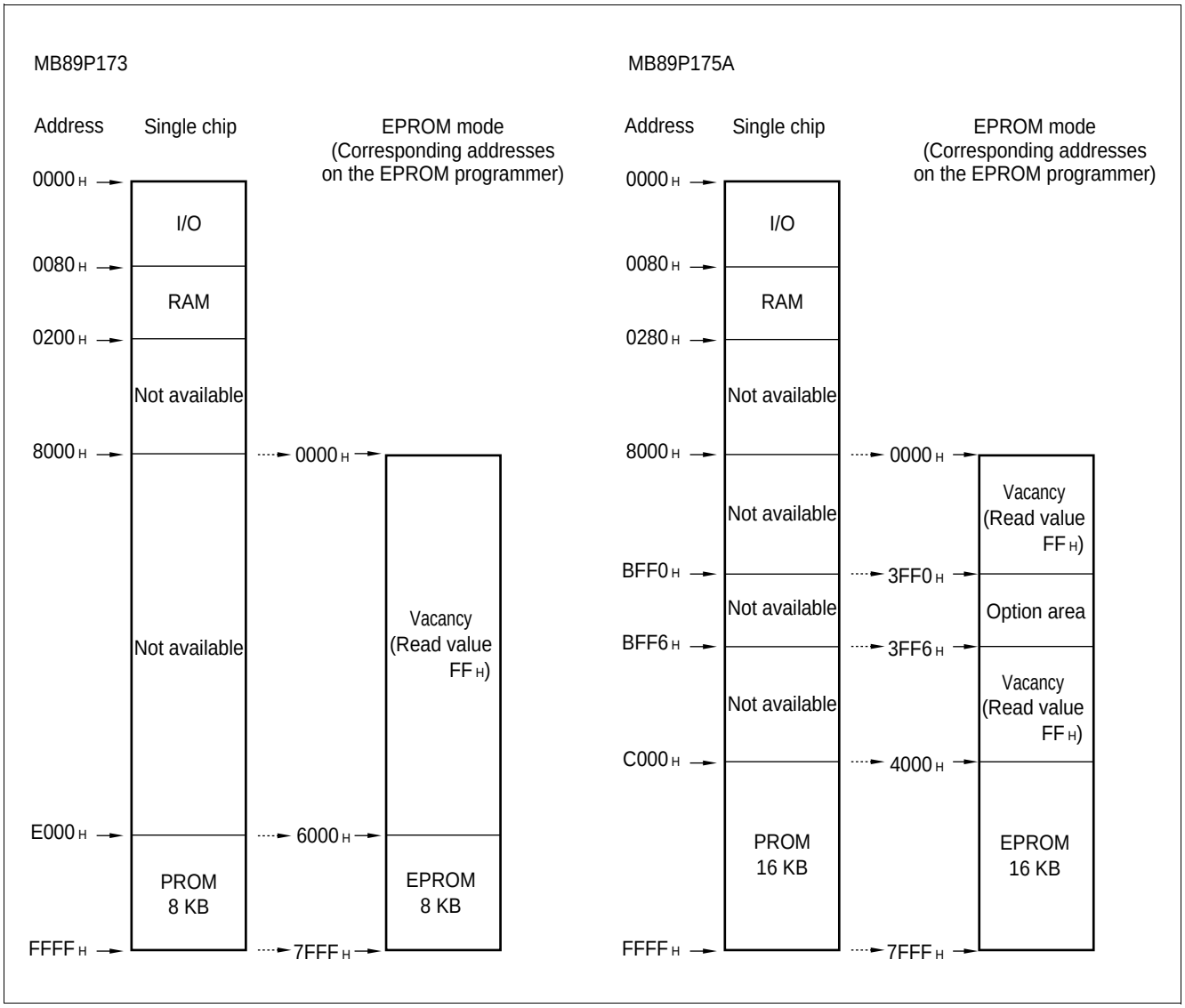
The MB89P173 is an OTPROM (one-time PROM) versions of the MB89170/170L series, and the MB89P175A is of the MB89170A/170L series.

1. Features

- 8-Kbyte (MB89P173), 16-Kbyte (MB89P175A) PROM on chip
- Options can be set using the EPROM programmer (MB89P175A only).
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 8-Kbyte PROM,16-Kbyte PROM and option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P173 and MB89P175A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure (MB89P173)**

(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 6000_H to $7FFF_H$ (note that addresses $E000_H$ to $0FFFF_H$ while operating as a single chip correspond to 6000_H to $7FFF_H$ in EPROM mode).

(3) Program the data to the EPROM with the EPROM programmer.

- **Programming procedure (MB89P175A)**

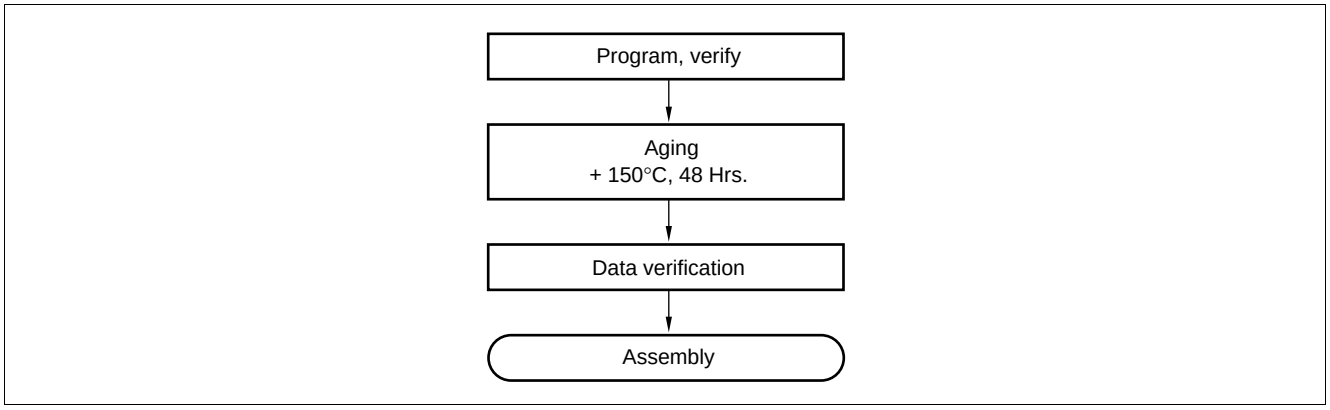
(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$ (note that addresses $C000_H$ to $0FFFF_H$ while operating as a single chip assign to 4000_H to $7FFF_H$ in EPROM mode).
Load option data into addresses $3FF0_H$ to $3FF6_H$ of the EPROM programmer. (For information about each corresponding option, see “7. Setting OTPROM Options (MB89P175A Only).”)

(3) Program the data to the EPROM with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

Due to its nature, bit programming test can’t be conducted as Fujitsu delivery test. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Part number	Package	Compatible socket adapter Sun Hayato Co., Ltd.
MB89P175A	QFP-48P	ROM-48QF-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

7. Setting OTPROM Options (MB89P175A Only)

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Clock mode select 1: 1 clock 0: 2 clocks	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization time 00 $2^3/F_{CH}$ 01 $2^{12}/F_{CH}$	 10 $2^{16}/F_{CH}$ 11 $2^{18}/F_{CH}$
3FF1H	P07 Pull-up 1: Yes 0: No	P06 Pull-up 1: Yes 0: No	P05 Pull-up 1: Yes 0: No	P04 Pull-up 1: Yes 0: No	P03 Pull-up 1: Yes 0: No	P02 Pull-up 1: Yes 0: No	P01 Pull-up 1: Yes 0: No	P00 Pull-up 1: Yes 0: No
3FF2H	P17 Pull-up 1: Yes 0: No	P16 Pull-up 1: Yes 0: No	P15 Pull-up 1: Yes 0: No	P14 Pull-up 1: Yes 0: No	P13 Pull-up 1: Yes 0: No	P12 Pull-up 1: Yes 0: No	P11 Pull-up 1: Yes 0: No	P10 Pull-up 1: Yes 0: No
3FF3H	P37 Pull-up 1: Yes 0: No	P36 Pull-up 1: Yes 0: No	P35 Pull-up 1: Yes 0: No	P34 Pull-up 1: Yes 0: No	P33 Pull-up 1: Yes 0: No	P32 Pull-up 1: Yes 0: No	P31 Pull-up 1: Yes 0: No	P30 Pull-up 1: Yes 0: No
3FF4H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF5H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF6H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

Note: Each bit is set to ‘1’ as the initialized value, therefore the pull-up option is selected.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

2. Programming Socket Adapter

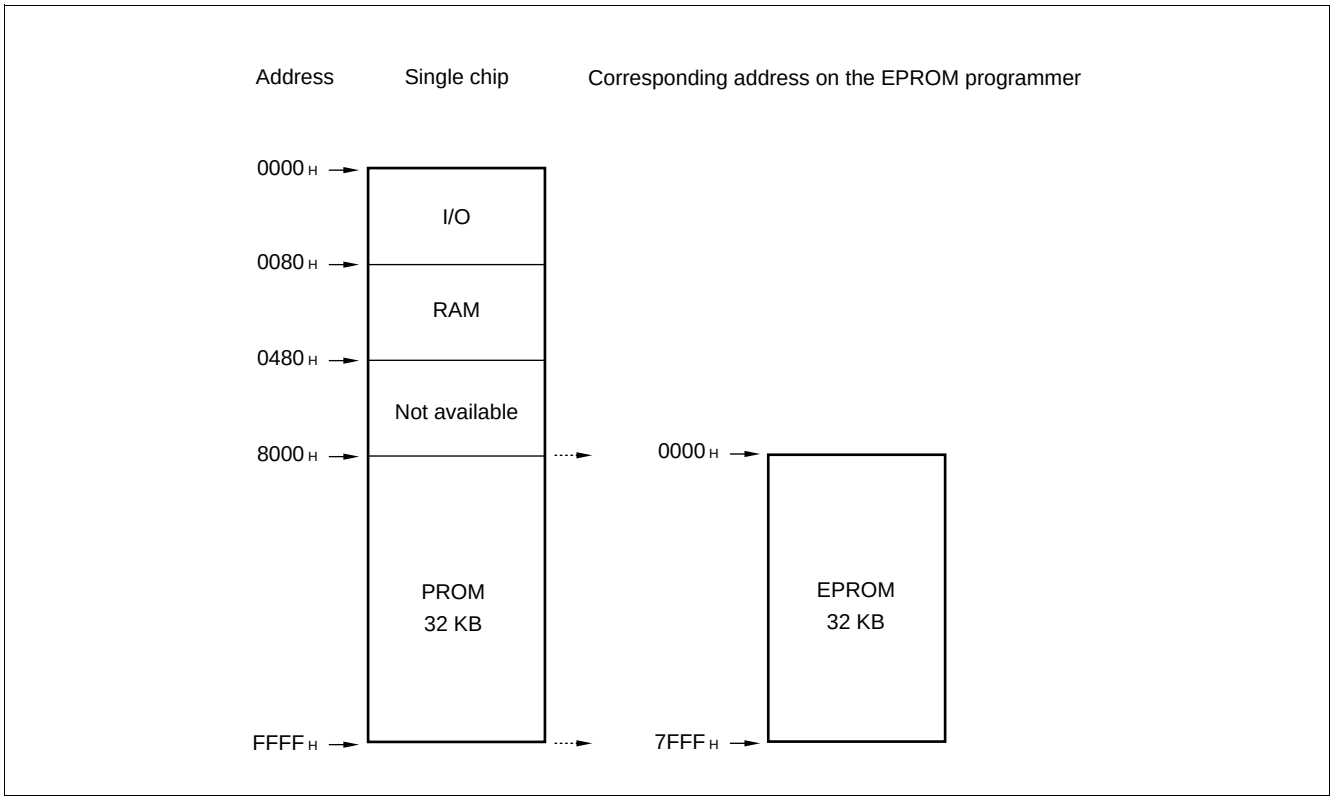
To program to the EPROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Socket adapter part number
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

3. Memory Space

Memory space in each mode, such as 32-Kbyte EPROM, is diagrammed below.



4. Programming to the EPROM

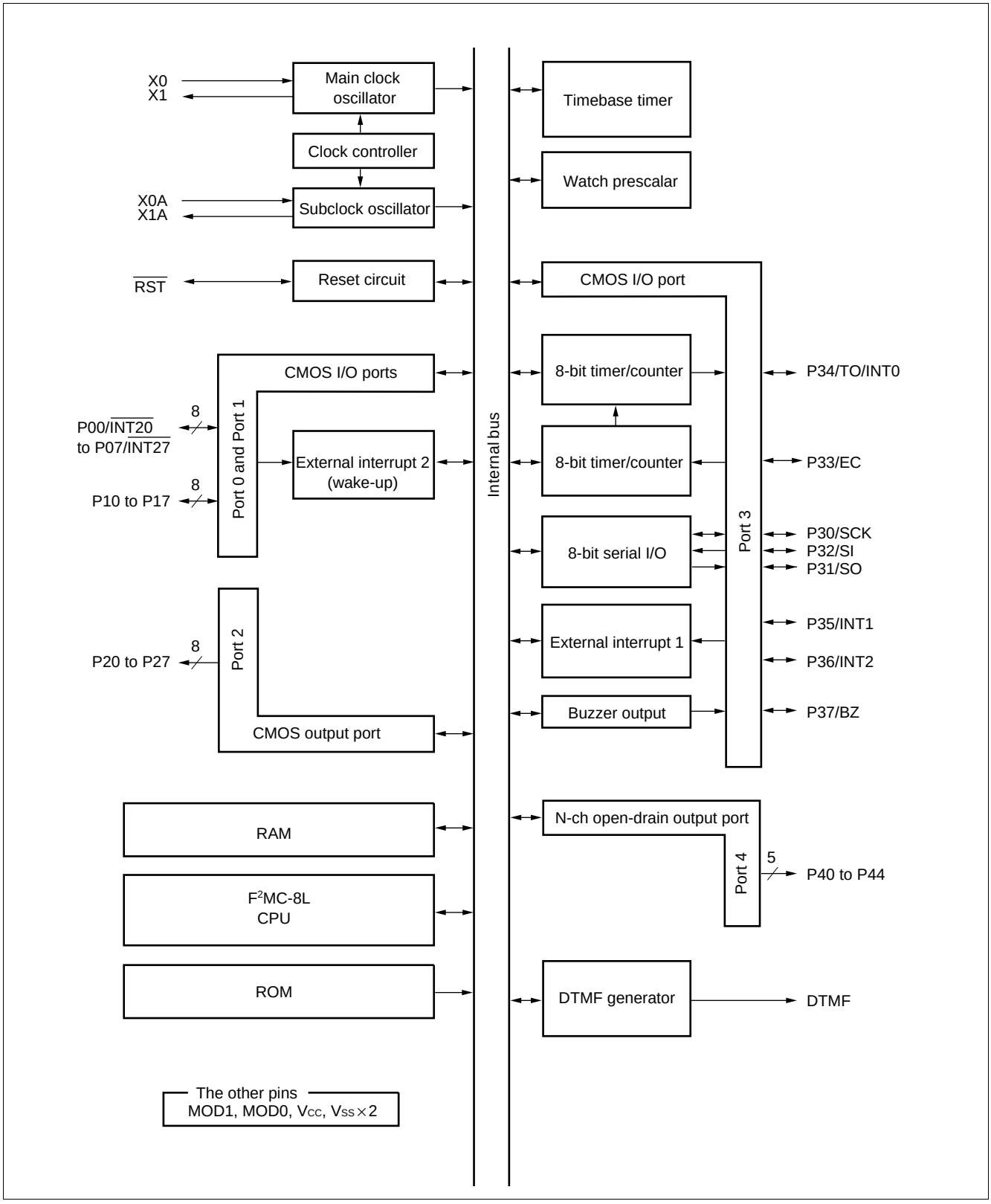
(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

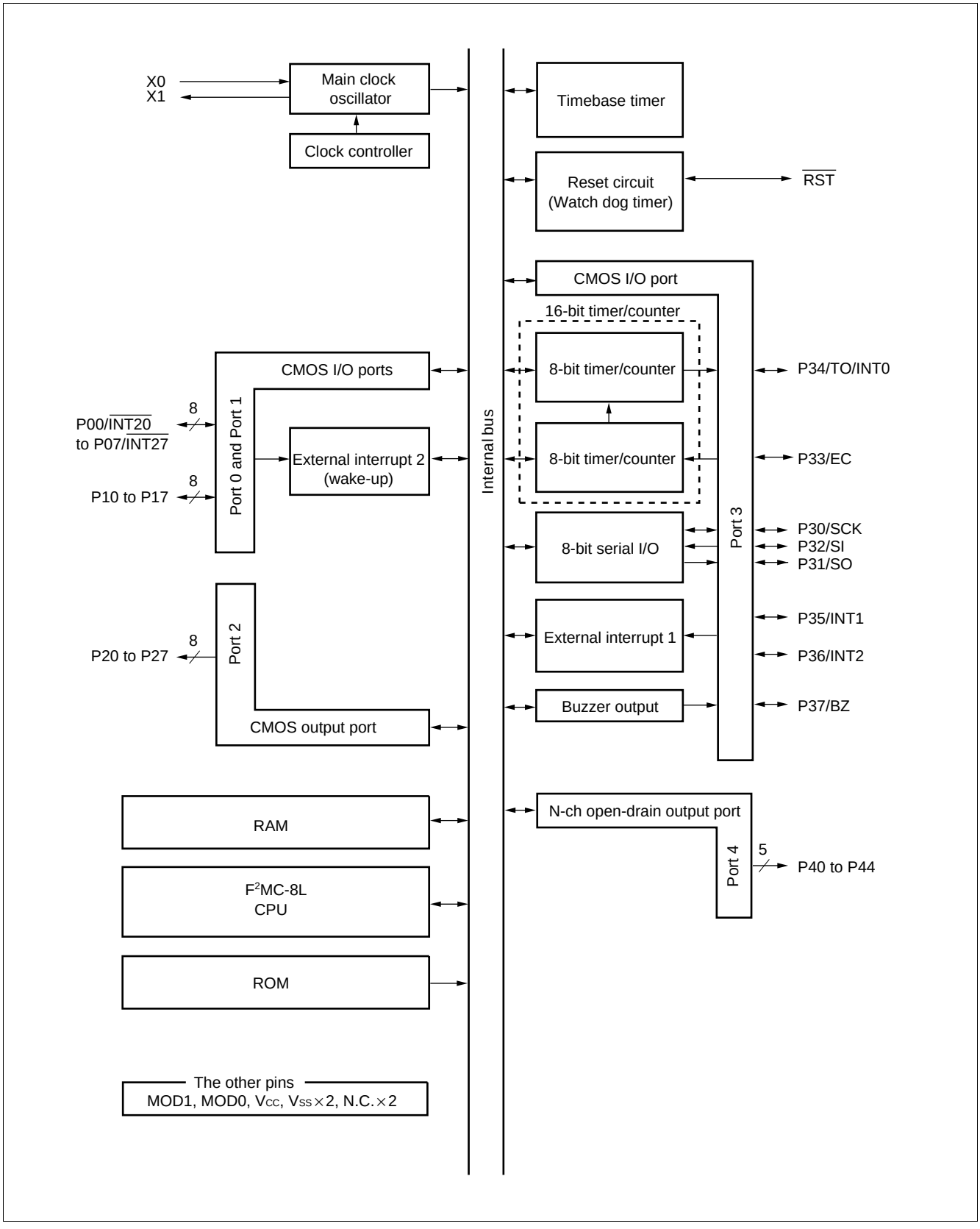
(3) Program with the EPROM programmer.

■ BLOCK DIAGRAM

1. MB89170/170A series



2. MB89170L series

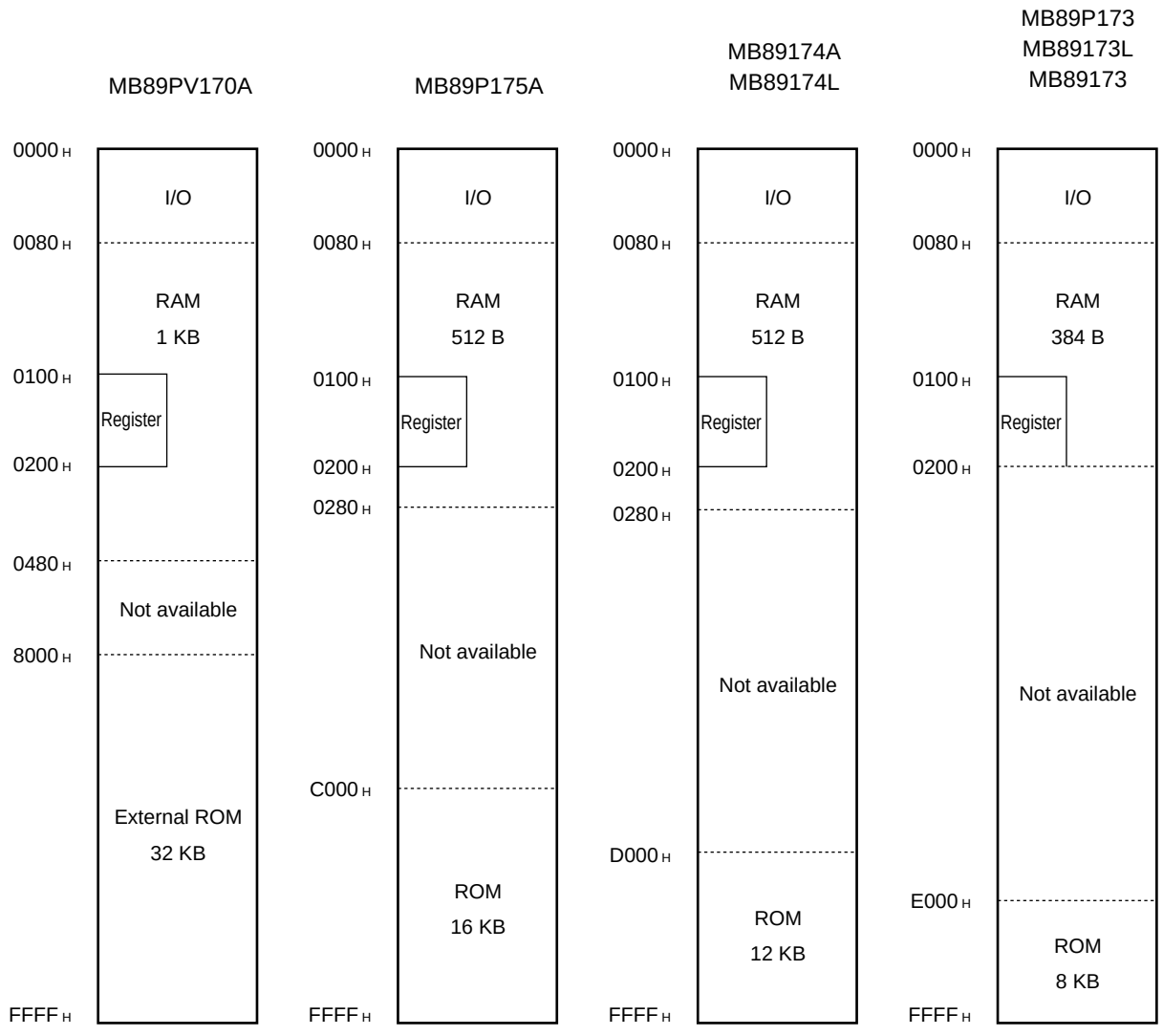


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89170/170A/170L series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end of I/O area, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89170/170A/170L series is structured as illustrated below.

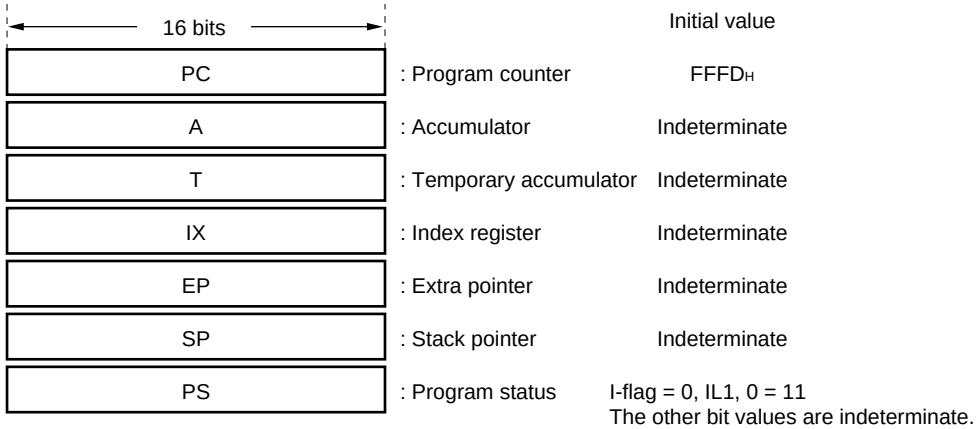
Memory Space



2. Registers

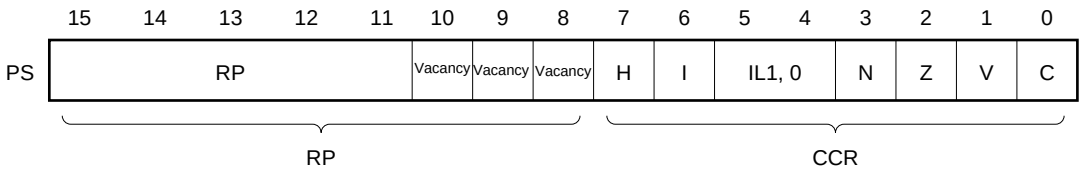
The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose memory registers. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which is used for arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP) :	A 16-bit pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit pointer for indicating a stack area
Progam status (PS) :	A 16-bit register for storing a register pointer, a condition code



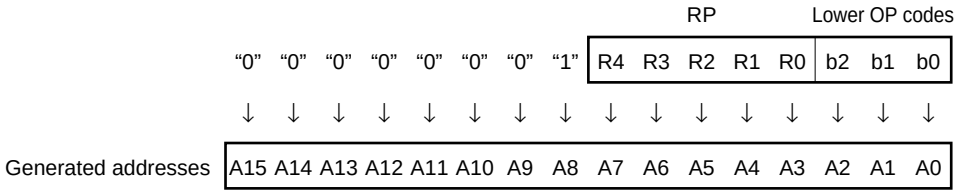
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

Z-flag: Set to '1' when an arithmetic operation results in '0'. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

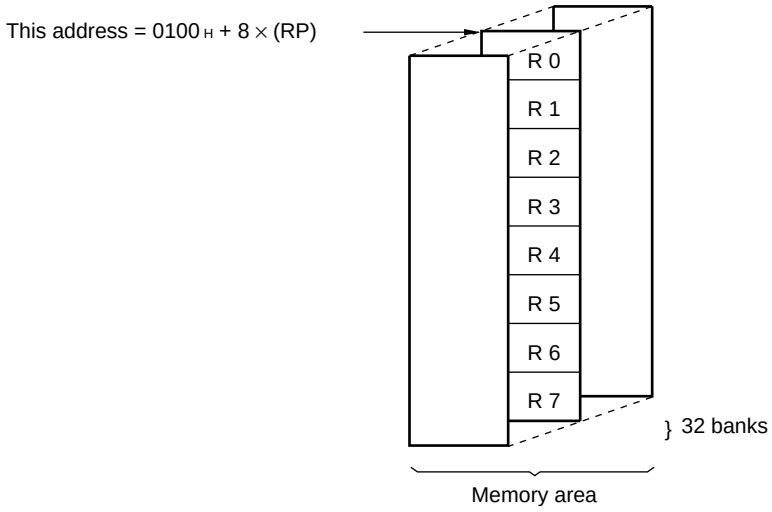
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose register: An 8-bit register for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89170/170A/170L series . The bank currently in use is indicated by the register bank pointer(RP).

Register Bank Configuraiton



■ I/O MAP

1. MB89170/170A series

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H			Vacancy
06_H			Vacancy
07_H	(R/W)	SYCC	System clock control register
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog control register
$0A_H$	(R/W)	TBTC	Timebase timer control register
$0B_H$	(R/W)	WPCR	Watch prescaler control register
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	(R/W)	DDR3	Port 3 data direction register
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	BZCR	Buzzer register
10_H			Vacancy
11_H			Vacancy
12_H			Vacancy
13_H			Vacancy
14_H			Vacancy
15_H			Vacancy
16_H			Vacancy
17_H			Vacancy
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$	(R/W)	SMR	Serial mode register
$1D_H$	(R/W)	SDR	Serial data register
$1E_H$			Vacancy
$1F_H$			Vacancy

(Continued)

(Continued)

Address	Read/write *	Register name	Register description
20_H	(R/W)	DTMC	DTMF control register
21_H	(R/W)	DTMD	DTMF data register
22_H			Vacancy
23_H	(R/W)	EIC1	External interrupt control register 1
24_H	(R/W)	EIC2	External interrupt control register 2
25_H to 31_H			Vacancy
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

* R/W: Readable and writable
  R: Read only
  W: Write only

Note: Do not use vacancies.

2. MB89170L series

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H			Vacancy
06_H			Vacancy
07_H	(R/W)	SYCC	System clock control register
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog control register
$0A_H$	(R/W)	TBTC	Timebase timer control register
$0B_H$			Vacancy
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	(R/W)	DDR3	Port 3 data direction register
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	BZCR	Buzzer register
10_H			Vacancy
11_H			Vacancy
12_H			Vacancy
13_H			Vacancy
14_H			Vacancy
15_H			Vacancy
16_H			Vacancy
17_H			Vacancy
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$	(R/W)	SMR	Serial mode register
$1D_H$	(R/W)	SDR	Serial data register
$1E_H$			Vacancy
$1F_H$			Vacancy

(Continued)

(Continued)

Address	Read/write *	Register name	Register description
20_H			Vacancy
21_H			Vacancy
22_H			Vacancy
23_H	(R/W)	EIC1	External interrupt control register 1
24_H	(R/W)	EIC2	External interrupt control register 2
25_H to 31_H			Vacancy
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

* R/W: Readable and writable
  R: Read only
  W: Write only

Note: Do not use vacancies.
As for MB89170L series, WPCR register($0B_H$), DTMC register(20_H) and DTMD register(21_H) become Vacancy.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P44
	V_{I2}	V_{SS} – 0.3	V_{CC} + 0.3	V	P40 to P44 (with pull-up option)
		V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P44 (without pull-up option)
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P40 to P44
	V_{O2}	V_{SS} – 0.3	V_{CC} + 0.3	V	P40 to P44 (with pull-up option)
		V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P44 (without pull-up option)
“L” level maximum output current	I_{OL}	—	10	mA	
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	20	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–10	mA	
“H” level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–25	mA	
“H” level total average output current	ΣI_{OHAV}	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

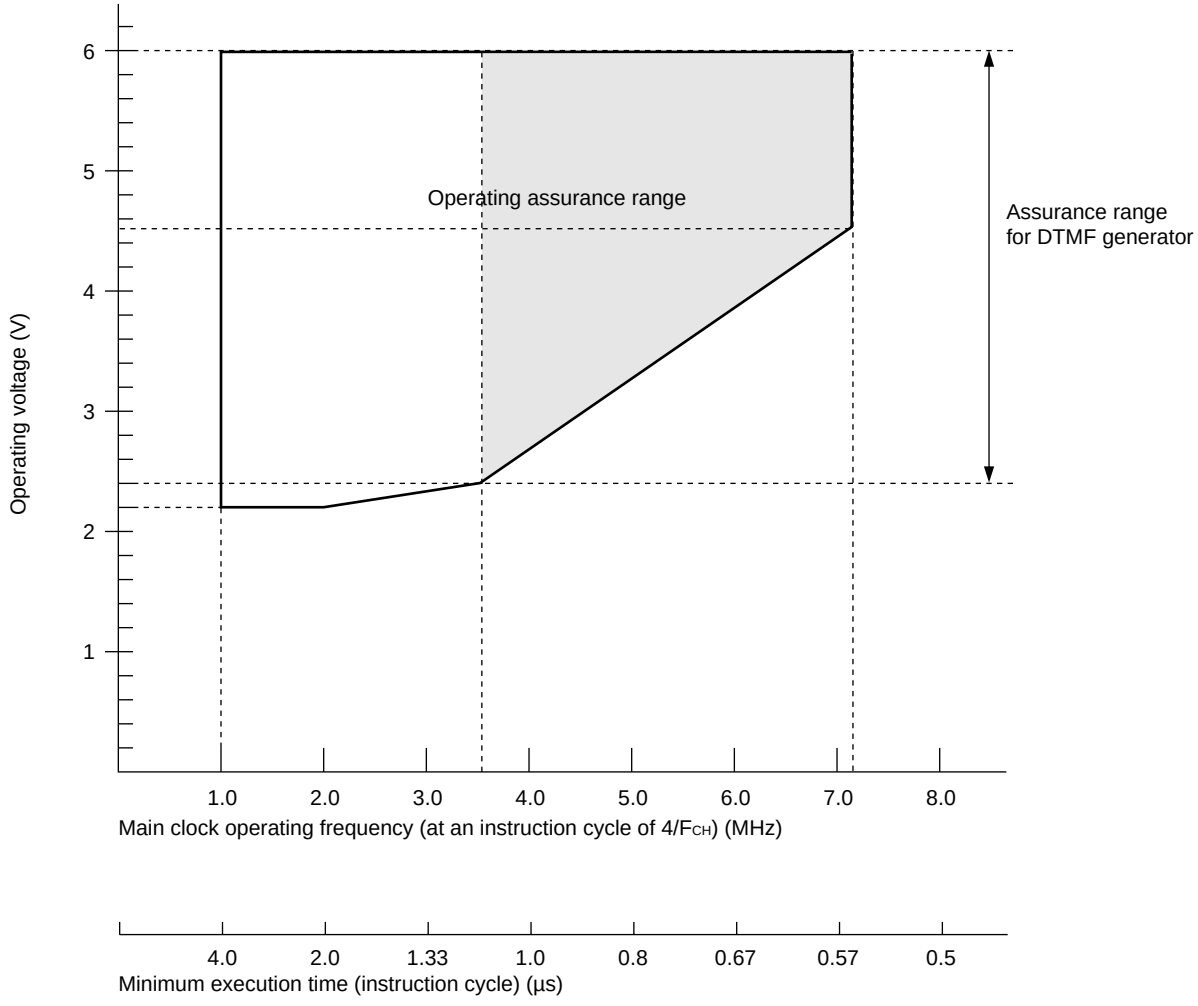
2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89174A/173/174L/173L
		2.7*	6.0*	V	Normal operation assurance range* MB89PV170A/P175A/P173
		1.5	6.0	V	Retains the RAM state in the stop mode
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, instruction cycle, and the assurance range for the DTMF generator. See Figure 1 and “(7) Electrical Characteristics of DTMF Generator” in “4. AC characteristics.”

Figure 1 Operating Voltage vs. Main Clock Operating Frequency(MB89170/170A series)



Note: The shaded area is assured only for the MB89170A series.

Figure 2 Operating Voltage vs. Main Clock Operating Frequency(MB89170L series)

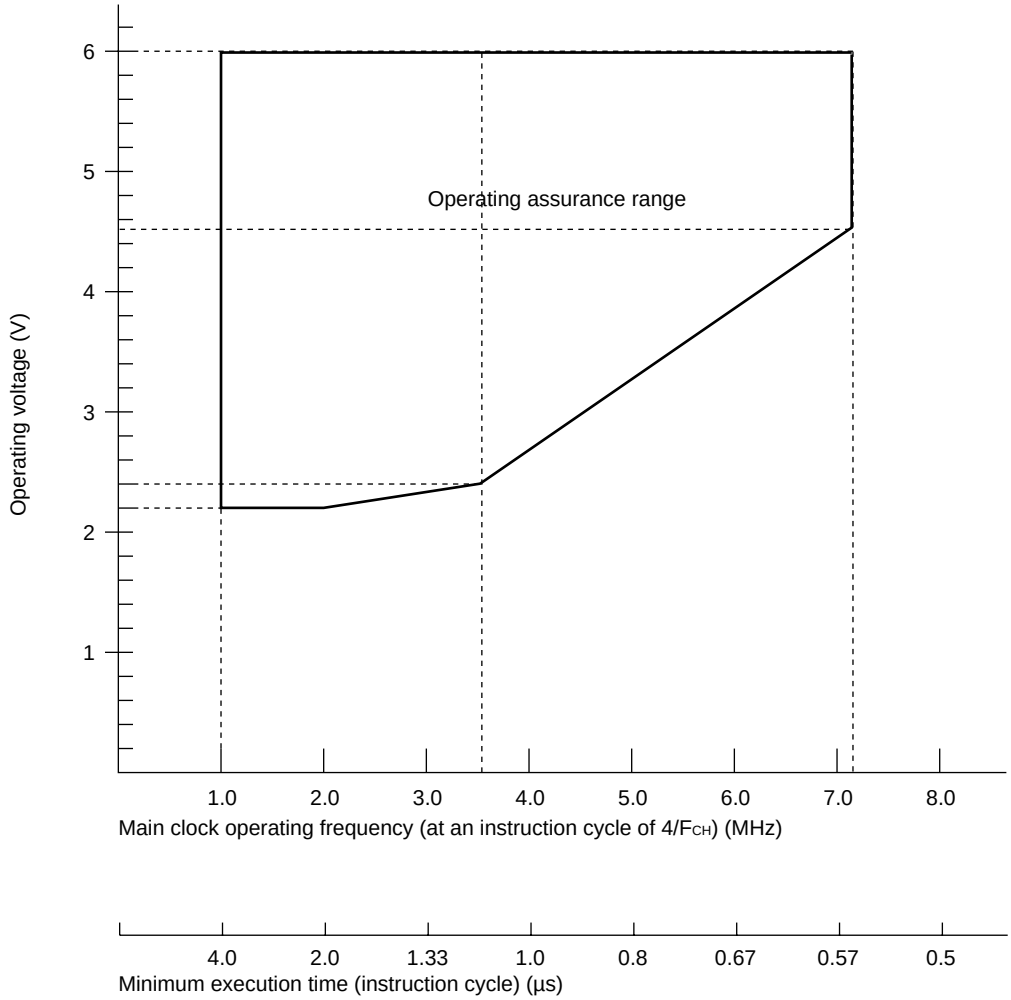


Figure 1 and figure 2 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, $\overline{INT20}$ to $\overline{INT27}$		0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, PI0 to PI7		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, P30 to P37, $\overline{INT20}$ to $\overline{INT27}$		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin applied voltage	V_D	P40 to P44		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37	I_{OH} = –2.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P44	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.6	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P44, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P44, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor

(Continued)

(Continued)

(V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply voltage*	I_{CC}	V_{CC} (when DTMF is not operating)	V_{CC} = 5.0 V F_{CH} = 3.58 MHz • Main clock operation mode • Highest gear speed	—	3.5	8	mA	MB89173/ 174A/173L/ 174L
				—	6.5	10	mA	MB89P173/ P175A
	I_{CCS1}		V_{CC} = 5.0 V F_{CH} = 3.58 MHz • Main clock sleep mode • Highest gear speed	—	2	5	mA	
	I_{CCS2}		V_{CC} = 3.0 V F_{CL} = 32.768 kHz • Subclock sleep mode	—	25	50	µA	
	I_{CCH}		T_A = +25°C • Subclock stop mode • Main clock stop mode in single clock system	—	—	1	µA	
	I_{CSB}		V_{CC} = 3.0 V F_{CL} = 32.768 kHz • Subclock operation mode	—	50	100	µA	MB89173/ 174A
				—	1	3	mA	MB89P173/ P175A
	I_{CCT}		V_{CC} = 3.0 V • Watch mode	—	—	15	µA	
	I_D	V_{CC} (when DTMF is operating)	V_{CC} = 5.0 V F_{CH} = 3.58 MHz • Main clock operation mode • Highest gear speed	—	5.5	10	mA	MB89173/ 174A
				—	8.5	13	mA	MB89P173/ P175A
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}	f = 1 MHz	—	10	—	pF	

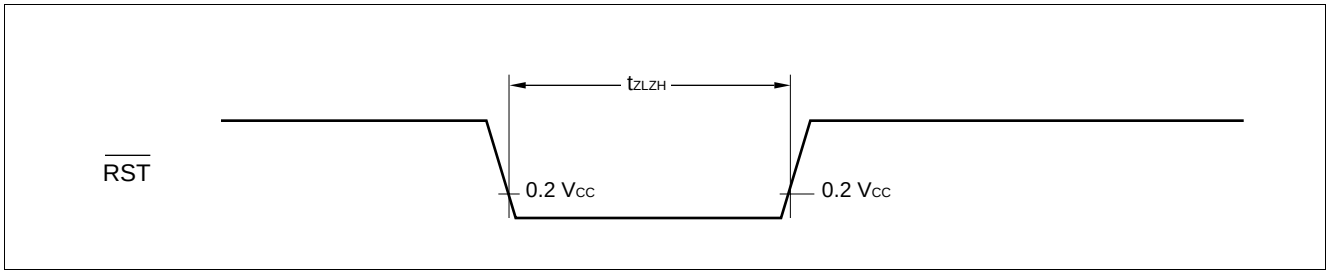
* : The power supply current is measured at the external clock.

4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

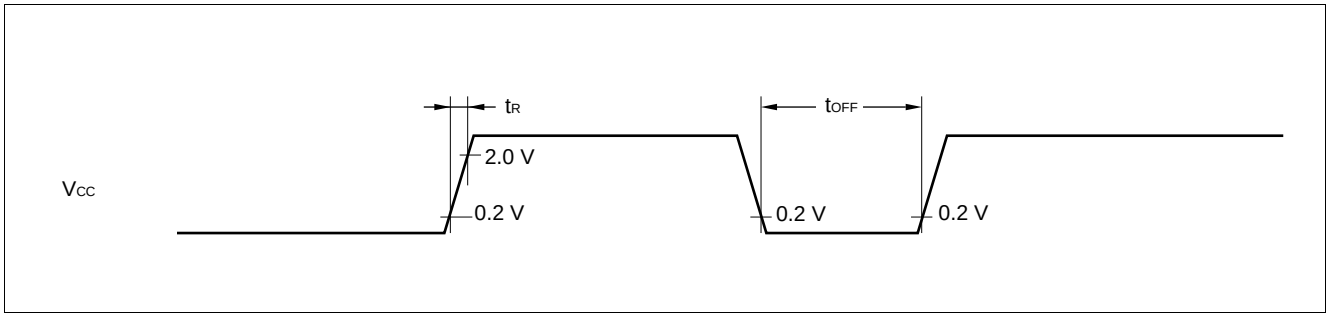


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the oscillation stabilization time selected.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

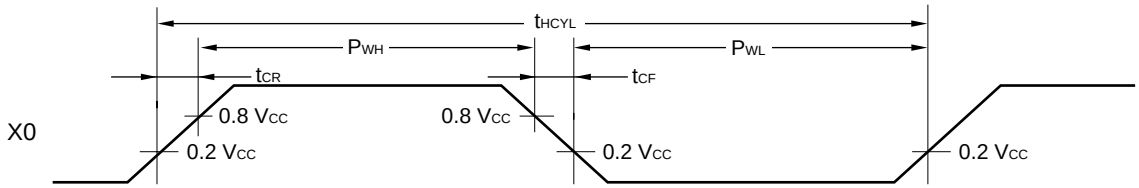


(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

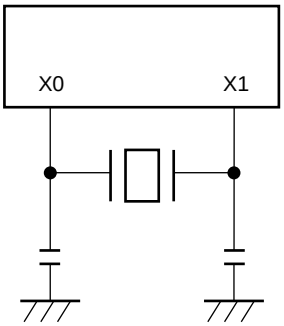
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	1	—	3.58	MHz	MB89173/ P173
				1	—	7.16	MHz	MB89174A/ P175A/ PV170A/ 173L/174L
	F_{CL}	X0A, X1A		—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1		280	—	1000	ns	MB89173/ P173
				140	—	1000	ns	MB89174A/ P175A/ PV170A/ 173L/174L
	t_{LCYL}	X0A, X1A		—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A		—	15.2	—	µs	External clock
Input clock rising/ falling time	t_{CR} t_{CF}	X0, X0A		—	—	10	ns	External clock

• **Main Clock Timing Condition**

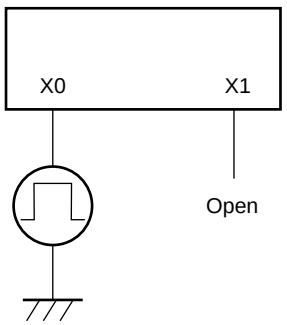


• **Main Clock Configurations**

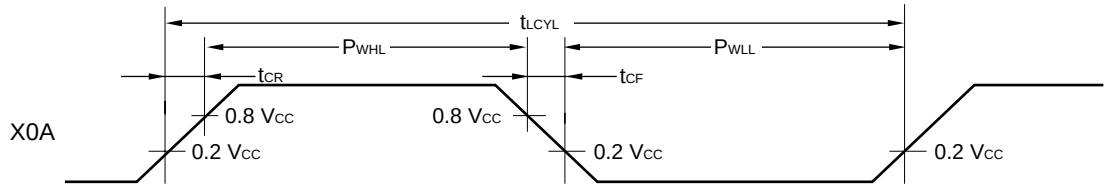
When a crystal or ceramic resonator is used



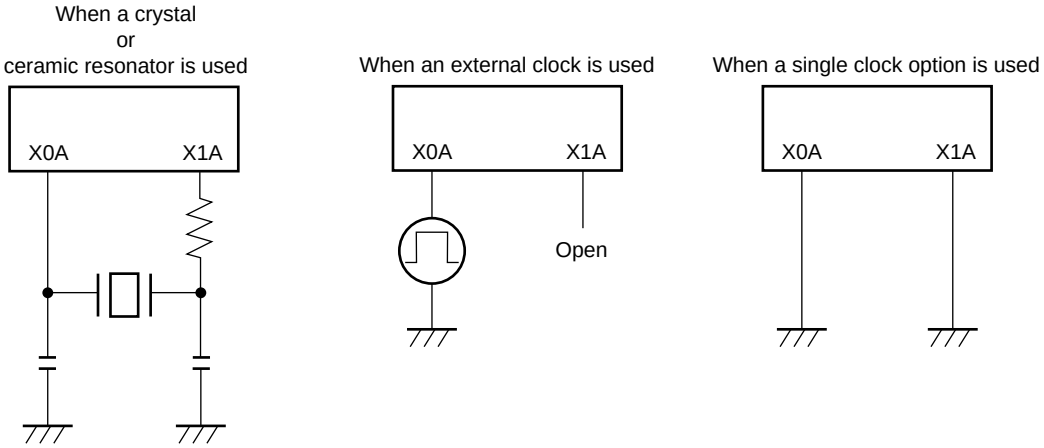
When an external clock is used



• **Subclock Timing Condition**



• **Subclock Configurations**

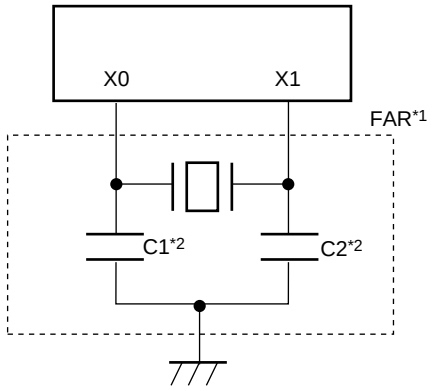


(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_C)$ t_{inst} = 1.1 µs when operating at F_C = 3.58 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz (MB89170/170A series only)

(5) Recommend Resonator Manufacturers

- **Sample Application of Piezoelectric Resonator (FAR Family) (MB89170 series only)**



*1: Fujitsu Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristics of FAR frequency (T_A = –20°C+60°C)	Loading capacitors*2
FAR-C4□A-03580-□01	3.58	±0.5%	±0.5%	Built-in

Inquiry: FUJITSU LIMITED

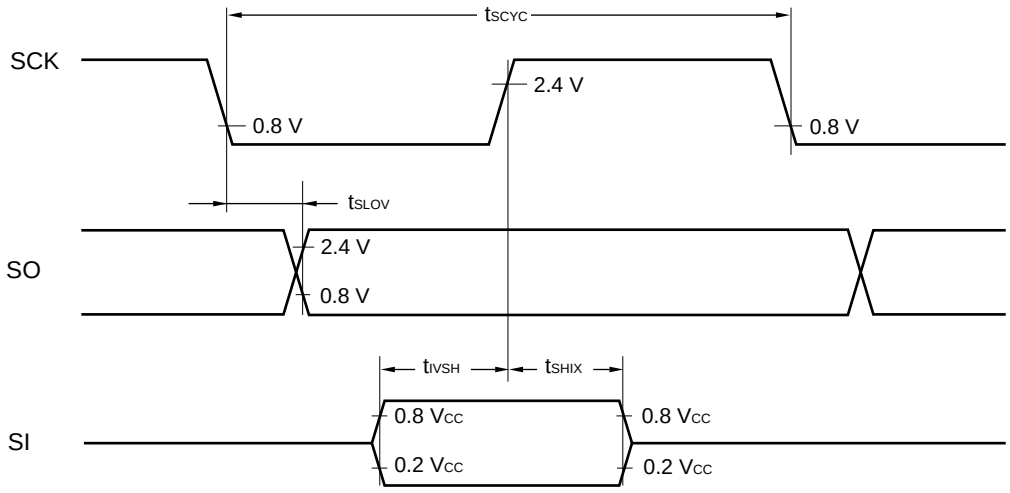
(6) Serial I/O Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

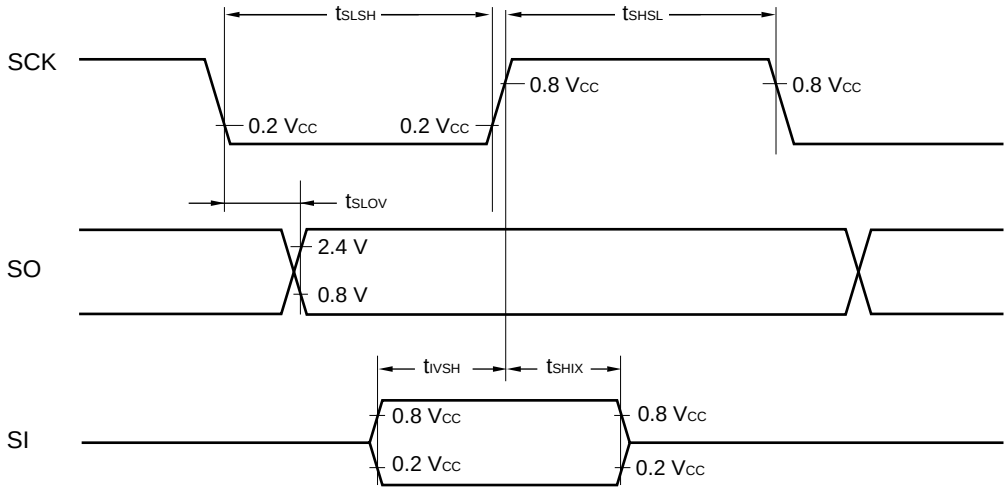
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

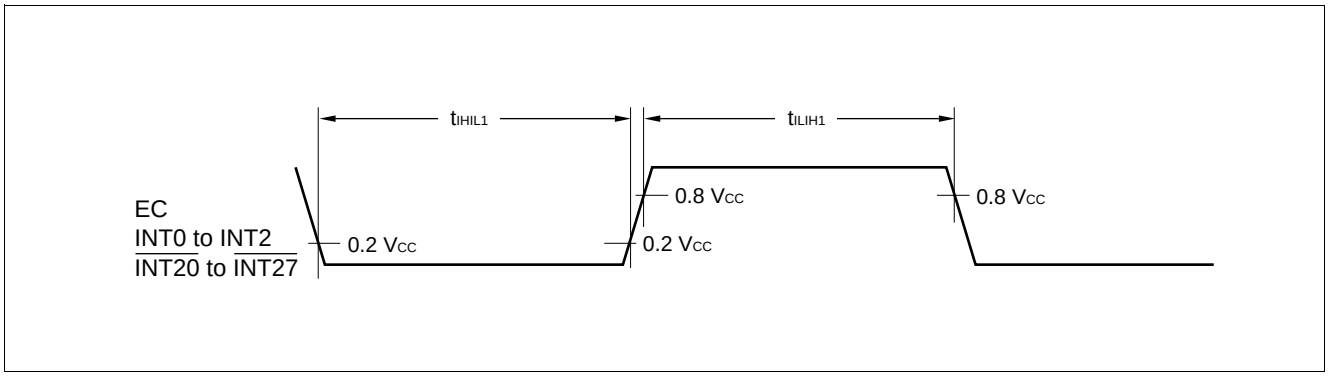


(7) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	EC, INT0 to INT2, INT20 to INT27	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



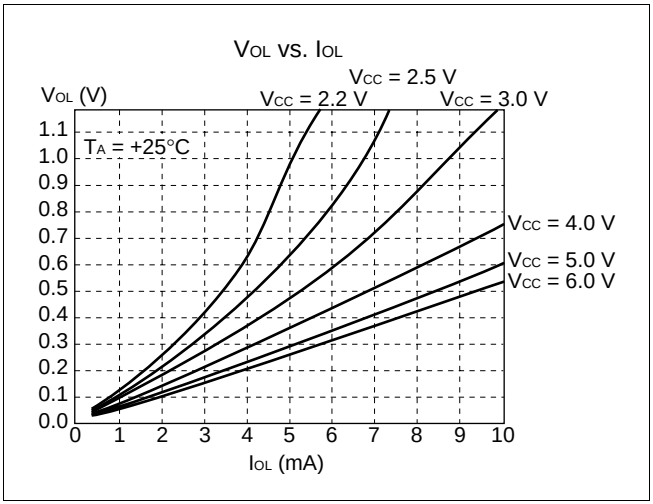
(8) Electrical Characteristics of DTMF Generator

(V_{SS} = 0.0 V, F_{CH} = 3.579545 MHz, T_A = –30°C to + 60°C)

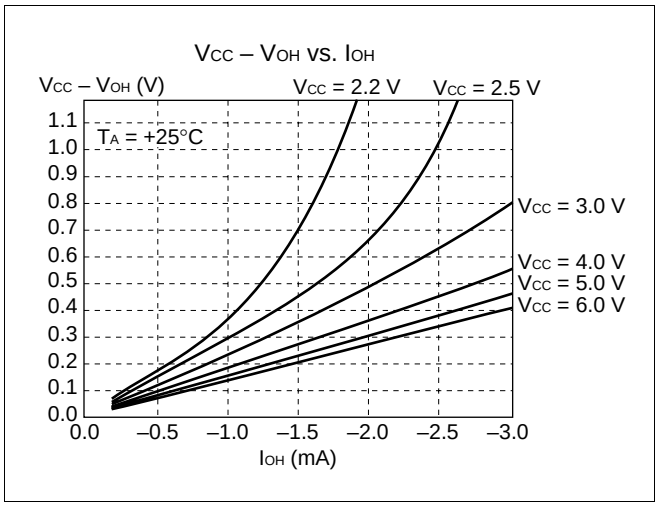
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Operating voltage range	—	—	3.0	—	6.0	V	MB89P173
			2.4	—	6.0	V	MB89173/174A/P175A
Output load requirements	R_O	V_{CC} = 4.5 V to 6.0 V	30	—	—	kΩ	Defined when the DTMF pin is connected to a pull-down resistor for the MB89P173.
		V_{CC} = 3.0 V to 4.5 V	200	—	—	kΩ	
		—	30	—	—	kΩ	Defined when the DTMF pin is connected to a pull-down resistor for the MB89173/174A/P175A
DTMF output offset voltage (at signal output)	V_{MOF}	V_{CC} = 5.0 V	—	2.4	—	V	When the DTMF pin is open for MB89P173.
			—	0.6	—	V	When the DTMF pin is open for the MB89173/174A/P175A.
DTMF output amplitude (COL single tone)	V_{MFOC}	V_{CC} = 5.0 V	450	530	600	mV_{P-P}	When DTMF pin is open.
DTMF output amplitude (ROW single tone)	V_{MFOR}	V_{CC} = 5.0 V	350	420	480	mV_{P-P}	
Difference between COL and ROW levels	R_{MF}	—	1.6	2.0	2.4	dB	

■ EXAMPLE CHARACTERISTICS

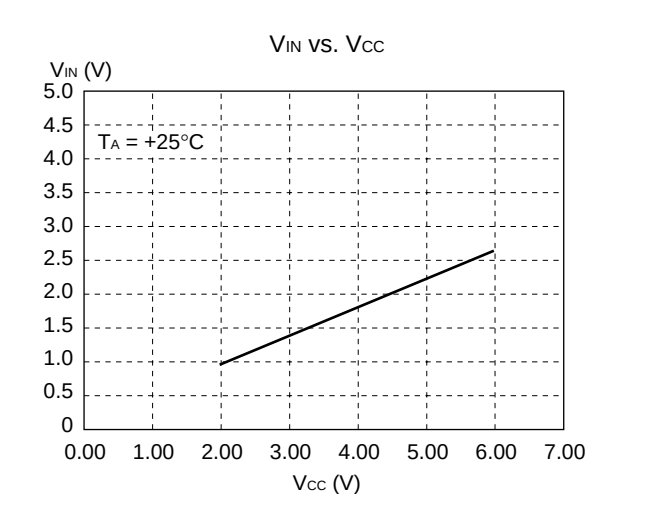
(1) “L” Level Output Voltage



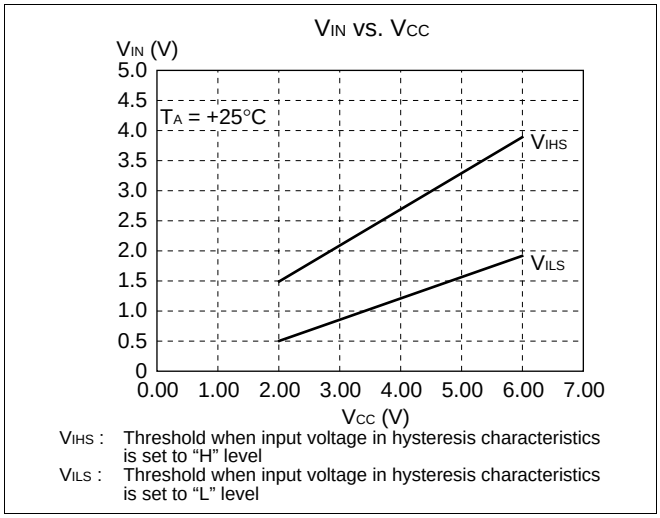
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L”ow Level Input Voltage (CMOS Input)



(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

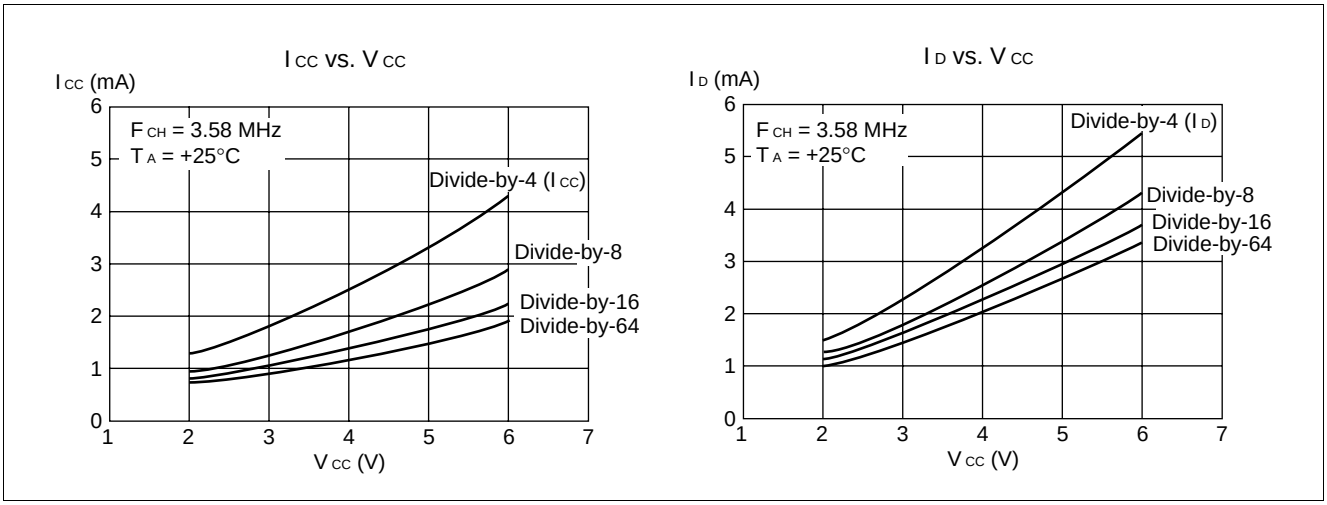


VIHS : Threshold when input voltage in hysteresis characteristics is set to “H” level

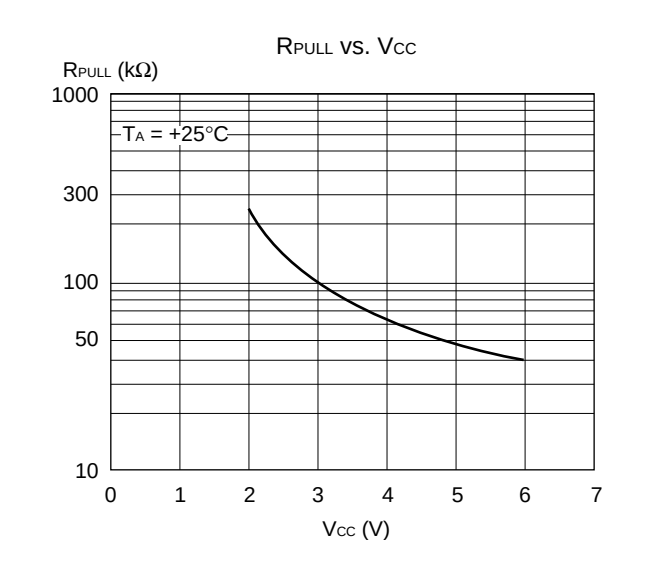
VILS : Threshold when input voltage in hysteresis characteristics is set to “L” level

MB89170/170A Series

(5) Power Supply Current



(6) Pull-up Resistance



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic:	Assembler notation of an instruction
~:	The number of instructions
#:	The number of bytes
Operation:	Operation of an instruction
TL, TH, AH:	A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following: • “–” indicates no change. • dH is the 8 upper bits of operation description data. • AL and AH must become the contents of AL and AH prior to the instruction executed. • 00 becomes 00.
N, Z, V, C:	An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.
OP code:	Code of an instruction. If an instruction is more than one code, it is written according to the following rule: Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A →	–	–	–	+ + – +	03
ROLC A	2	1	← C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89173L MB89174L	MB89P173 MB89173 MB89174A	MB89P173-201	MB89P175A	MB89PV170A
	Specifying procedure	Specify when ordering masking	Specify when ordering masking	Standard option product	Set with EPROM programmer	Setting not possible
1	Pull-up resistors • P00 to P07, P10 to P17 • P30 to P37, P40 to P44	Can be selected per pin	Can be selected per pin	All ports Fixed to no pull-up resistor	Can be set per pin (However, P40 to P44 are available only for no pull-up resistor.)	All ports Fixed to no pull-up resistor option
2	Power-on reset • Power-on reset provided • No power-on reset	Selectable	Selectable	Fixed to no power-on reset option	Setting possible	Fixed to power-on reset option
3	Selection of oscillation stabilization time initial value (when operating at F_{CH} = 3.58 MHz) 3: $2^{18}/F_{CH}$ (approx. 73.2 ms) 2: $2^{16}/F_{CH}$ (approx. 18.3 ms) 1: $2^{12}/F_{CH}$ (approx. 1.1 ms) 0: $2^{3}/F_{CH}$ (approx. 0 ms)	Selectable	Selectable	Fixed to $2^{16}/F_{CH}$	Setting possible	Fixed to $2^{18}/F_{CH}$
4	Reset pin output • Reset output enabled • Reset output disabled	Selectable	Selectable	Fixed to reset output option	Setting possible	Fixed to reset output option
5	Clock mode selection • Dual-clock mode • Single-clock mode	Fixed to single-clock mode	Selectable	Fixed to dual-clock mode	Setting possible	Fixed to dual-clock mode

Note: Reset is input asynchronized with the internal clock whether power-on reset is provided or not.

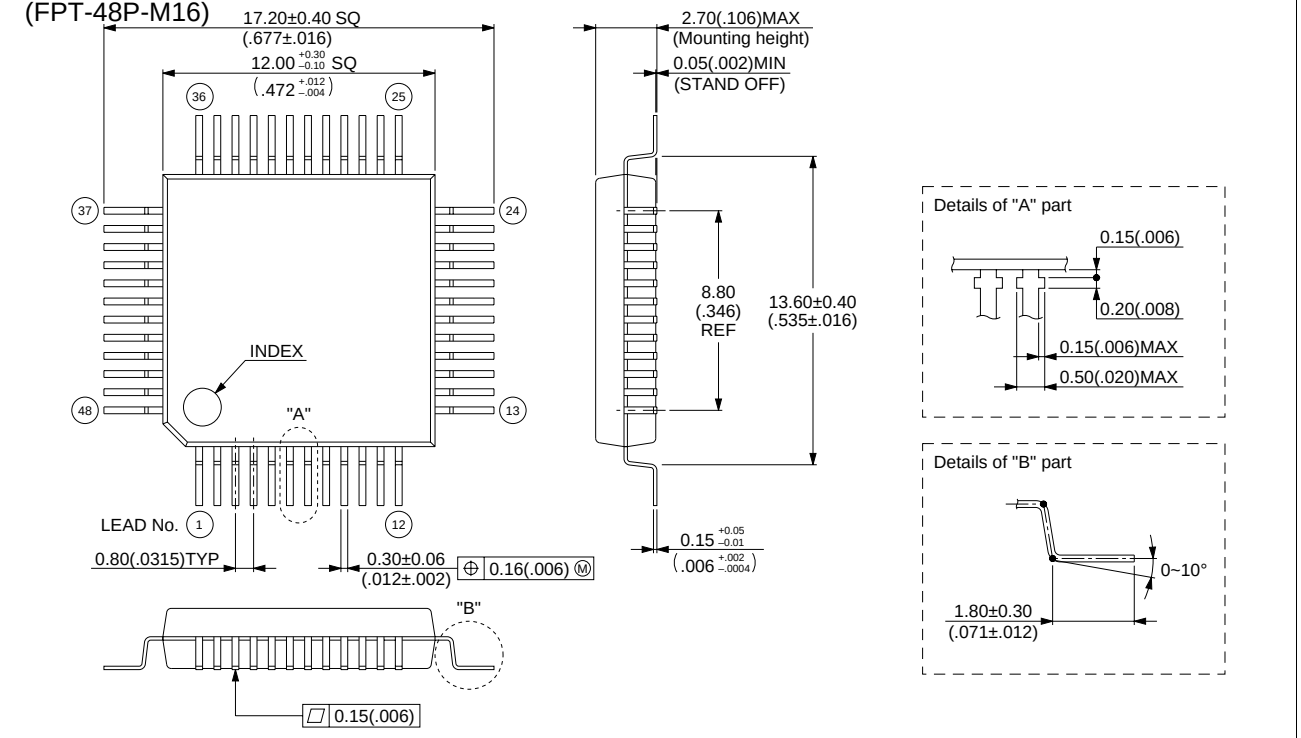
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89173PF MB89174APF MB89P173PF MB89P175APF MB89173LPF MB89174LPF	48-pin Plastic QFP (FPT-48P-M16)	
MB89PV170ACF	48-pin Ceramic MQFP (MQP-48C-P01)	

MB89170/170A Series

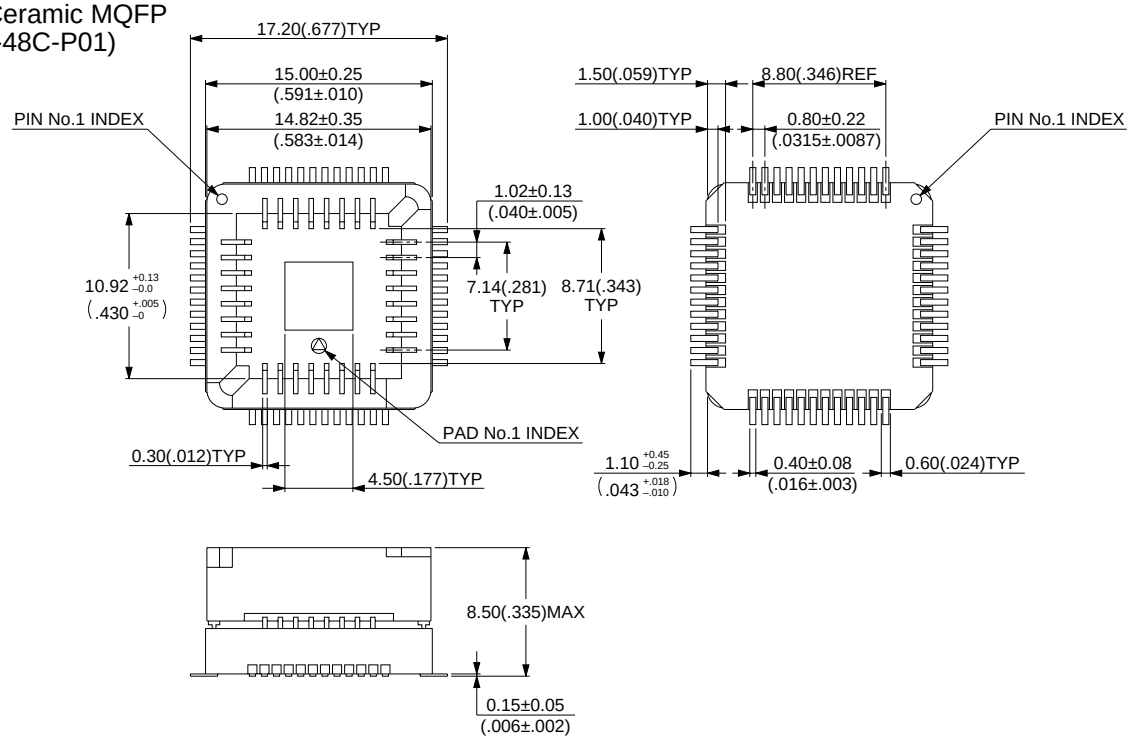
■ PACKAGE DIMENSION

48-pin Plastic QFP
(FPT-48P-M16)



Dimensions in mm (inches)

48-pin Ceramic MQFP
(MQP-48C-P01)



Dimensions in mm (inches)

MB89170/170A Series

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