

# 8-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-8L MB89190/190A Series

**MB89191/193/195/P195/PV190****MB89191A/191AH/193A/193AH/195A/P195A/PV190A**

### ■ OUTLINE

The MB89190/190A series microcontrollers contain various resources such as timers, serial interfaces, A/D converters, external interrupts, and remote-control functions, as well as an F<sup>2</sup>MC\*-8L CPU core for low-voltage and high-speed operations. These single-chip microcontrollers are suitable for small devices such as remote controllers with compact packages.

\*: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

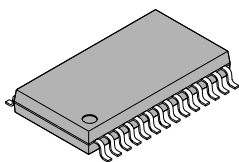
### ■ FEATURES

- Minimum execution time: 0.95  $\mu$ s at 4.2 MHz ( $V_{CC} = 2.7$  V)
- F<sup>2</sup>MC-8L family CPU core
- Two timers
  - 8/16-bit timer/counter
  - 20-bit timebase counter
- Serial interface
  - 8-bit synchronous serial (Selectable transfer direction allows communication with various equipment.)

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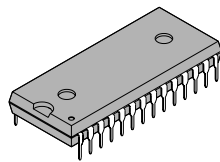
### ■ PACKAGE

28-pin Plastic SOP



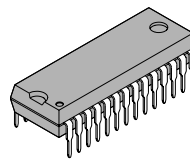
(FPT-28P-M17)

28-pin Plastic DIP



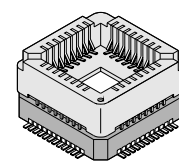
(DIP-28P-M05)

28-pin Plastic SH-DIP



(DIP-28P-M03)

48-pin Ceramic MQFP



(MQP-48C-P01)

# MB89190/190A Series

(Continued)

- External interrupts  
Edge detection (Selectable edge): 3 channels  
Low-level interrupt (Wake-up function): 8 channels
- A/D converter (MB89190A series only)  
8-bit successive approximation type: 8 channels
- Built-in remote-control transmitting frequency generator
- Low-power consumption modes  
Stop mode (Almost no current consumption occurs because oscillation stops.)  
Sleep mode (The current consumption is reduced about 1/3 of that during normal operation because the CPU stops.)
- Packages  
SOP-28, SH-DIP-28, and DIP-28

## ■ PRODUCT LINEUP

Part number Item	MB89191 MB89191A MB89191AH	MB89193 MB89193A MB89193AH	MB89195 MB89195A	MB89P195 MB89P195A	MB89PV190 MB89PV190A
Classification	Mask ROM products			One-time product	For development and evaluation
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits			
CPU functions	The number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, and 16 bits Minimum execution time: 0.95 μs at 4.2 MHz Interrupt processing time: 8.57 μs at 4.2 MHz				
Ports	Output port (N channel open drain): 4 (also serves as peripherals for MB89190A series) or 6 (for MB89190 series) I/O port (CMOS): 16 (also serves as peripherals) Total: 20 or 22				
Timer counter	2 channels of 8-bit timer counter or one 16-bit event counter (operation clock: 1.9 μs, 30.4 μs, and 487.6 μs at 4.2 MHz, and external clock)				
Serial I/O	8 bits LSB/MSB first selectable Transfer clock (external, 1.9 μs, 7.6 μs, 30.4 μs at 4.2 MHz)				
A/D converter (MB89190A series only)	8 bits × 8 channels A/D conversion mode (conversion time: 41.9 μs at 4.2 MHz) Sense mode (conversion time: 11.9 μs at 4.2 MHz) Capable of continuous activation by an internal timer. Reference voltage input				

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# MB89190/190A Series

(Continued)

Part number Item	MB89191 MB89191A MB89191AH	MB89193 MB89193A MB89193AH	MB89195 MB89195A	MB89P195 MB89P195A	MB89PV190 MB89PV190A
External interrupt 1	3 independent channels (selectable edge, interrupt vector, and interrupt source flag) Rising/falling/both edge selectable Used for wake-up from stop/sleep mode. (Edge detection is also permitted in the stop mode.)				
External interrupt 2 (Wake-up function)	8 channels (low-level interrupt only)				
Remote-control transmitting frequency generator	The pulse width and cycle are software-programmable.				
Standby mode	Sleep mode and stop mode				
Process	CMOS				
Operating voltage*	2.2 V to 6.0 V			2.7 V to 6.0 V	
EPROM for use					MBM27C256A- 20TVM

\* : Varies with conditions such as operating frequencies (see "■ Electrical Characteristics.") It differs from the operating voltage of an A/D converter.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89191 MB89191A MB89191AH MB89193 MB89193A MB89193AH MB89195 MB89195A	MB89P195 MB89P195A	MB89PV190 MB89PV190A
DIP-28P-M05	○	○	×
DIP-28P-M03	○	×	×
FPT-28P-M17	○	○	×
MQP-48C-P01	×	×	○*

○ : Available    × : Not available

\* : A socket (manufacturer: Sun Hayato Co., Ltd.) for pin pitch conversion is available.

48QF-28SOP-8L: (MQP-48C-P01) → for conversion to FPT-28P-M17

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403

FAX (81)-3-5396-9106

Note: For more information on each package, see "■ Package Dimensions."

# MB89190/190A Series

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback model, verify its difference from the model that will actually be used. Take particular care on the following points:

- On the MB89191/191A, addresses 0140<sub>H</sub> to 0180<sub>H</sub> cannot be used for register banks.
- The stack area, etc., is set in the upper limit of the RAM.

### 2. Current Consumption

- In the case of MB89PV190/PV190A, added is the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the products with an OTPROM (EPROM) will consume more current than the products with a mask ROM.  
However, the same is current consumption in the sleep/stop mode. (For more information, see “■ Electrical Characteristics.”)

### 3. Mask Options

Functions that can be selected as options and how to designate these options vary with product.

Before using options, check “■ Mask Options.”

Take particular care on the following points:

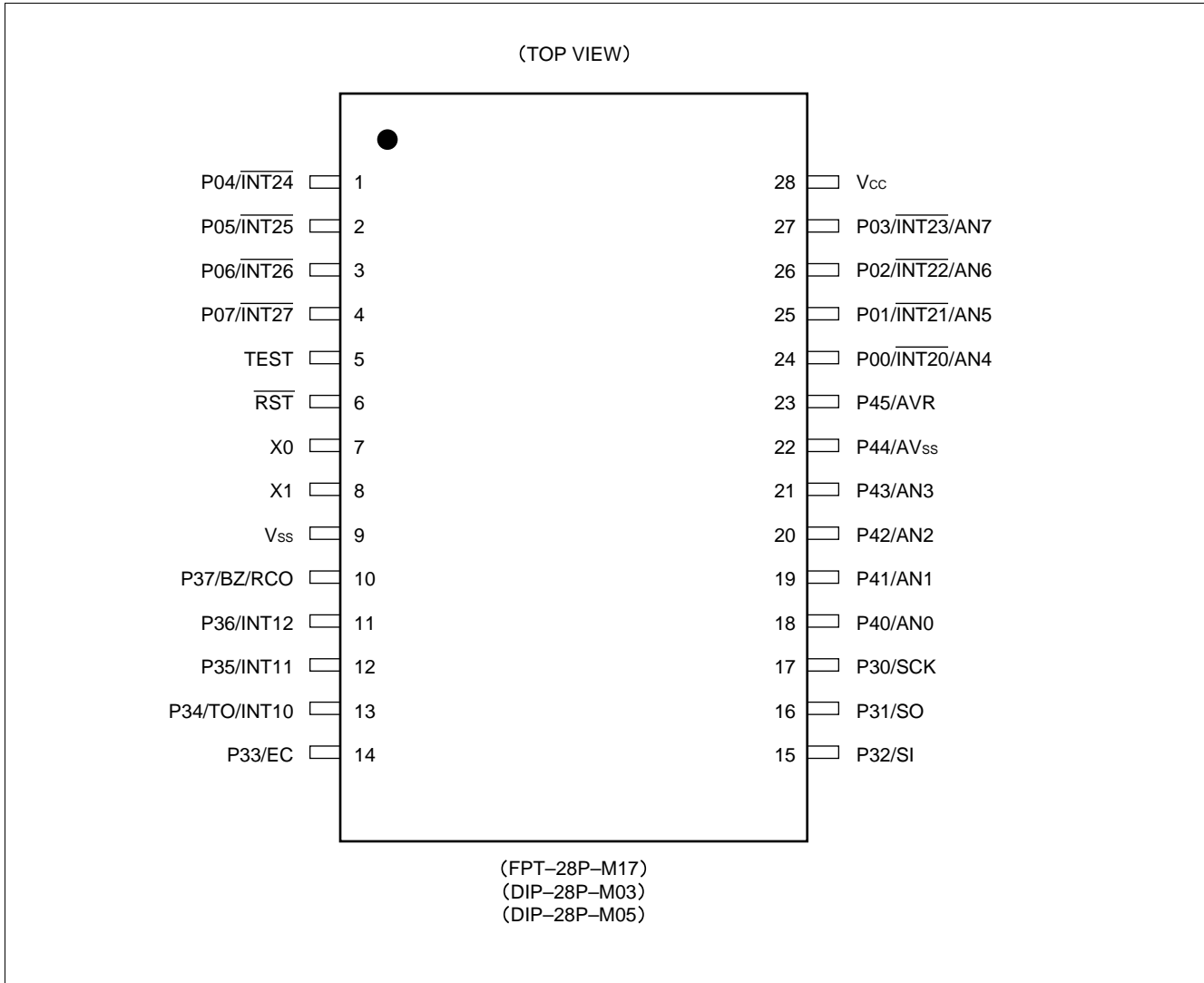
- Pull-up resistor optional cannot be set for P00 to P03, and P40 to P45 on the MB89191A/193A/195A/P195A.
- The power-on reset option is fixed as “enabled” for MB89P195/P195A.
- Options are fixed on the MB89PV190/PV190A.

### 4. MB89191AH/MB89193AH

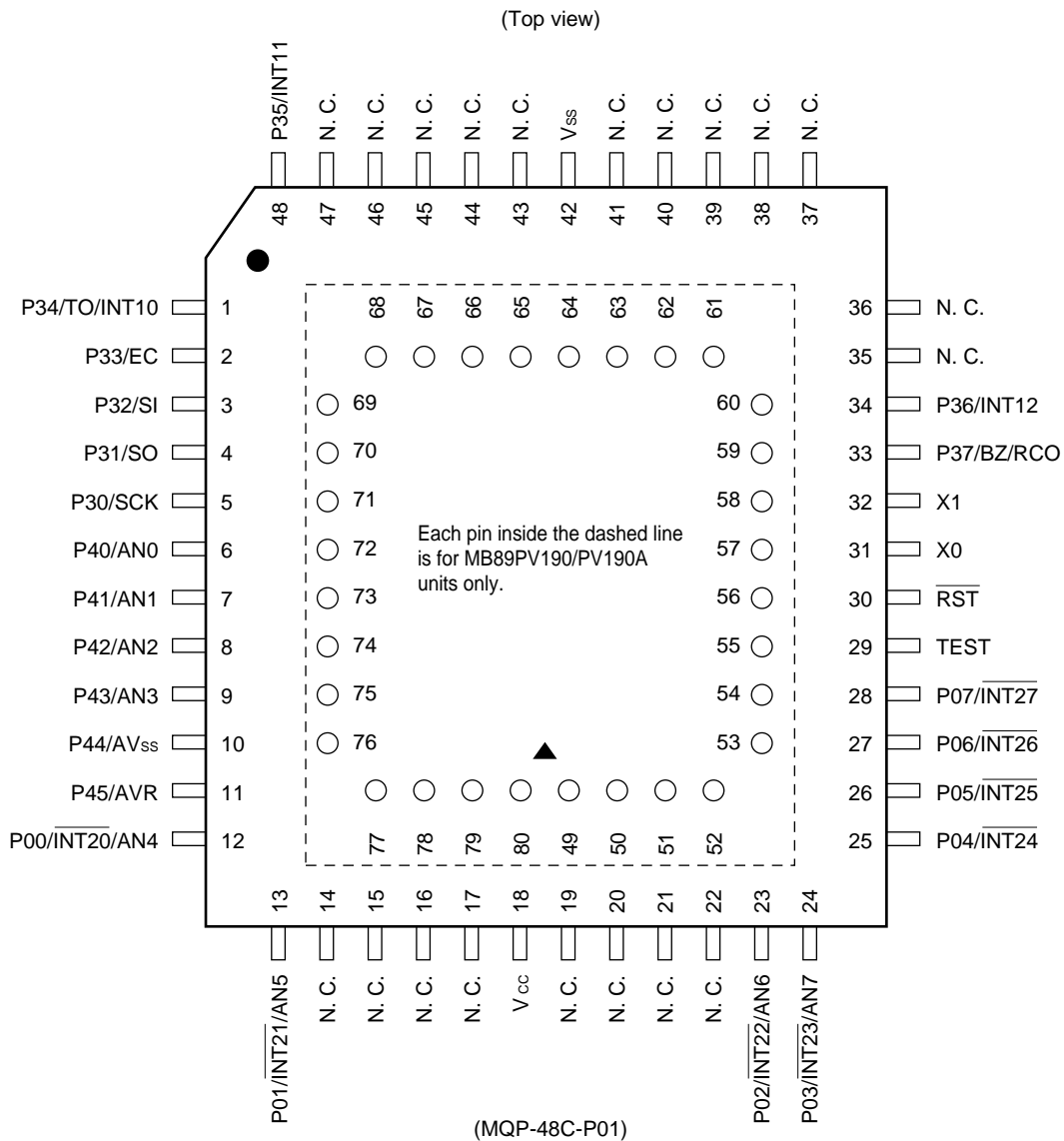
MB89191AH/193AH are “L” level heavy output current drive type of P30 to P32 and P40 to P43 of MB89191A/193A. Characteristics other than “L” level output of P30 to P32 and P40 to P43 are the same as MB89191A/193A.

# MB89190/190A Series

## ■ PIN ASSIGNMENT



# MB89190/190A Series



• Pin assignment on the package top (MB89PV190/PV190A only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V <sub>PP</sub>	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V <sub>SS</sub>	72	N.C.	80	V <sub>CC</sub>

N.C.: Internally connected. Do not use.

# MB89190/190A Series

## ■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SOP <sup>*1</sup> , DIP <sup>*2</sup> SH-DIP <sup>*3</sup>	MQFP <sup>*4</sup>			
7	31	X0	A	Clock oscillation pins
8	32	X1		
5	29	TEST	B	Test input pin Connect directly to V <sub>ss</sub> .
6	30	$\overline{\text{RST}}$	C	Reset I/O pin This pin consists of an N-ch open-drain output with a pull-up resistor and of hysteresis input. A low level is output from this pin by internal source. The internal circuit is initialized by the input of a low level.
24 to 27	12, 13, 23, 24	P00/ $\overline{\text{INT20}}$ / AN4 to P03/ $\overline{\text{INT23}}$ /AN7	G	General-purpose I/O ports Also serve as external interrupt input pins. In the MB89190A series, also serve as analog input pins. External interrupt input is of hysteresis input type.
1 to 4	25 to 28	P04/ $\overline{\text{INT24}}$ to P07/ $\overline{\text{INT27}}$	D	General-purpose I/O ports Also serve as external interrupt input. External interrupt input is of hysteresis input type.
17	5	P30/SCK	D	General-purpose I/O port Also serves as clock I/O for the 8-bit serial I/O interface. The serial I/O clock input is of hysteresis input type with a built-in noise filter.
16	4	P31/SO	E	General-purpose I/O port Also serves as a serial I/O data output pin.
15	3	P32/SI	D	General-purpose I/O port Also serves as a serial I/O data input pin. The serial I/O data input is of hysteresis input type with a built-in noise filter.
14	2	P33/EC	D	General-purpose I/O port Also serves as an external clock input pin for the 8-bit timer/counter. External clock input of the 8-bit timer/counter is hysteresis input type with a built-in noise filter.
13	1	P34/TO/ INT10	D	General-purpose I/O port Also serves as the overflow output and external interrupt input for the 8-bit timer/counter. External interrupt input is of hysteresis input type with a built-in noise filter.

\*1: FPT-28P-M17

\*2: DIP-28C-M05

\*3: DIP-28P-M03

\*4: MQP-48C-P01

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# MB89190/190A Series

(Continued)

Pin no.		Pin name	Circuit type	Function
SOP* <sup>1</sup> , DIP* <sup>2</sup> SH-DIP* <sup>3</sup>	MQFP* <sup>4</sup>			
12	48	P35/INT11	D	General-purpose I/O port Also serve as external interrupt input pins. External interrupt input is of hysteresis input type with a built-in noise filter.
11	34	P35/INT12		
10	33	P37/BZ/RCO	E	General-purpose I/O port Also serves as a buzzer output pin and remote-control output pin.
18 to 21	6 to 9	P40/AN0 to P43/AN3	F	N-ch open-drain output ports Also serve as analog input pins for the A/D converter.
23	11	P45/AVR	F	In the MB89190A series, also serves as a reference voltage input pin for the A/D converter. In the MB89190 series, serves as an N-ch open-drain output port.
22	10	P44/AV <sub>ss</sub>	F	In the MB89190A series, also serves as a power pin for the A/D converter, and should be applied the same voltage as V <sub>ss</sub> to. In the MB89190 series, also serves as an N-ch open-drain output port.
28	18	V <sub>cc</sub>	—	Power supply pin
9	42	V <sub>ss</sub>	—	Power supply (GND) pin

\*1: FPT-28P-M17

\*2: DIP-28P-M05

\*3: DIP-28P-M03

\*4: MQP-48C-P01



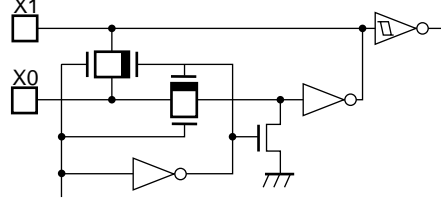
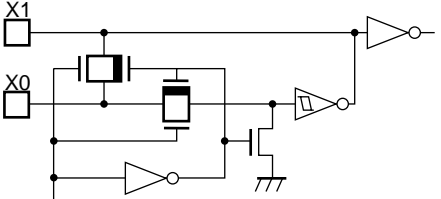
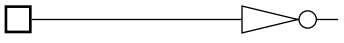
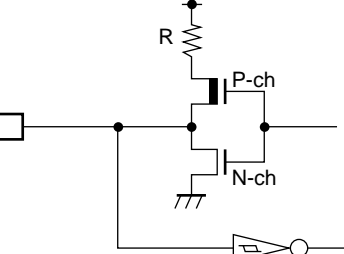
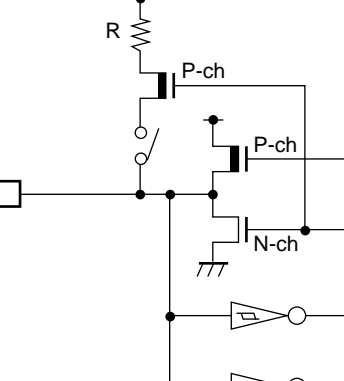
# MB89190/190A Series

- External EPROM pins (MB89PV190/PV190A)

Pin no.	Pin name	I/O	Function
49	V <sub>PP</sub>	O	"H" level output pin
79	A14	O	Address output pins
78	A13		
50	A12		
75	A11		
71	A10		
76	A9		
77	A8		
51	A7		
52	A6		
53	A5		
54	A4		
55	A3		
58	A2		
59	A1		
60	A0		
61	O1	I	Data input pins
62	O2		
63	O3		
65	O4		
66	O5		
67	O6		
68	O7		
69	O8		
70	$\overline{CE}$	O	ROM chip enable pin Outputs "H" during standby.
73	$\overline{OE}$	O	ROM output enable pin Outputs "L" at all times.
80	V <sub>CC</sub>	O	EPROM power pin
64	V <sub>SS</sub>	O	Power supply (GND) pin

# MB89190/190A Series

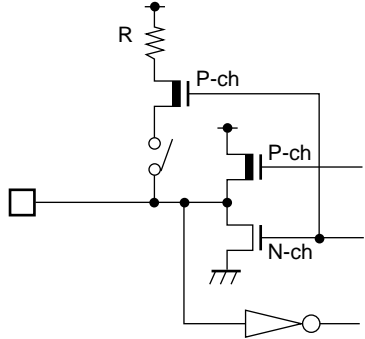
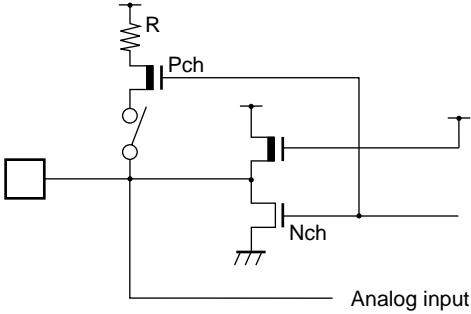
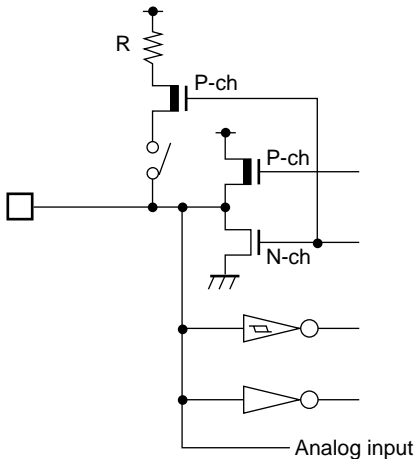
## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>• Oscillation feedback resistor of approximately 1 MΩ at 5 V</li> <li>• When crystal and ceramic oscillators are selected optionally</li> </ul>
	 <p>Standby control signal</p>	<ul style="list-style-type: none"> <li>• When CR oscillation is selected optionally</li> </ul>
B		
C	 <p>R P-ch N-ch</p>	<ul style="list-style-type: none"> <li>• Output pull-up resistor (P-ch): Approx. 50 kΩ at 5 V</li> <li>• Hysteresis input</li> </ul>
D	 <p>R P-ch P-ch N-ch</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input (resource input)</li> <li>• Pull-up resistor optional</li> </ul>

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# MB89190/190A Series

(Continued)

Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Pull-up resistor optional</li> </ul>
F	 <p style="text-align: right;">Analog input</p>	<ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• Analog input</li> <li>• Pull-up resistor optional (MB89190 series only)</li> </ul>
G	 <p style="text-align: right;">Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input (resource input)</li> <li>• Analog input</li> <li>• Pull-up resistor optional (MB89190 series only)</li> </ul>

# MB89190/190A Series

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input or output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ Electrical Characteristics” is applied between  $V_{CC}$  to  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply ( $AV_{CC}$  and  $AVR$ ) and analog input from exceeding the digital power supply ( $V_{CC}$ ) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be  $AV_{CC}=DAVC=V_{CC}$  and  $AV_{SS}=AVR=V_{SS}$  even if the A/D and D/A converters are not in use.

### 4. Treatment of N.C. Pin

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Fluctuations

Although operation is assured within the rated range of  $V_{CC}$  power supply voltage, a rapid fluctuation of the voltage could cause malfunctions within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

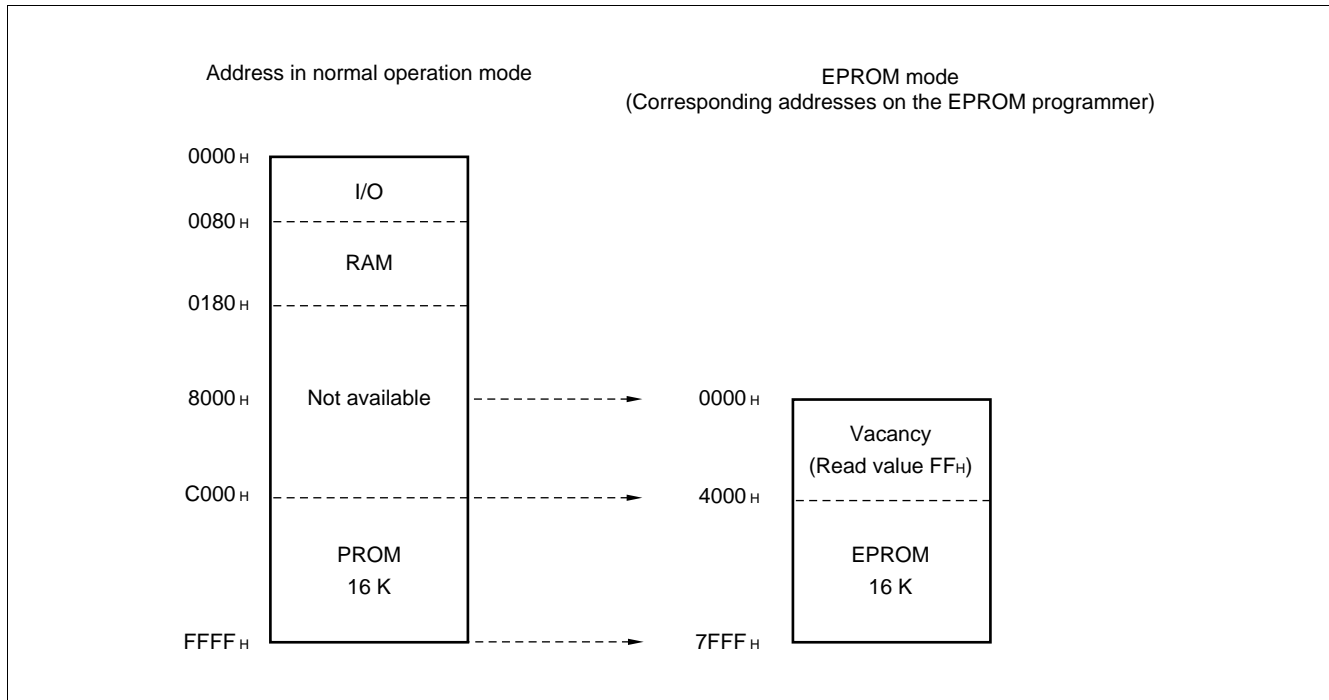
Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and release from stop mode.

# MB89190/190A Series

## ■ PROGRAMMING TO PROM ON THE MB89P195/P195A

The MB89P195/P195A can program data in the internal PROM using a dedicated conversion adaptor and specified general-purpose EPROM programmer.

### 1. Memory Space



#### • Programming procedure

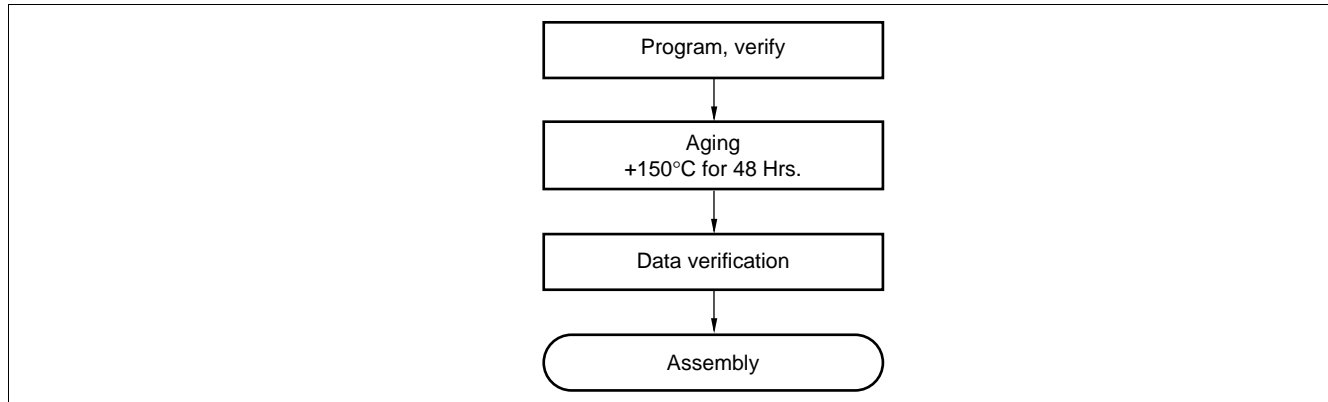
- (1) Load program data into the ROM programmer at addresses 4000<sub>H</sub> to 7FFF<sub>H</sub>. (Addresses 0C000<sub>H</sub> to 0FFFF<sub>H</sub> in the operation mode correspond to 4000<sub>H</sub> to 7FFF<sub>H</sub> in ROM programmer. See the illustration above.)
- (2) Set the data at addresses 0000<sub>H</sub> to 3FFF<sub>H</sub> of the programmer ROM in the ROM programmer, to FF<sub>H</sub>.
- (3) Program in the successive-address write mode of the ROM programmer.

Note: Program must be started at the address 00000<sub>H</sub>.  
For details, contact our Sales Division.

# MB89190/190A Series

## 2. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcontroller program.



## 3. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test. For this reason, a programming yield of 100% cannot be assured at all times.

## 4. EPROM Programmer Socket Adapter

Part no.	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Recommended programmer manufacturer and programmer name			
			Minato Electronics Inc.		Data I/O Co., Ltd.	
			MODEL1890A (ver.2.2) + OU-910 (ver.4.1)	UNISITE (ver.5.0 or later)	3900 (ver.2.8 or later)	2900 (ver.3.8 or later)
MB89P195	DIP-28	ROM-28DP-28DP-8L	Recommended	Recommended		
MB89P195A						
MB89P195PF	SOP-28	ROM-28SOP-28DP-8L	Recommended	Recommended		
MB89P195APF						

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403

FAX: (81)-3-5396-9106

Minato Electronics Inc.: TEL: USA (1)-916-348-6066

JAPAN (81)-45-591-5611

Data I/O Co., Ltd.: TEL: USA/ASIA (1)-206-881-6444

EUROPE (49)-8-985-8580

# MB89190/190A Series

## ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20TVM

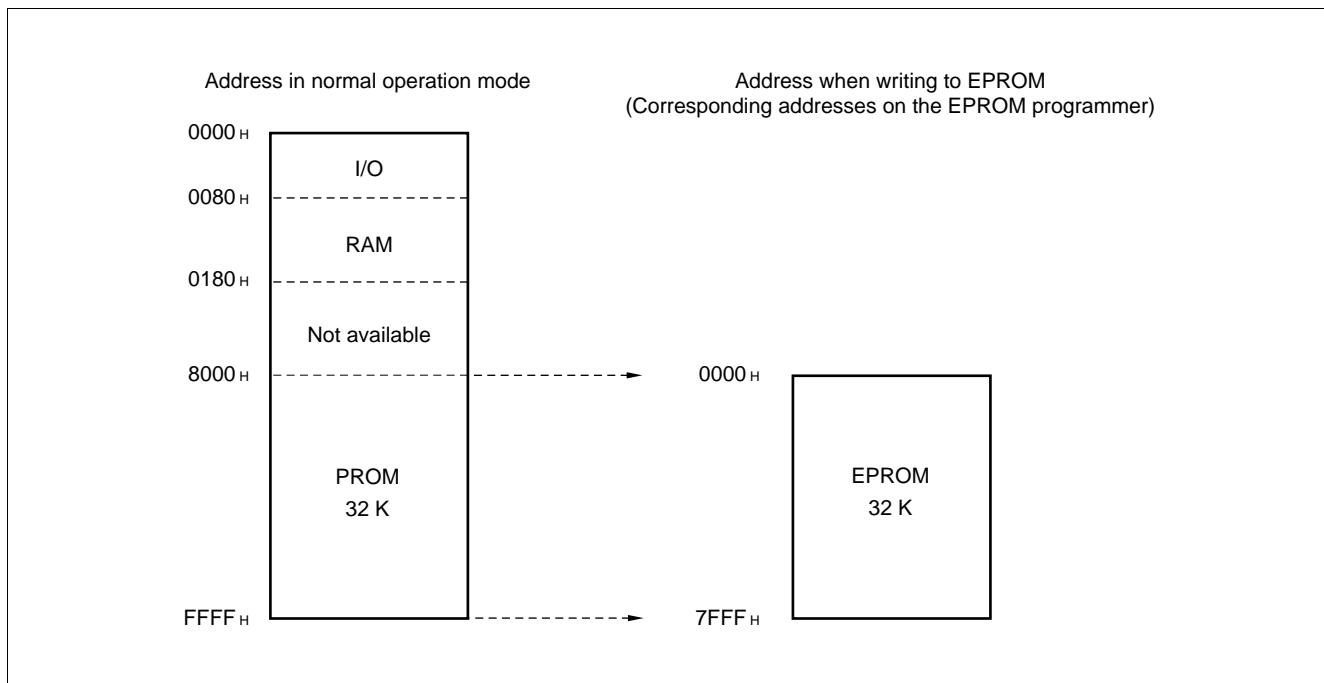
### 2. Programming Socket Adapter

To program to the EPROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) below.

Package	Adapter socket part number
LCC-32	ROM-32LC-28DP-YS

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403  
FAX (81)-3-5396-9106

### 3. Memory Space

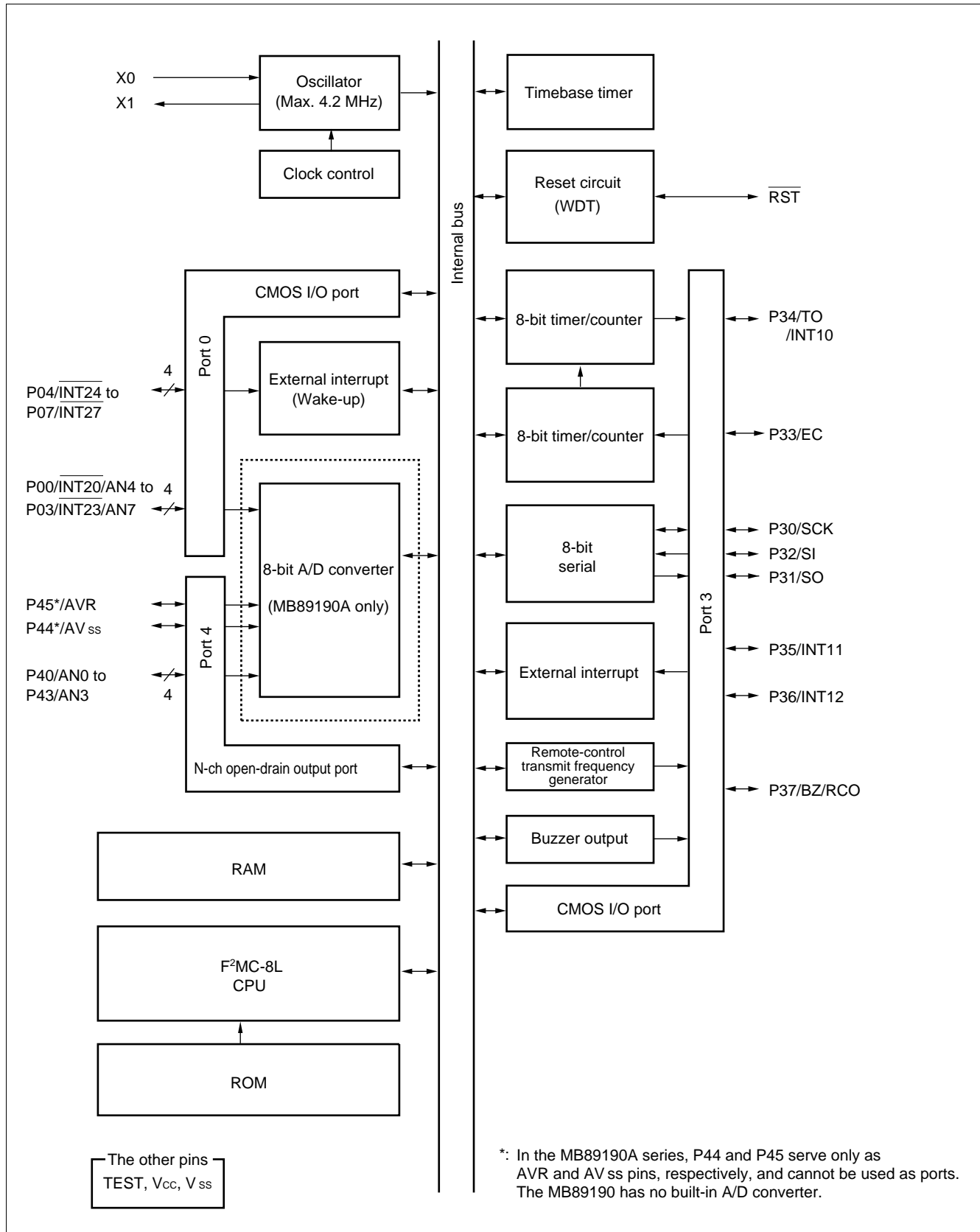


### 4. Programming to the EPROM

- (1) Set the EPROM programmer for MBM27C256A.
- (2) Load program data into the EPROM programmer at 0000<sub>H</sub> to 7FFF<sub>H</sub>.
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

# MB89190/190A Series

## ■ BLOCK DIAGRAM



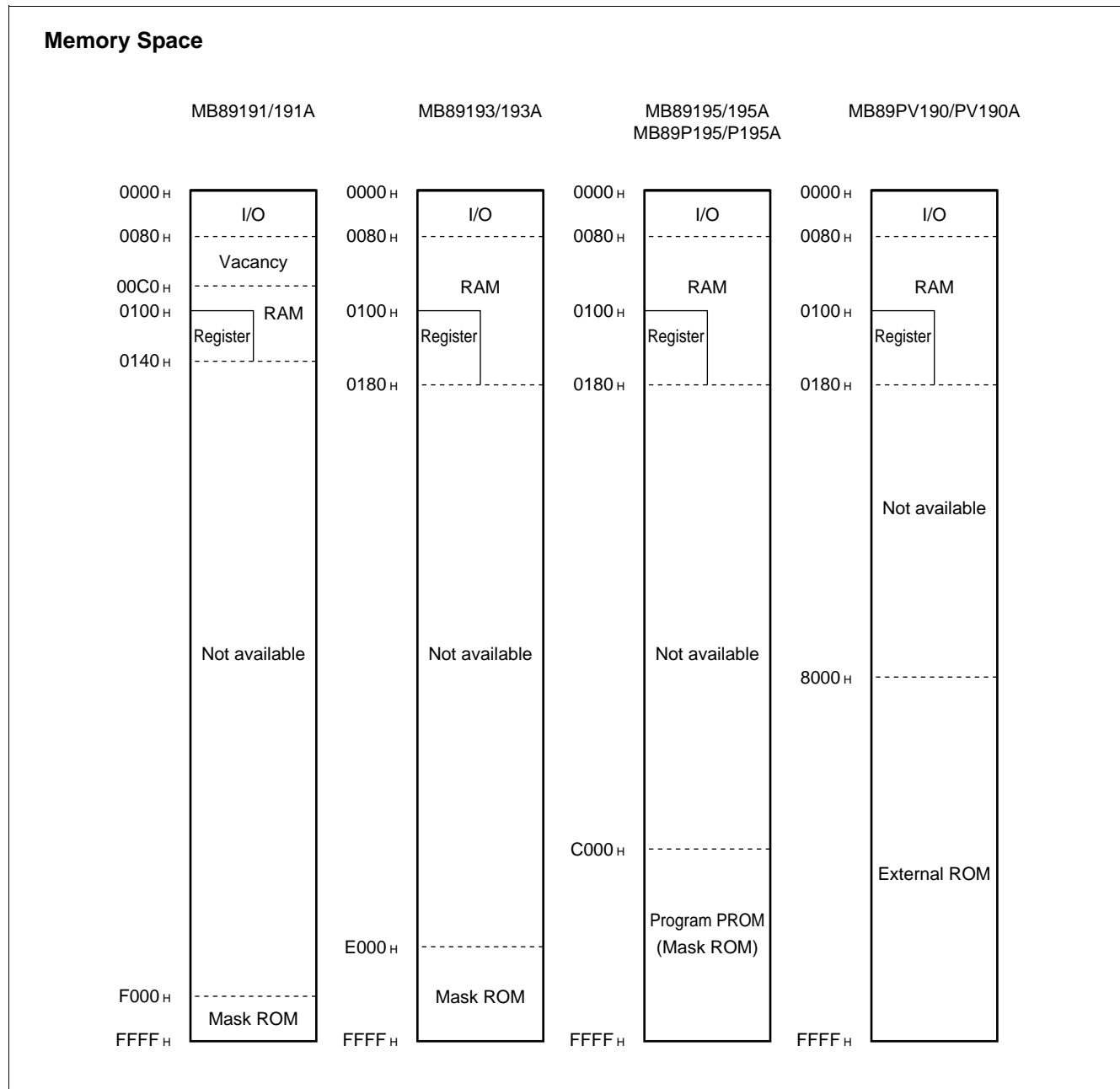


# MB89190/190A Series

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of MB89190/190A series offer a 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end of I/O area, that is, the highest address. The tables of interrupt reset vectors, and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89190/190A series is structured below:

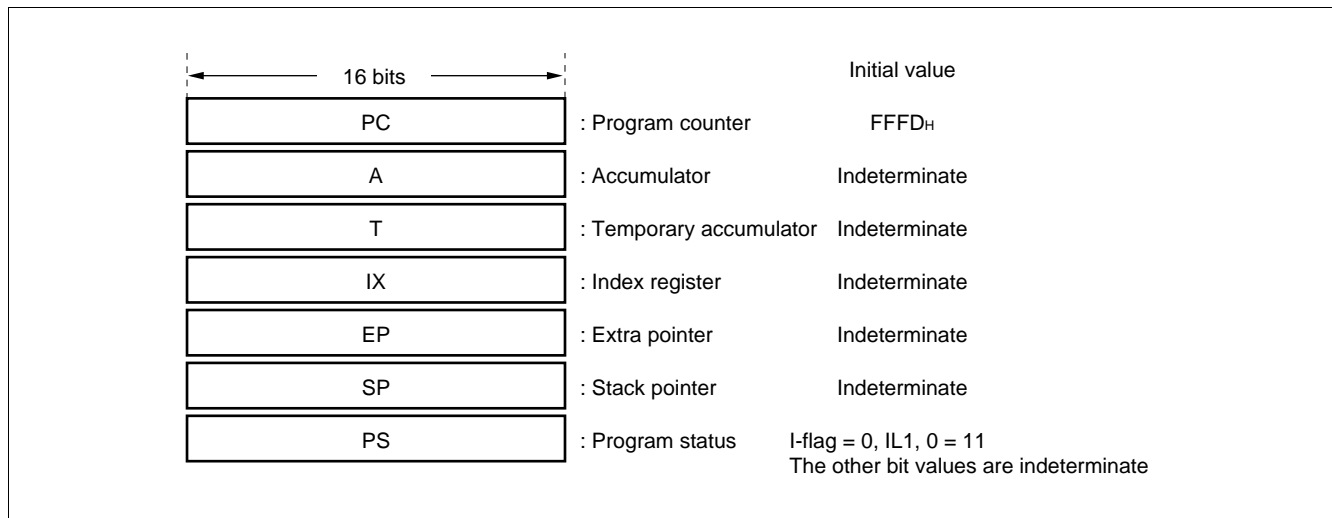


# MB89190/190A Series

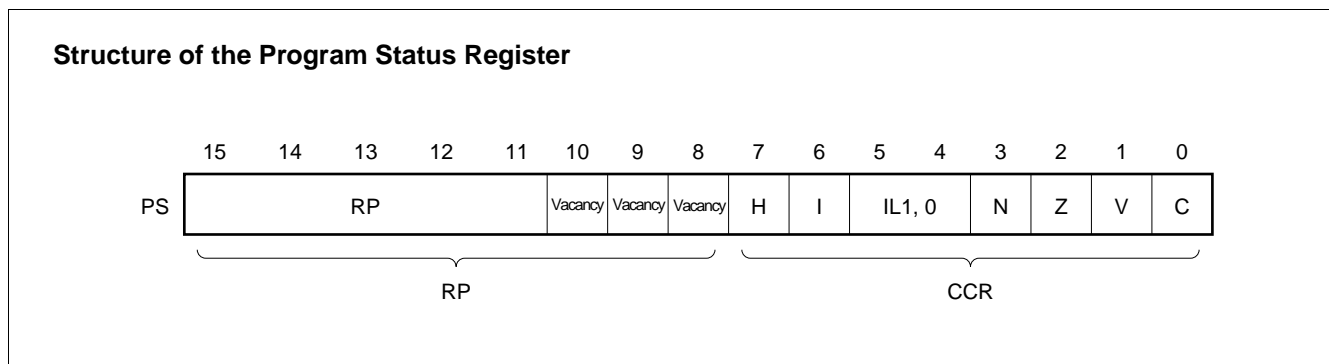
## 2. Registers

The F<sup>2</sup>MC-8L family has two types of registers; dedicated hardware registers and general-purpose memory registers. The following dedicated registers are provided:

Program counter (PC):	A 16-bit-long register for indicating the instruction storage positions
Accumulator (A):	A 16-bit-long temporary register for arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit-long register which is used for arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit-long register for index modification
Extra pointer (EP) :	A 16-bit-long pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit-long pointer for indicating a stack area
Program status (PS) :	A 16-bit-long register for storing a register pointer, a condition code



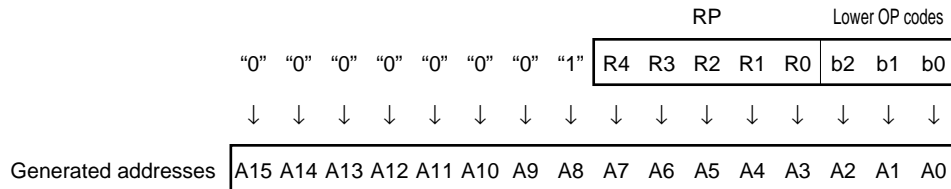
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) (see the diagram below).



# MB89190/190A Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

## Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

**H-flag:** Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

**I-flag:** Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

**IL1, 0:** Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	ILO	Interrupt level	High-low
0	0	1	High
0	1		↑
1	0	2	↓
1	1	3	

**N-flag:** Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

**Z-flag:** Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

**V-flag:** Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

**C-flag:** Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to '1' the shift-out value in the case of a shift instruction.

# MB89190/190A Series

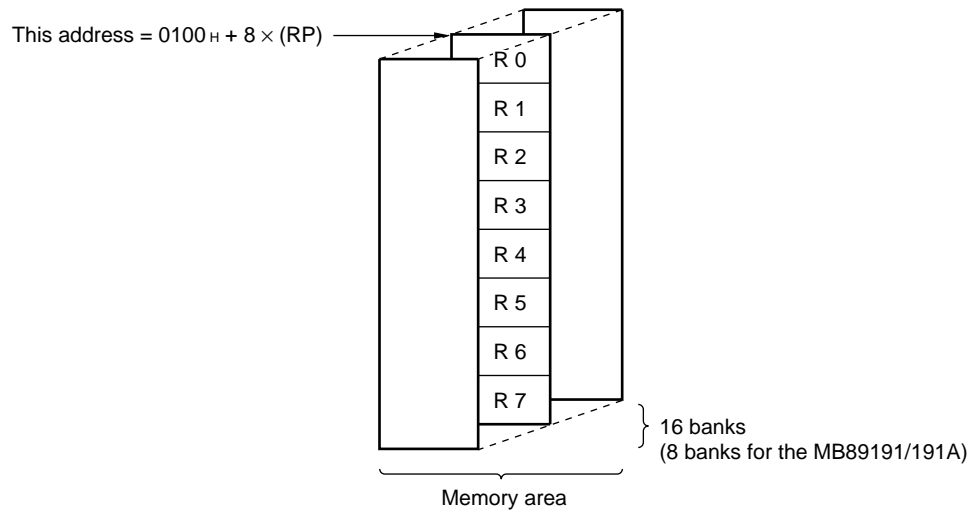
The following general-purpose registers are provided:

General-purpose registers: An 8-bit-long register for storing data

The general-purpose registers are of 8 bits and located in register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89190/190A (8 banks on MB89191/191A). The bank currently in use is indicated by the register bank pointer. (RP)

Note: The number of register banks that can be used varies with the RAM size.

## Register Bank Configuraiton



# MB89190/190A Series

## ■ I/O MAP

Address	Read/write	Register name	Register description
00 <sub>H</sub>	(R/W)	PDR0	Port 0 data register
01 <sub>H</sub>	(W)	DDR0	Port 0 data direction register
02 <sub>H</sub>	(R/W)	ENI0	Port 0 input enable register
03 <sub>H</sub> to 07 <sub>H</sub>			Vacancy
08 <sub>H</sub>	(R/W)	STBC	Standby control register
09 <sub>H</sub>	(R/W)	WDTC	Watchdog control register
0A <sub>H</sub>	(R/W)	TBTC	Time-base timer control register
0B <sub>H</sub>			Vacancy
0C <sub>H</sub>	(R/W)	PDR3	Port 3 data register
0D <sub>H</sub>	(W)	DDR3	Port 3 data direction register
0E <sub>H</sub>	(R/W)	PDR4	Port 4 data register
0F <sub>H</sub>	(R/W)	BUZR	Buzzer register
10 <sub>H</sub> to 13 <sub>H</sub>			Vacancy
14 <sub>H</sub>	(R/W)	RCR1	Remote-control transmit control register 1
15 <sub>H</sub>	(R/W)	RCR2	Remote-control transmit control register 2
16 <sub>H</sub>			Vacancy
17 <sub>H</sub>			Vacancy
18 <sub>H</sub>	(R/W)	T2CR	Timer 2 control register
19 <sub>H</sub>	(R/W)	T1CR	Timer 1 control register
1A <sub>H</sub>	(R/W)	T2DR	Timer 2 data register
1B <sub>H</sub>	(R/W)	T1DR	Timer 1 data register
1C <sub>H</sub>	(R/W)	SMR	Serial mode register
1D <sub>H</sub>	(R/W)	SDR	Serial data register
1E <sub>H</sub>			Vacancy
1F <sub>H</sub>			Vacancy
20 <sub>H</sub>	(R/W)	ADC1	A/D converter control register 1
21 <sub>H</sub>	(R/W)	ADC2	A/D converter control register 2
22 <sub>H</sub>	(R/W)	ADCD	A/D converter data register
23 <sub>H</sub>	(R/W)	EIC1	External interrupt control register 1
24 <sub>H</sub>	(R/W)	EIC2	External interrupt control register 2
25 <sub>H</sub> to 31 <sub>H</sub>			Vacancy
32 <sub>H</sub>	(R/W)	EIE2	External interrupt 2 enable register
33 <sub>H</sub>	(R/W)	EIF2	External interrupt 2 flag register
34 <sub>H</sub> to 7B <sub>H</sub>			Vacancy
7C <sub>H</sub>	(W)	ILR1	Interrupt level register 1
7D <sub>H</sub>	(W)	ILR2	Interrupt level register 2
7E <sub>H</sub>	(W)	ILR3	Interrupt level register 3
7F <sub>H</sub>			Vacancy

Note: Do not use vacancies.

# MB89190/190A Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Rating

( $V_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	Must not exceed $V_{CC} + 0.3\text{ V}$ . MB89190A series only
EPROM program voltage	$V_{PP}$	$V_{SS} - 0.3$	$V_{SS} + 13.0$	V	MB89P195/P195A only
Input voltage	$V_I$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Output voltage	$V_O$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
“L” level maximum output current	$I_{OL1}$	—	10	mA	Except P33 and P34 (Except P30 to P34 and P40 to P43 for MB89191AH/193AH)
	$I_{OL2}$	—	20	mA	P33, P34 (P30 to P34 and P40 to P43 for MB89191AH/193AH)
“L” level average output current	$I_{OLAV1}$	—	4	mA	Except P33 and P34 (Except P30 to P34 and P40 to P43 for MB89191AH/193AH) Average value (operating current × operation rate)
	$I_{OLAV2}$	—	8	mA	P33 and P34 (P30 to P34 and P40 to P43 for MB89191AH/193AH) Average value (operating current × operation rate)
“L” level total average output current	$\Sigma I_{OLAV}$	—	20	mA	Average value (operating current × operation rate)
“L” level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
“H” level maximum output current	$I_{OH1}$	—	-10	mA	Except P33, P34, and P37
	$I_{OH2}$	—	-20	mA	P33, P34, P37
“H” level average output current	$I_{OHAV1}$	—	-2	mA	Except P33, P34, and P37 Average value (operating current × operation rate)
	$I_{OHAV2}$	—	-4	mA	Except P33, P34, and P37 Average value (operating current × operation rate)
“H” level total average output current	$\Sigma I_{OHAV}$	—	-10	mA	Average value (operating current × operation rate)
“H” level total maximum output current	$\Sigma I_{OH}$	—	-30	mA	
Power consumption	$P_D$	—	200	mW	
Operating temperature	$T_a$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

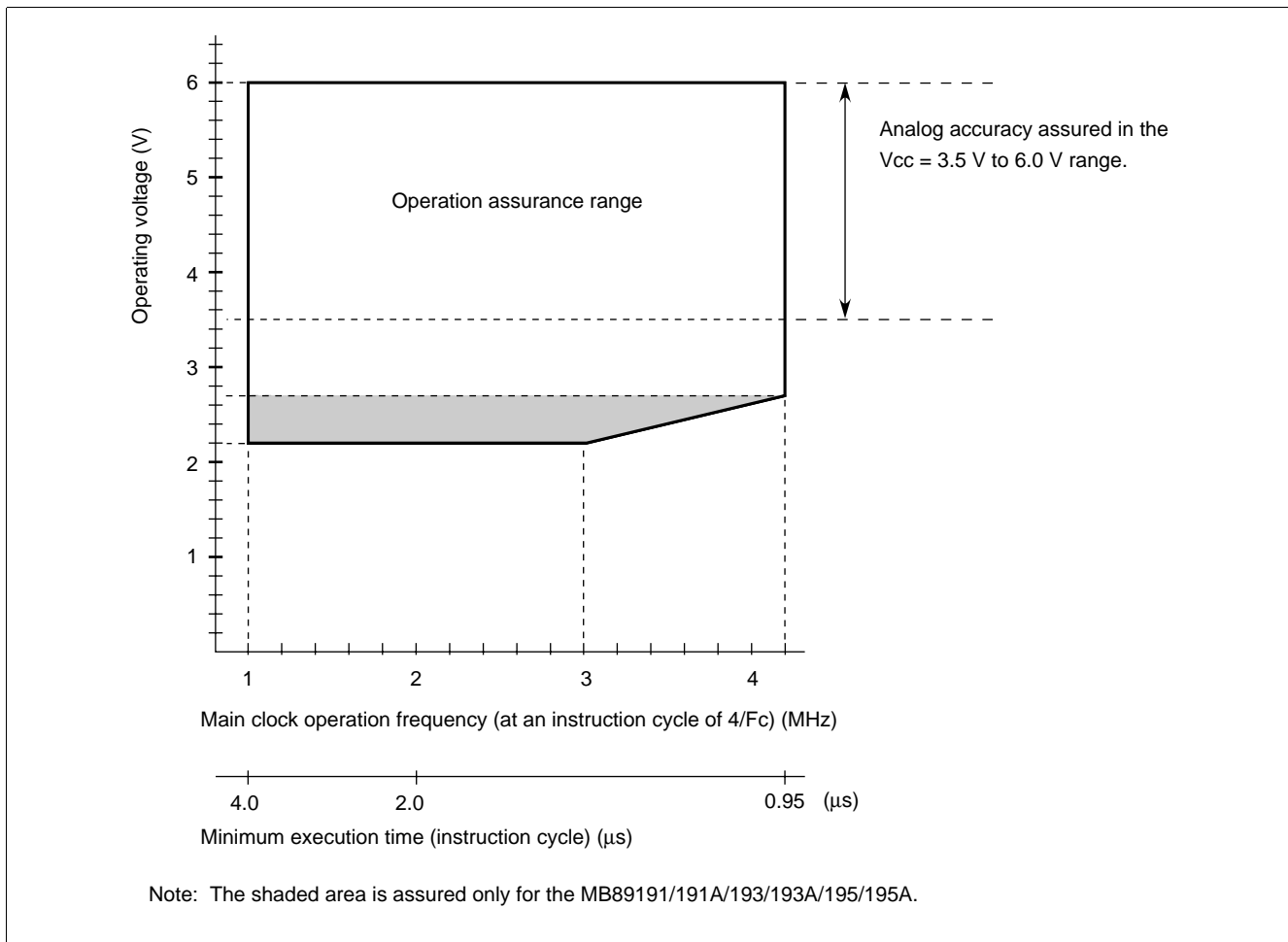
# MB89190/190A Series

## 2. Recommended Operating Conditions

(V<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V <sub>CC</sub>	2.2*	6.0*	V	Normal operation assurance range* MB89191/191A/193/193A/195/195A
		2.7*	6.0*	V	Normal operation assurance range* MB89P195/P195A/PV190/PV190A
		1.5	6.0	V	Retains the RAM state in the stop mode
A/D converter reference input voltage	AVR	0.0	V <sub>CC</sub>	V	
Operating temperature	T <sub>A</sub>	-40	+85	°C	

\* : These values vary with the operation frequency and the assured analog operation range. See Figure 1 and “ 5. A/D Converter Electrical Characteristics.”



**Figure 1 Operating Voltage vs. Main Clock Operating Frequency**

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F<sub>C</sub>.

# MB89190/190A Series

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## 3. DC Characteristics

( $V_{CC} = +5.0\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
“H” level input voltage	$V_{IH}$	P00 to P07, P30 to P37, TEST	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	$V_{IHS}$	$\overline{RST}$ , INT10 to INT12, EC, SCK, SI, INT20 to INT27	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	$V_{IL}$	P00 to P03, P33 to P36, TEST	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	$V_{ILS}$	$\overline{RST}$ , INT10 to INT12, EC, SCK, SI, INT 20 to INT27	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
Open-drain output pin applied voltage	$V_D$	P40 to P44	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	
“H” level output voltage	$V_{OH1}$	P00 to P07, P30 to P32, P35, P36	$I_{OH} = -2.0\text{ mA}$	2.4	—	—	V	
	$V_{OH2}$	P33, P34	$I_{OH} = -15\text{ mA}$	2.4	—	—	V	
	$V_{OH3}$	P37	$I_{OH} = -7.0\text{ mA}$	2.4	—	—	V	
“L” level output voltage	$V_{OL1}$	P00 to P07, P40 to P45, P30 to P32, P35 to P37	$I_{OL} = 1.8\text{ mA}$	—	—	0.4	V	Except MB89191AH/193AH
		P00 to P07, P35 to P37						MB89191AH/193AH
	$V_{OL2}$	$\overline{RST}$	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	$V_{OL3}$	P33, P34	$I_{OL} = 12\text{ mA}$	—	—	0.4	V	Except MB89191AH/193AH
P30 to P34, P40 to P43		MB89191AH/193AH						
Input leakage current (Hi-z output leakage current)	$I_{LI1}$	P00 to P07, P30 to P37, TEST	$0.0\text{ V} < V_I < V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$	Without pull-up resistor
Open-drain output leakage current (Off state)	$I_{LD1}$	P40 to P45	$0.0\text{ V} < V_I < V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$	Without pull-up resistor

(Continued)



# MB89190/190A Series

(Continued)

(V<sub>CC</sub> = 5.0 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Pull-up resistance	R <sub>PULL</sub>	P00 to P07, P30 to P37, P40 to P45, RST	V <sub>I</sub> = 0.0 V	25	50	100	kΩ	
Power supply voltage*	I <sub>CC</sub>	V <sub>CC</sub>	F <sub>C</sub> = 4.2 MHz	—	5	10	mA	MB89191/ 191A/193/ 193A/195/ 195A/PV190/ PV190A
				—	7	12	mA	MB89P195/ P195A
	I <sub>CCS</sub>		F <sub>C</sub> = 4.2 MHz	—	3	7	mA	Sleep mode
	I <sub>CCH</sub>		T <sub>A</sub> = +25 °C	—	—	1	μA	Stop mode
	I <sub>CCA</sub>		F <sub>C</sub> = 4.2 MHz During A/D converter operation	—	6	13	mA	MB89191A/ 193A/195A/ PV190A
—		8		15	mA	MB89P195A		
Input capacitance	C <sub>IN</sub>	Except AVR, AV <sub>SS</sub> , V <sub>CC</sub> , and V <sub>SS</sub>	f = 1 MHz	—	10	—	pF	

\* : For the MB89PV190/PV190A, the current consumption of a connected EPROM and ICE is not included.  
The measurement condition of the power supply current are set as V<sub>CC</sub> = 5.0 V with an external clock.

# MB89190/190A Series

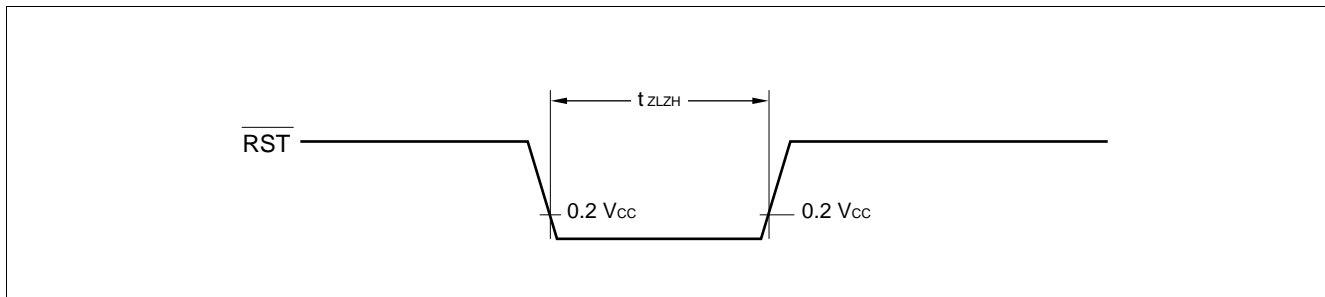
## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{\text{RST}}$ "L" pulse width	$t_{\text{ZLZH}}$	—	$16 t_{\text{CYL}}$	—	ns	

Note:  $t_{\text{CYL}}$  is the oscillation period ( $1/F_c$ ) input to the X0 pin.

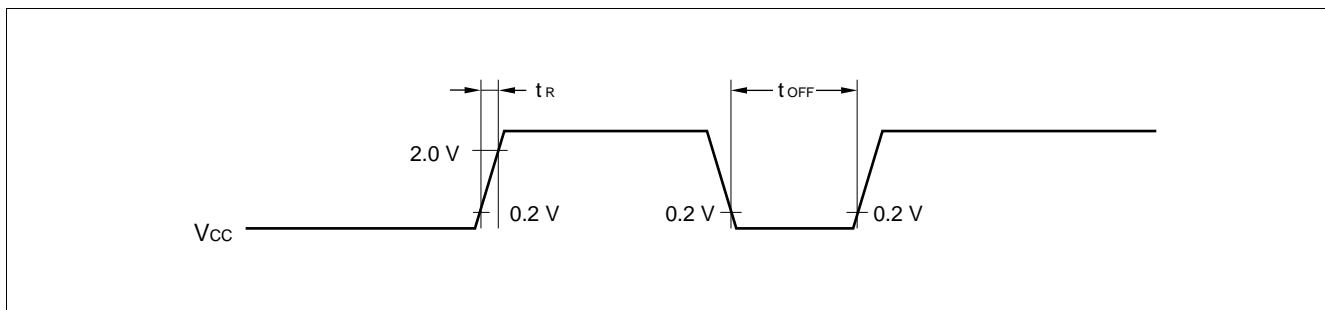


### (2) Power-on Reset

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	$t_{\text{R}}$	—	—	50	ms	
Power supply cut-off time	$t_{\text{OFF}}$	—	1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the oscillation stabilization time selected.  
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



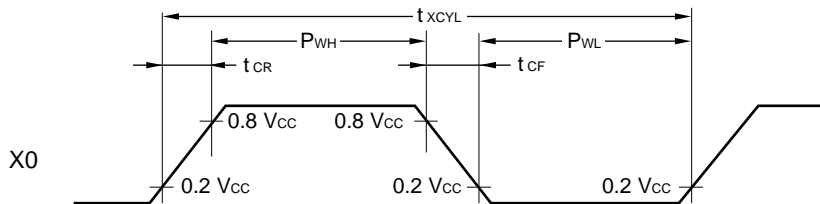
# MB89190/190A Series

## (3) Clock Timings

( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

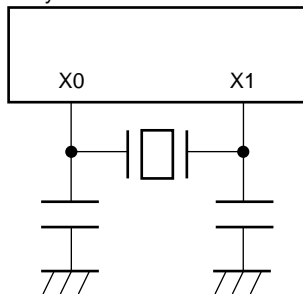
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	$F_C$	X0, X1	—	1	4.2	MHz	
Clock cycle time	$t_{XCYL}$	X0, X1	—	238	1000	ns	
Input clock pulse width	$P_{WH}$ $P_{WL}$	X0	—	20	—	ns	External clock
Input clock pulse rising/falling time	$t_{CR}$ $t_{CF}$	X0	—	—	10	ns	External clock

### X0, X1 Timings and Conditions of Applied Voltage

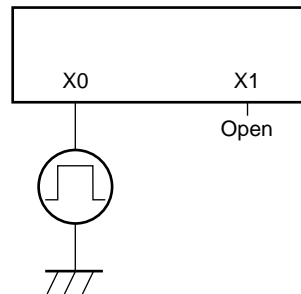


### Clock Conditions

When a crystal or ceramic resonator is used



When an external clock is used



## (4) Instruction Cycles

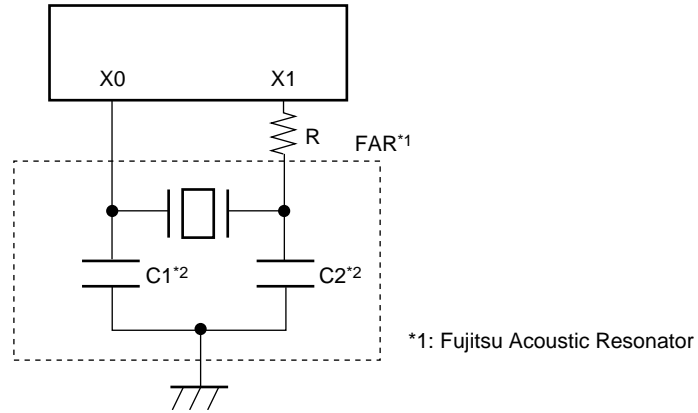
( $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	$t_{inst}$	$4/F_C$	$\mu\text{s}$	$t_{inst} = 0.95 \mu\text{s}$ when operating at $F_C = 4.2 \text{ MHz}$

# MB89190/190A Series

## (5) Recommended Resonator Manufacturers

### • Sample Application of Piezoelectric Resonator (FAR Series)

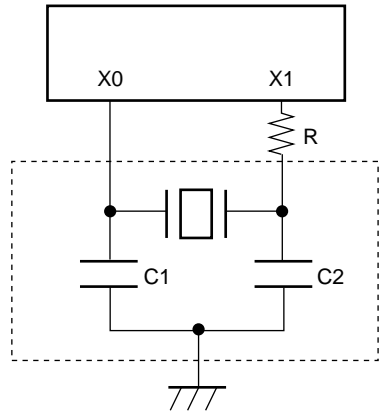


FAR part number (built-in capacitor type)	Frequency (MHz)	Damping resistor	Initial deviation of FAR frequency ( $T_A = +25^\circ\text{C}$ )	Temperature characteristics of FAR frequency ( $T_A = -20^\circ\text{C}$ to $+60^\circ\text{C}$ )	Loading capacitors*2
FAR-C4SA-04000-□01M	4.00	200 $\Omega$	$\pm 0.5\%$	$\pm 0.5\%$	Built-in

Inquiry: FUJITSU LIMITED

# MB89190/190A Series

## • Sample Application of Ceramic Resonator



### • Mask ROM products

Resonator manufacturer*	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg. Co., Ltd.	CSA2.00MG040	2.00	100	100	Not required
	CST2.00MG040		Built-in	Built-in	Not required
	CSA4.00MG	4.00	30	30	Not required
	CST4.00MGW		Built-in	Built-in	Not required
	CSTCS4.00MG0C5		Built-in	Built-in	Not required
TDK. Co., Ltd.	CCR4.0MC3	4.00	Built-in	Built-in	Not required
	FCR4.0MC5		Built-in	Built-in	Not required

### • One-time products

Resonator manufacturer*	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg. Co., Ltd.	CSA3.20MGCA	3.20	30	30	1 kΩ
	CST3.20MGA		Built-in	Built-in	1 kΩ
	CSA3.20MGA040	3.20	100	100	Not required
	CST3.20MGWA040		Built-in	Built-in	Not required
	CSA3.58MGCA	3.58	30	30	Not required
	CST3.58MGWHA		Built-in	Built-in	Not required

Inquiry: Murata Mfg. Co., Ltd

- Murata Electronics North America. Inc.: TEL 1-404-436-1300
- Murata Europe Mangement GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

TDK Corporation

- TDK Corporation of America  
Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH  
Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hongkong Co., Ltd.: TEL 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6633

# MB89190/190A Series

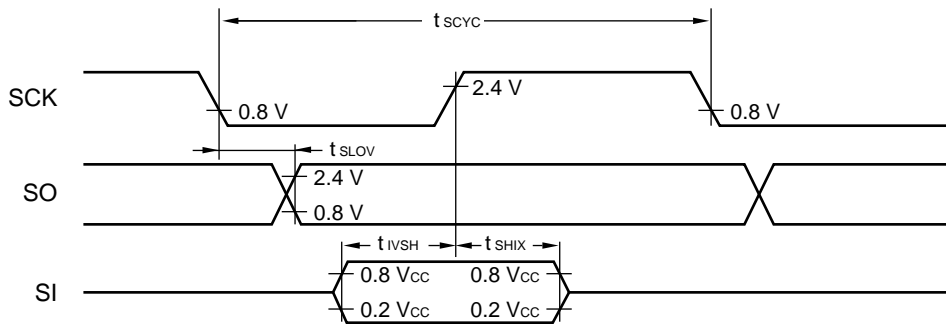
## (6) Serial I/O Timings

( $V_{CC} = 5.0 V \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

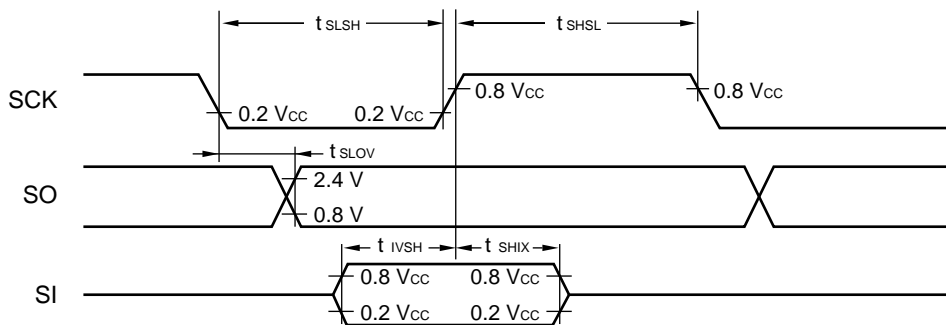
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation	$2 t_{inst}^*$	—	$\mu s$	
SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	SCK, SO		-200	200	ns	
Valid SI $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SI, SCK		$1/2 t_{inst}^*$	—	$\mu s$	
SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	SCK, SI		$1/2 t_{inst}^*$	—	$\mu s$	
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External clock operation	$1 t_{inst}^*$	—	$\mu s$	
Serial clock "L" pulse width	$t_{SLSH}$			$1 t_{inst}^*$	—	$\mu s$	
SCK $\downarrow \rightarrow$ SO time	$t_{SLOV}$	SCK, SO		0	200	ns	
Valid SI $\rightarrow$ SCK $\uparrow$	$t_{IVSH}$	SI, SCK		$1/2 t_{inst}^*$	—	$\mu s$	
SCK $\uparrow \rightarrow$ valid SI hold time	$t_{SHIX}$	SCK, SI	$1/2 t_{inst}^*$	—	$\mu s$		

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycles."

### Internal Shift Clock Mode



### External Shift Clock Mode



# MB89190/190A Series

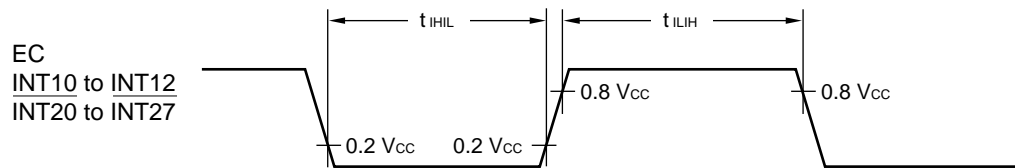
## (7) Peripheral Input Timings

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input "H" pulse width 1	$t_{ILIH1}$	EC, INT10 to INT12, INT20 to INT27	$2 t_{inst}^*$	—	$\mu s$	
Peripheral input "L" pulse width 1	$t_{IHIL1}$		$2 t_{inst}^*$	—	$\mu s$	

\* : For information on  $t_{inst}$ , see "(4) Instruction Cycles."

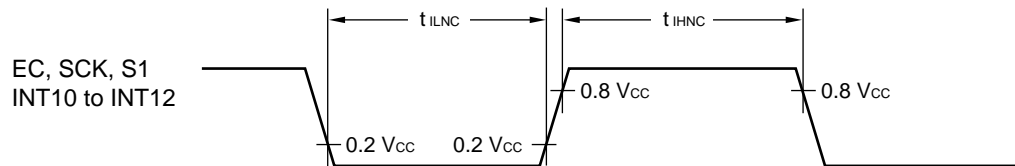
### Peripheral Input Timing Diagram



( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input "H" noise limit width	$t_{IHNC}$	EC, SI, SCK INT10 to INT12	7	15	23	ns	
Peripheral input "L" noise limit width	$t_{ILNC}$	EC, SI, SCK INT10 to INT12	7	15	23	ns	

### Peripheral Input Timing Diagram



# MB89190/190A Series

## 5. A/D Converter Electrical Characteristics (MB89190A Series Only)

( $AV_{CC} = V_{CC} = 3.5 \text{ V to } 6.0 \text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			—	—	±1.5	LSB		
Linearity error			—	—	±1.0	LSB		
Differential linearity error			—	—	±0.9	LSB		
Zero transition voltage	$V_{OT}$	—	$AVR = AV_{CC}$	$AV_{SS}$ -1.0 LSB	$AV_{SS}$ +0.5 LSB	$AV_{SS}$ +2.0 LSB	mV	
Full-scale transition voltage	$V_{FST}$			$AVR$ -3.0 LSB	$AVR$ -1.5 LSB	$AVR$	mV	
Inter channel disparity	—			—	—	0.5	LSB	
A/D mode conversion time	—	—	—	—	$44 t_{inst}^*$	—	$\mu\text{s}$	
Sense mode conversion time	—			—	$12 t_{inst}^*$	—	$\mu\text{s}$	
Analog port input current	$I_{AIN}$	AN0 to AN7	—	—	—	10	$\mu\text{A}$	
Analog input voltage	—	—	—	0	—	$AVR$	V	
Reference voltage	—			0	—	$V_{CC}$	V	
Reference voltage supply current	$I_R$	AVR	$AVR = V_{CC} = 5.0 \text{ V}$ when A/D conversion is operating	—	100	300	$\mu\text{A}$	
	$I_{RH}$			—	—	1	$\mu\text{A}$	

\* : For information on  $t_{inst}$ , see “(4) Instruction Cycles” in “4. AC Characteristics.”

## 6. A/D Converter Glossary

- Resolution

Analog changes that are identifiable by the A/D converter.

When the number of bits is 8, analog voltage can be divided into  $2^8=256$ .

Linearity error (unit: LSB)

The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1110” ↔ “1111 1111”) from actual conversion characteristics.

Differential linearity error (unit: LSB)

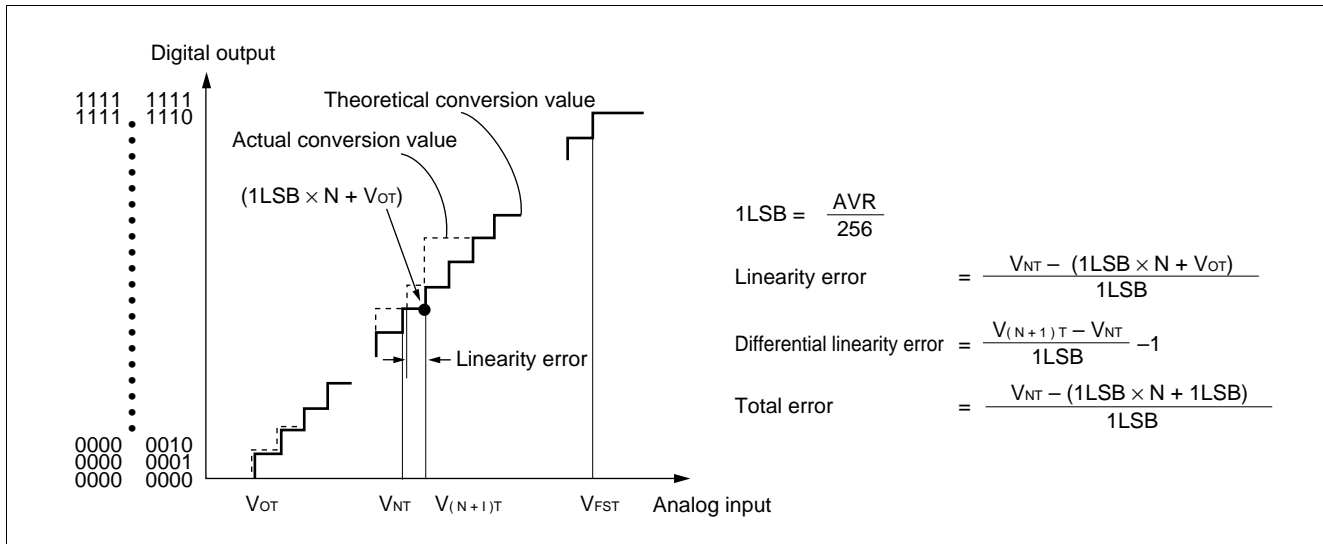
The deviation of input voltage needed change the output code by 1 LSB from the theoretical value.

- Total error (unit: LSB)

The difference between theoretical and actual conversion values.



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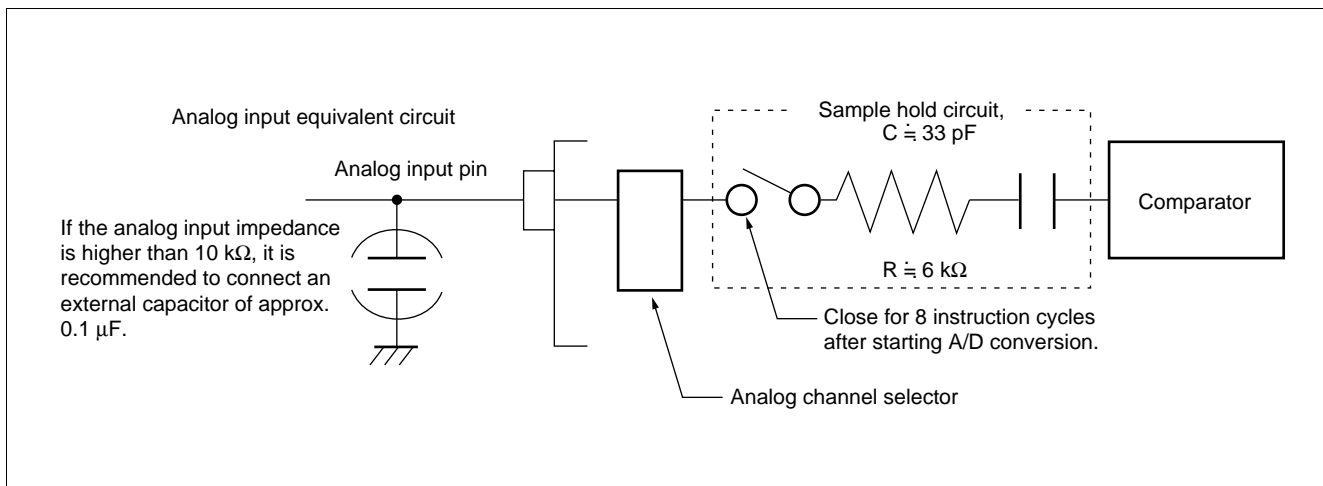
## 7. Notes on Using A/D Converter

### • Input impedance of analog input pins

The A/D converter used for the MB89190A series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after starting A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 k $\Omega$ ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of approx. 0.1  $\mu\text{F}$  for the analog input pin.



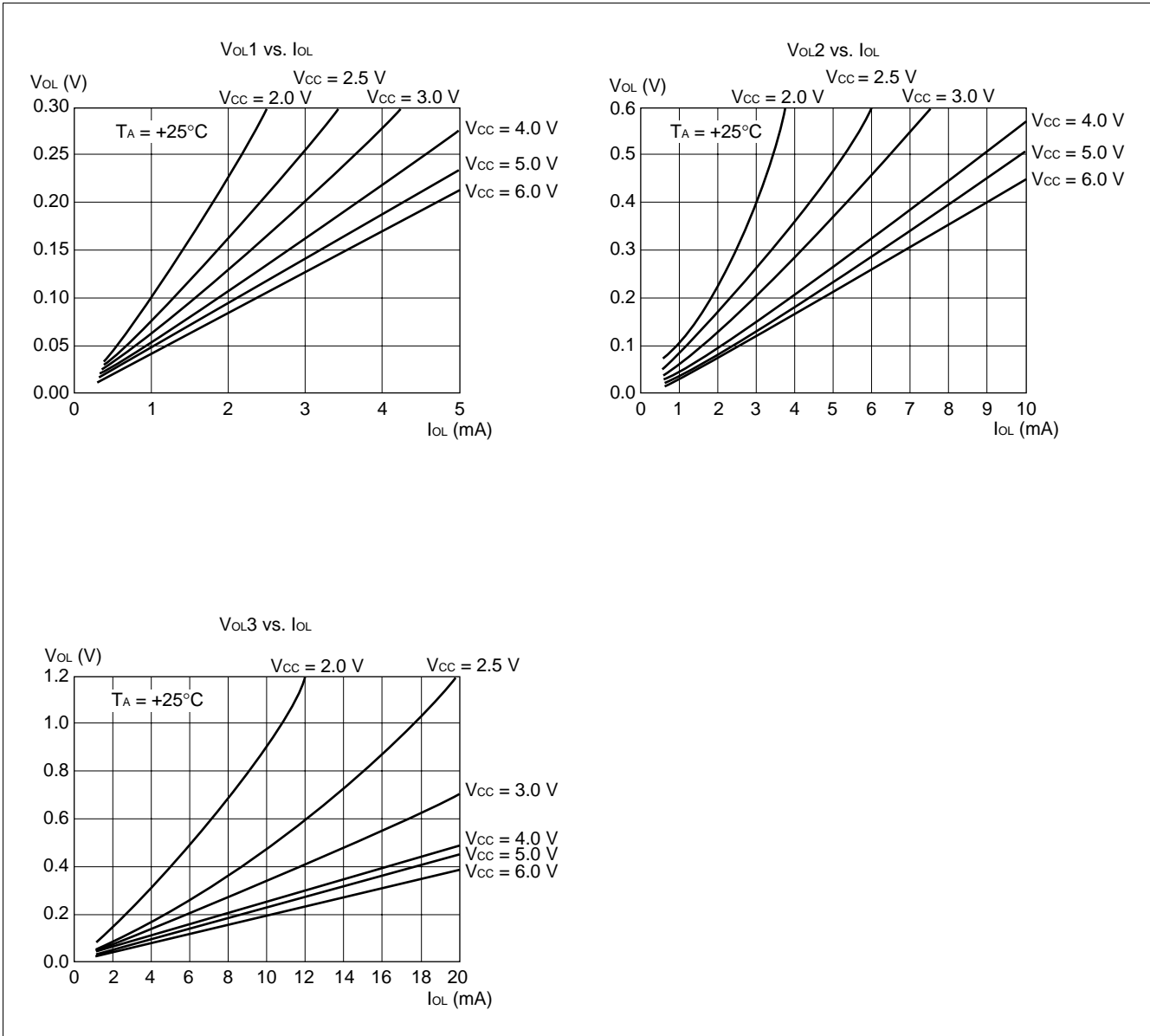
### • Error

The smaller the  $|AVR - AV_{SS}|$ , the greater the error would become relatively.

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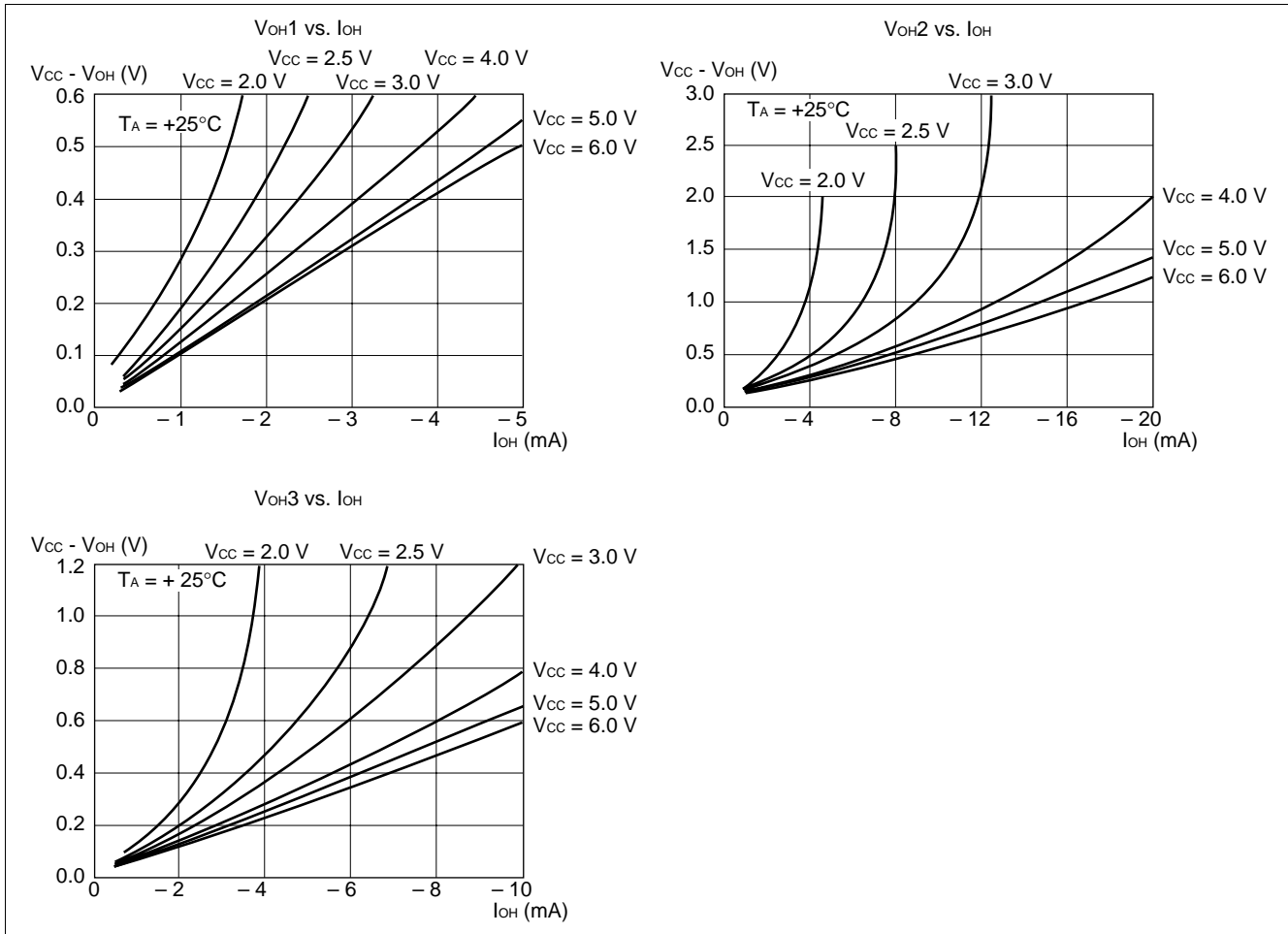
## EXAMPLE CHARACTERISTICS

### (1) "L" Level Output Voltage

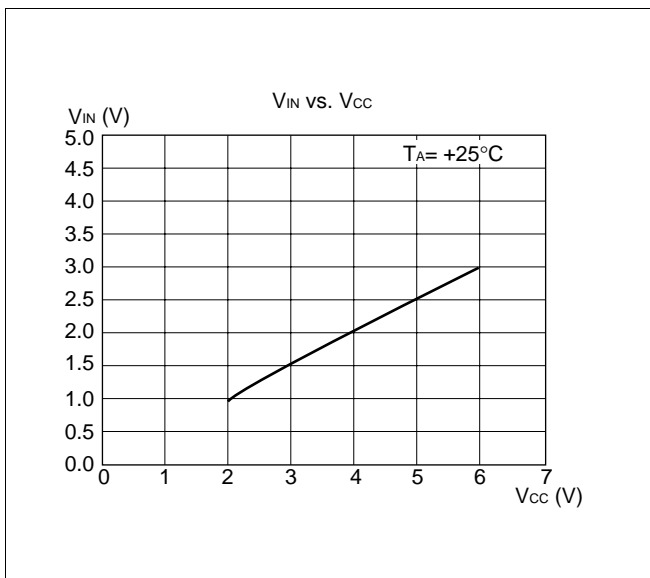


# MB89190/190A Series

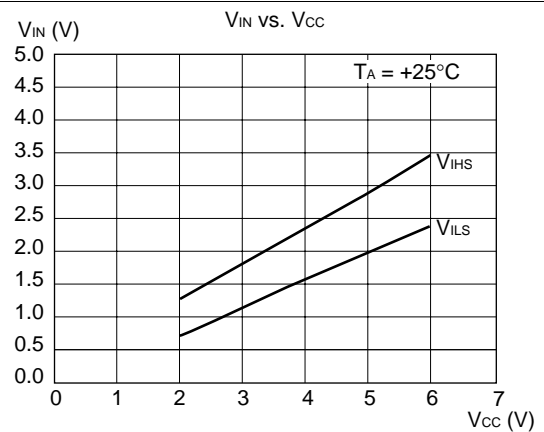
## (2) "H" Level Output Voltage



## (3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



## (4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

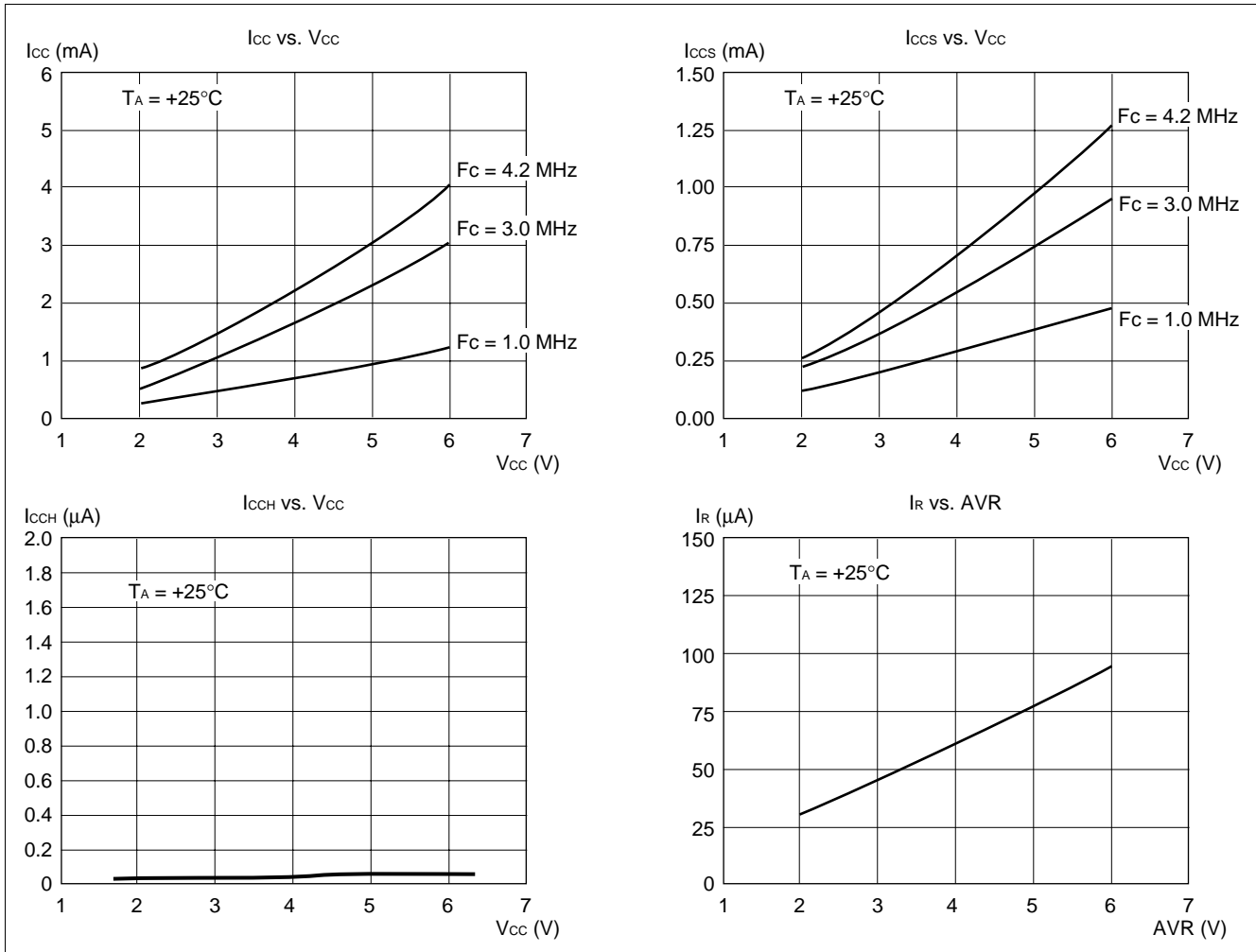


$V_{IHS}$ : Threshold when input voltage in hysteresis characteristics is set to "H" level

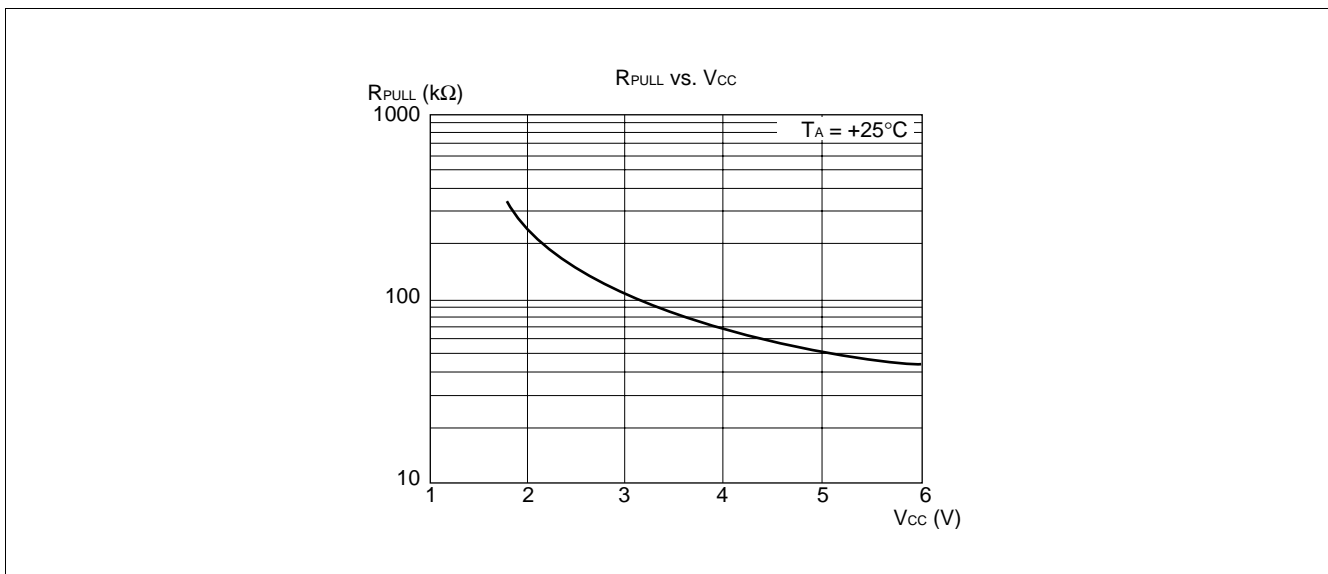
$V_{ILS}$ : Threshold when input voltage in hysteresis characteristics is set to "L" level

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## (5) Power Supply Current (External Clock)



## (6) Pull-up Resistance



# MB89190/190A Series

## ■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

**Table 1 Instruction Symbols**

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

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Columns indicate the following:

Mnemonic:	Assembler notation of an instruction
~:	The number of instructions
#:	The number of bytes
Operation:	Operation of an instruction
TL, TH, AH:	<p>A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:</p> <ul style="list-style-type: none"><li>• “-” indicates no change.</li><li>• dH is the 8 upper bits of operation description data.</li><li>• AL and AH must become the contents of AL and AH prior to the instruction executed.</li><li>• 00 becomes 00.</li></ul>
N, Z, V, C:	An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.
OP code:	<p>Code of an instruction. If an instruction is more than one code, it is written according to the following rule:</p> <p>Example: 48 to 4F ← This indicates 48, 49, ... 4F.</p>

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Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
MOV dir,A	3	2	(dir) ← (A)	-	-	-	----	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	-	-	-	----	46
MOV ext,A	4	3	(ext) ← (A)	-	-	-	----	61
MOV @EP,A	3	1	((EP)) ← (A)	-	-	-	----	47
MOV Ri,A	3	1	(Ri) ← (A)	-	-	-	----	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	-	-	++--	04
MOV A,dir	3	2	(A) ← (dir)	AL	-	-	++--	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	-	-	++--	06
MOV A,ext	4	3	(A) ← (ext)	AL	-	-	++--	60
MOV A,@A	3	1	(A) ← ((A))	AL	-	-	++--	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	-	-	++--	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	-	-	++--	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	-	-	-	----	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	-	-	-	----	86
MOV @EP,#d8	4	2	((EP)) ← d8	-	-	-	----	87
MOV Ri,#d8	4	2	(Ri) ← d8	-	-	-	----	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	-	-	-	----	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	-	-	-	----	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	-	-	-	----	D4
MOVW @EP,A	4	1	((EP)) ← (AH),(EP + 1) ← (AL)	-	-	-	----	D7
MOVW EP,A	2	1	(EP) ← (A)	-	-	-	----	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	++--	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	++--	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	++--	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	++--	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A) + 1)	AL	AH	dH	++--	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	++--	C7
MOVW A,EP	2	1	(A) ← (EP)	-	-	dH	----	F3
MOVW EP,#d16	3	3	(EP) ← d16	-	-	-	----	E7
MOVW IX,A	2	1	(IX) ← (A)	-	-	-	----	E2
MOVW A,IX	2	1	(A) ← (IX)	-	-	dH	----	F2
MOVW SP,A	2	1	(SP) ← (A)	-	-	-	----	E1
MOVW A,SP	2	1	(A) ← (SP)	-	-	dH	----	F1
MOV @A,T	3	1	((A)) ← (T)	-	-	-	----	82
MOVW @A,T	4	1	((A)) ← (TH),(A + 1) ← (TL)	-	-	-	----	83
MOVW IX,#d16	3	3	(IX) ← d16	-	-	-	----	E6
MOVW A,PS	2	1	(A) ← (PS)	-	-	dH	----	70
MOVW PS,A	2	1	(PS) ← (A)	-	-	-	++++	71
MOVW SP,#d16	3	3	(SP) ← d16	-	-	-	----	E5
SWAP	2	1	(AH) ↔ (AL)	-	-	AL	----	10
SETB dir: b	4	2	(dir): b ← 1	-	-	-	----	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	-	-	-	----	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	-	-	----	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	----	43
XCHW A,EP	3	1	(A) ↔ (EP)	-	-	dH	----	F7
XCHW A,IX	3	1	(A) ↔ (IX)	-	-	dH	----	F6
XCHW A,SP	3	1	(A) ↔ (SP)	-	-	dH	----	F5
MOVW A,PC	2	1	(A) ← (PC)	-	-	dH	----	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.

- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F<sup>2</sup>MC-8 family)

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**Table 3 Arithmetic Operation Instructions (62 instructions)**

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
ADDC A,Ri	3	1	$(A) \leftarrow (A) + (Ri) + C$	-	-	-	++++	28 to 2F
ADDC A,#d8	2	2	$(A) \leftarrow (A) + d8 + C$	-	-	-	++++	24
ADDC A,dir	3	2	$(A) \leftarrow (A) + (dir) + C$	-	-	-	++++	25
ADDC A,@IX +off	4	2	$(A) \leftarrow (A) + ((IX) + off) + C$	-	-	-	++++	26
ADDC A,@EP	3	1	$(A) \leftarrow (A) + ((EP)) + C$	-	-	-	++++	27
ADDCW A	3	1	$(A) \leftarrow (A) + (T) + C$	-	-	dH	++++	23
ADDC A	2	1	$(AL) \leftarrow (AL) + (TL) + C$	-	-	-	++++	22
SUBC A,Ri	3	1	$(A) \leftarrow (A) - (Ri) - C$	-	-	-	++++	38 to 3F
SUBC A,#d8	2	2	$(A) \leftarrow (A) - d8 - C$	-	-	-	++++	34
SUBC A,dir	3	2	$(A) \leftarrow (A) - (dir) - C$	-	-	-	++++	35
SUBC A,@IX +off	4	2	$(A) \leftarrow (A) - ((IX) + off) - C$	-	-	-	++++	36
SUBC A,@EP	3	1	$(A) \leftarrow (A) - ((EP)) - C$	-	-	-	++++	37
SUBCW A	3	1	$(A) \leftarrow (T) - (A) - C$	-	-	dH	++++	33
SUBC A	2	1	$(AL) \leftarrow (TL) - (AL) - C$	-	-	-	++++	32
INC Ri	4	1	$(Ri) \leftarrow (Ri) + 1$	-	-	-	+++-	C8 to CF
INCW EP	3	1	$(EP) \leftarrow (EP) + 1$	-	-	-	----	C3
INCW IX	3	1	$(IX) \leftarrow (IX) + 1$	-	-	-	----	C2
INCW A	3	1	$(A) \leftarrow (A) + 1$	-	-	dH	+- - -	C0
DEC Ri	4	1	$(Ri) \leftarrow (Ri) - 1$	-	-	-	+++-	D8 to DF
DECW EP	3	1	$(EP) \leftarrow (EP) - 1$	-	-	-	----	D3
DECW IX	3	1	$(IX) \leftarrow (IX) - 1$	-	-	-	----	D2
DECW A	3	1	$(A) \leftarrow (A) - 1$	-	-	dH	+- - -	D0
MULU A	19	1	$(A) \leftarrow (AL) \times (TL)$	-	-	dH	----	01
DIVU A	21	1	$(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$	dL	00	00	----	11
ANDW A	3	1	$(A) \leftarrow (A) \wedge (T)$	-	-	dH	++R-	63
ORW A	3	1	$(A) \leftarrow (A) \vee (T)$	-	-	dH	++R-	73
XORW A	3	1	$(A) \leftarrow (A) \nabla (T)$	-	-	dH	++R-	53
CMP A	2	1	$(TL) - (AL)$	-	-	-	++++	12
CMPW A	3	1	$(T) - (A)$	-	-	-	++++	13
RORC A	2	1	$\rightarrow C \rightarrow A$	-	-	-	++-+	03
ROLC A	2	1	$\leftarrow C \leftarrow A$	-	-	-	++-+	02
CMP A,#d8	2	2	$(A) - d8$	-	-	-	++++	14
CMP A,dir	3	2	$(A) - (dir)$	-	-	-	++++	15
CMP A,@EP	3	1	$(A) - ((EP))$	-	-	-	++++	17
CMP A,@IX +off	4	2	$(A) - ((IX) + off)$	-	-	-	++++	16
CMP A,Ri	3	1	$(A) - (Ri)$	-	-	-	++++	18 to 1F
DAA	2	1	Decimal adjust for addition	-	-	-	++++	84
DAS	2	1	Decimal adjust for subtraction	-	-	-	++++	94
XOR A	2	1	$(A) \leftarrow (AL) \nabla (TL)$	-	-	-	++R-	52
XOR A,#d8	2	2	$(A) \leftarrow (AL) \nabla d8$	-	-	-	++R-	54
XOR A,dir	3	2	$(A) \leftarrow (AL) \nabla (dir)$	-	-	-	++R-	55
XOR A,@EP	3	1	$(A) \leftarrow (AL) \nabla ((EP))$	-	-	-	++R-	57
XOR A,@IX +off	4	2	$(A) \leftarrow (AL) \nabla ((IX) + off)$	-	-	-	++R-	56
XOR A,Ri	3	1	$(A) \leftarrow (AL) \nabla (Ri)$	-	-	-	++R-	58 to 5F
AND A	2	1	$(A) \leftarrow (AL) \wedge (TL)$	-	-	-	++R-	62
AND A,#d8	2	2	$(A) \leftarrow (AL) \wedge d8$	-	-	-	++R-	64
AND A,dir	3	2	$(A) \leftarrow (AL) \wedge (dir)$	-	-	-	++R-	65

(Continued)



## MB89190/190A Series

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
AND A,@EP	3	1	$(A) \leftarrow (AL) \wedge ((EP))$	-	-	-	++R-	67
AND A,@IX +off	4	2	$(A) \leftarrow (AL) \wedge ((IX) +off)$	-	-	-	++R-	66
AND A,Ri	3	1	$(A) \leftarrow (AL) \wedge (Ri)$	-	-	-	++R-	68 to 6F
OR A	2	1	$(A) \leftarrow (AL) \vee (TL)$	-	-	-	++R-	72
OR A,#d8	2	2	$(A) \leftarrow (AL) \vee d8$	-	-	-	++R-	74
OR A,dir	3	2	$(A) \leftarrow (AL) \vee (dir)$	-	-	-	++R-	75
OR A,@EP	3	1	$(A) \leftarrow (AL) \vee ((EP))$	-	-	-	++R-	77
OR A,@IX +off	4	2	$(A) \leftarrow (AL) \vee ((IX) +off)$	-	-	-	++R-	76
OR A,Ri	3	1	$(A) \leftarrow (AL) \vee (Ri)$	-	-	-	++R-	78 to 7F
CMP dir,#d8	5	3	$(dir) - d8$	-	-	-	++++	95
CMP @EP,#d8	4	2	$((EP)) - d8$	-	-	-	++++	97
CMP @IX +off,#d8	5	3	$((IX) +off) - d8$	-	-	-	++++	96
CMP Ri,#d8	4	2	$(Ri) - d8$	-	-	-	++++	98 to 9F
INCW SP	3	1	$(SP) \leftarrow (SP) + 1$	-	-	-	----	C1
DECW SP	3	1	$(SP) \leftarrow (SP) - 1$	-	-	-	----	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
BZ/BEQ rel	3	2	If $Z = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FD
BNZ/BNE rel	3	2	If $Z = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FC
BC/BLO rel	3	2	If $C = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	F9
BNC/BHS rel	3	2	If $C = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	F8
BN rel	3	2	If $N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FB
BP rel	3	2	If $N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FA
BLT rel	3	2	If $V \vee N = 1$ then $PC \leftarrow PC + rel$	-	-	-	----	FF
BGE rel	3	2	If $V \vee N = 0$ then $PC \leftarrow PC + rel$	-	-	-	----	FE
BBC dir: b,rel	5	3	If $(dir: b) = 0$ then $PC \leftarrow PC + rel$	-	-	-	-+---	B0 to B7
BBS dir: b,rel	5	3	If $(dir: b) = 1$ then $PC \leftarrow PC + rel$	-	-	-	-+---	B8 to BF
JMP @A	2	1	$(PC) \leftarrow (A)$	-	-	-	----	E0
JMP ext	3	3	$(PC) \leftarrow ext$	-	-	-	----	21
CALLV #vct	6	1	Vector call	-	-	-	----	E8 to EF
CALL ext	6	3	Subroutine call	-	-	-	----	31
XCHW A,PC	3	1	$(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$	-	-	dH	----	F4
RET	4	1	Return from subroutine	-	-	-	----	20
RETI	6	1	Return from interrupt	-	-	-	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	NZVC	OP code
PUSHW A	4	1		-	-	-	----	40
POPW A	4	1		-	-	dH	----	50
PUSHW IX	4	1		-	-	-	----	41
POPW IX	4	1		-	-	-	----	51
NOP	1	1		-	-	-	----	00
CLRC	1	1		-	-	-	----R	81
SETC	1	1		-	-	-	----S	91
CLRI	1	1		-	-	-	----	80
SETI	1	1		-	-	-	----	90

# MB89190/190A Series

## INSTRUCTION MAP

L	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLR A	SETI	CLR dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC	
1	MULLU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLR dir: 1	SETC	CLR dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SPA	MOVW A,SP	
2	ROL A	CMP A	ADDC A	SUBC A	XCH A,T	XOR A,T	AND A	OR A	MOV @A,T	MOV @A,T	MOV A,@A	CLR dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A,T	XORW A,T	ANDW A	ORW A	MOVW @A,T	MOVW @A,T	MOVW A,@A	CLR dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EPA	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8	XOR A,#d8	XOR A,#d8	AND A,#d8	OR A,#d8	DAA A,#d8	DAS	MOV dir:#d8	CLR dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	XOR A,dir	MOV dir,A	AND A,dir	OR A,dir	MOV dir:#d8	CMP dir:#d8	CMP dir:#d8	CLR dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX+d	CMP A,@IX+d	ADDC A,@IX+d	SUBC A,@IX+d	XOR A,@IX+d	MOV @IX+d,A	AND A,@IX+d	OR A,@IX+d	MOV @IX+d:#d8	CMP @IX+d:#d8	CMP @IX+d:#d8	CLR dir: 6	BBC dir: 6,rel	MOVW A,@IX+d	MOVW @IX+d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	XOR A,@EP	MOV @EPA	AND A,@EP	OR A,@EP	MOV @EP:#d8	CMP @EP:#d8	CMP @EP:#d8	CLR dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EPA	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	XOR R0,A	MOV R0,A	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	XOR R1,A	MOV R1,A	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	XOR R2,A	MOV R2,A	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	XOR R3,A	MOV R3,A	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	XOR R4,A	MOV R4,A	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	XOR R5,A	MOV R5,A	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	XOR R6,A	MOV R6,A	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	XOR R7,A	MOV R7,A	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

# MB89190/190A Series

## ■ MASK OPTION LIST

No.	Part number		MB89191 MB89193 MB89195	MB89191A MB89193A MB89195A	MB89P195		MB89P195A		MB89PV190 MB89PV190A
	Specifying procedure		Specify when ordering masking		-101 <sup>*2</sup>	Specify when ordering masking		-201 <sup>*2</sup>	Fixed
1	Port pull-up resistors	P00 to P07 P30 to P37	Selectable by pin		None	Selectable by pin		None	Not available
		P00 to P03 P40 to P45	Selectable by pin	Not available	None	Selectable by pin	Not available	None	Not available
2	Power-on reset <ul style="list-style-type: none"> <li>Power-on reset provided</li> <li>No power-on reset</li> </ul>		Selectable		Provided	Provided		Provided	Provided
3	Selection of oscillation stabilization wait time (at 4.2 MHz) <sup>*1</sup> <ul style="list-style-type: none"> <li><math>2^{18}/F_c</math> (approx. 62.4 ms)</li> <li><math>2^{16}/F_c</math> (approx. 15.6 ms)</li> <li><math>2^{12}/F_c</math> (approx. 0.98 ms)</li> <li><math>2^2/F_c</math> (approx. 0 ms)</li> </ul>		Selectable		Fixed to $2^{16}/F_c$	Selectable		Fixed to $2^{16}/F_c$	Fixed to $2^{16}/F_c$
4	Reset pin output <ul style="list-style-type: none"> <li>Reset output provided</li> <li>No reset output</li> </ul>		Selectable		Provided	Selectable		Provided	Provided
5	Oscillation type of clock <ul style="list-style-type: none"> <li>1 Crystal and ceramic oscillators</li> <li>2 CR</li> </ul>		Selectable		"1" only	Selectable		"1" only	"1" only

\*1: The oscillation stabilization time is generated by dividing the original clock oscillation. The time described in this item should be used as a rough guideline since the oscillation cycle is unstable immediately after oscillation starts. "Fc" indicates the original oscillation frequency.

\*2: -101 and -201 are provided respectively for the MB89P195 and MB89P195A OTP versions as the standard products.

# MB89190/190A Series

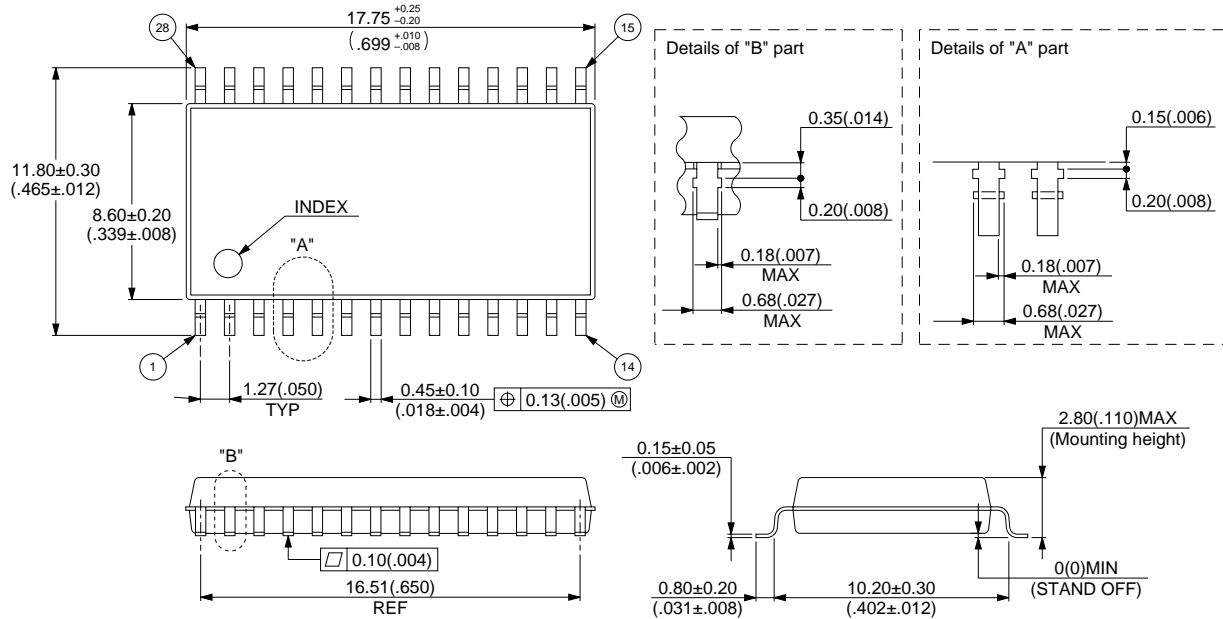
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB89191PF MB89193PF MB89195PF MB89P195PF-101 MB89191APF MB89191AHPF MB89193APF MB89193AHPF MB89195APF MB89P195APF-201	28-pin Plastic SOP (FPT-28P-M17)	
MB89191P-SH MB89193P-SH MB89195P-SH MB89191AP-SH MB89191AHP-SH MB89193AP-SH MB89193AHP-SH MB89195AP-SH	28-pin Plastic SH-DIP (DIP-28C-M03)	
MB89191P MB89193P MB89195P MB89P195P-101 MB89191AP MB89191AHP MB89193AP MB89193AHP MB89195AP MB89P195AP-201	28-pin Plastic DIP (DIP-28P-M05)	
MB89PV190CF MB89PV190ACF	48-pin Ceramic MQFP (MQP-48C-P01)	

# MB89190/190A Series

## ■ PACKAGE DIMENSION

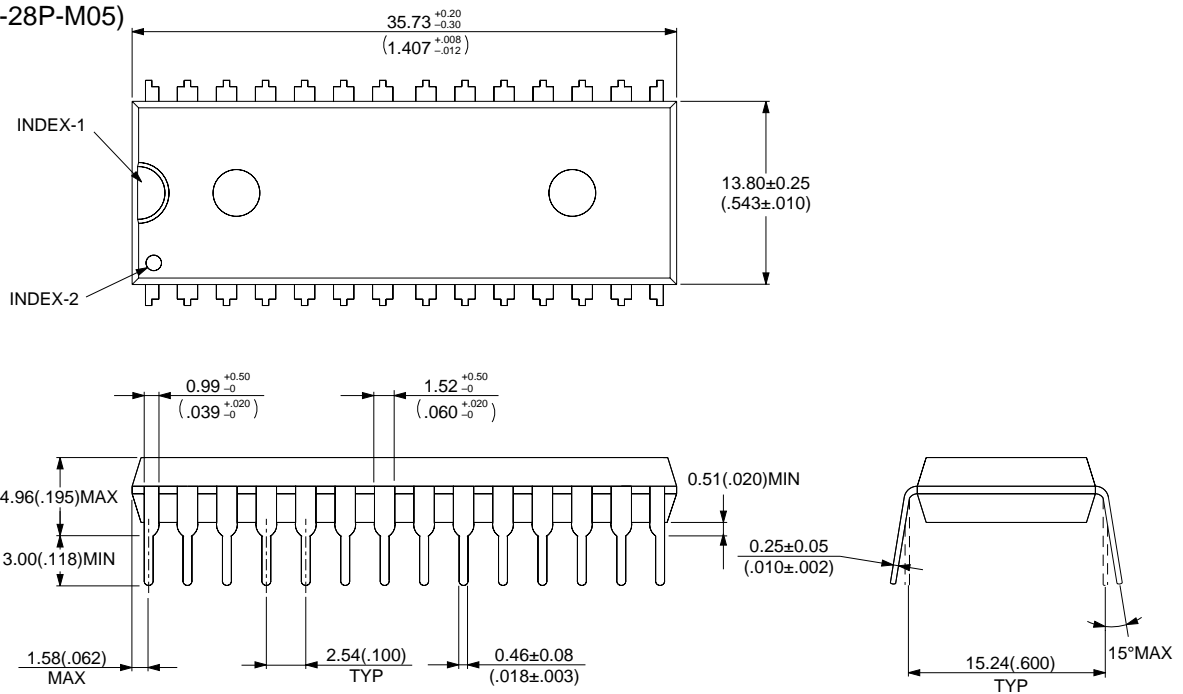
28-pin Plastic SOP  
(FPT-28P-M17)



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Dimensions in mm (inches)

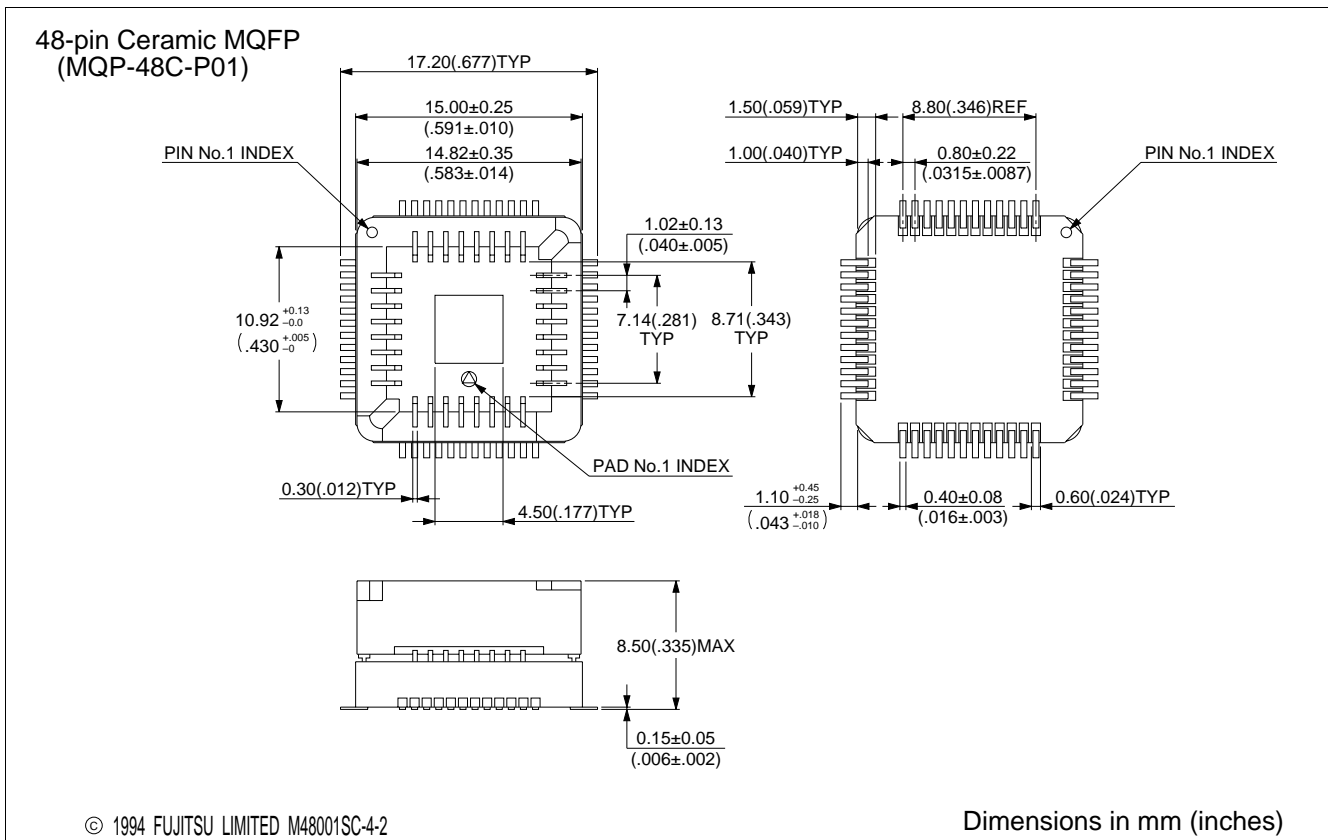
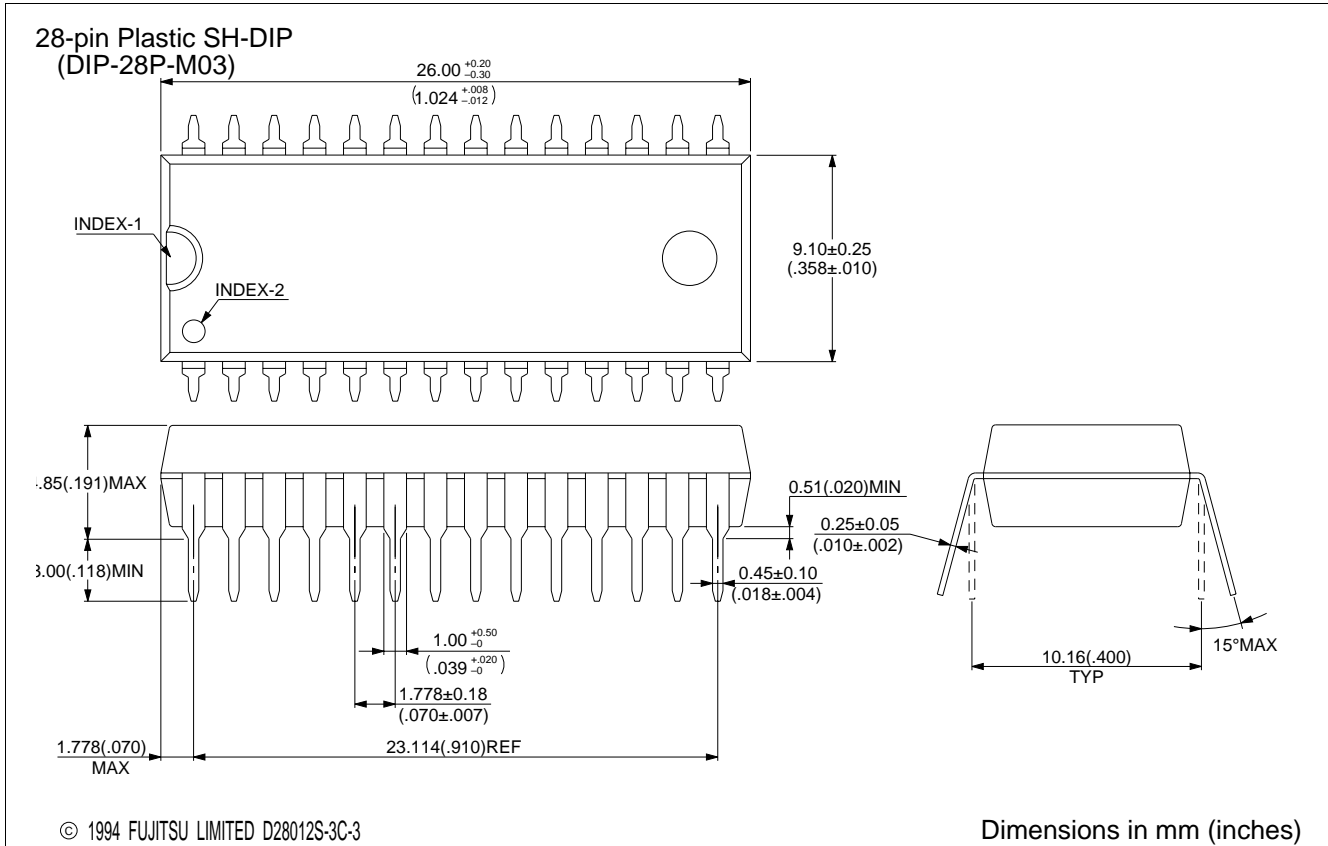
28-pin Plastic DIP  
(DIP-28P-M05)



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Dimensions in mm (inches)

# MB89190/190A Series



# MB89190/190A Series

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