FUJITSU SEMICONDUCTOR
DATA SHEET

ASSP Magnetic Disk

BIPOLAR

Read/Write Amplifier
(For HDD MR and Thin Film Composite Heads, 6 Channels)
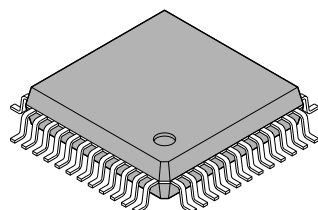
MB4138

■ **DESCRIPTION**

The MB4138 is a 6-channel read/write amplifier IC for magneto-resistive (MR) and inductive thin film composite heads used in hard disk drives.

■ **FEATURES**

- Drives six MR and thin film composite heads.
- The bias current for the MR head can be set in the range of 5 to 12 mA (DC).
- The read signal from the MR head is directly connected to the internal differential amplifier.
- High gain (×150), low noise (0.51 nV/$\sqrt{Hz}$) read amplifier
- Read amplifier output buffer type: open collector.
- Voltage output function pin for MR heads (VHR)
- VHR pin ground fault protection function
- Read output voltage stabilization at mode switching
- Psuedo-ECL level differential input for write data
- The write current can be set in the range from 10 to 40 mA (DC).
- Internal write-unsafe detect circuit. Detects write head faults.
- TTL level control inputs
- Internal voltage monitor detects low supply voltage
- Operates on a single +5.0V power supply.
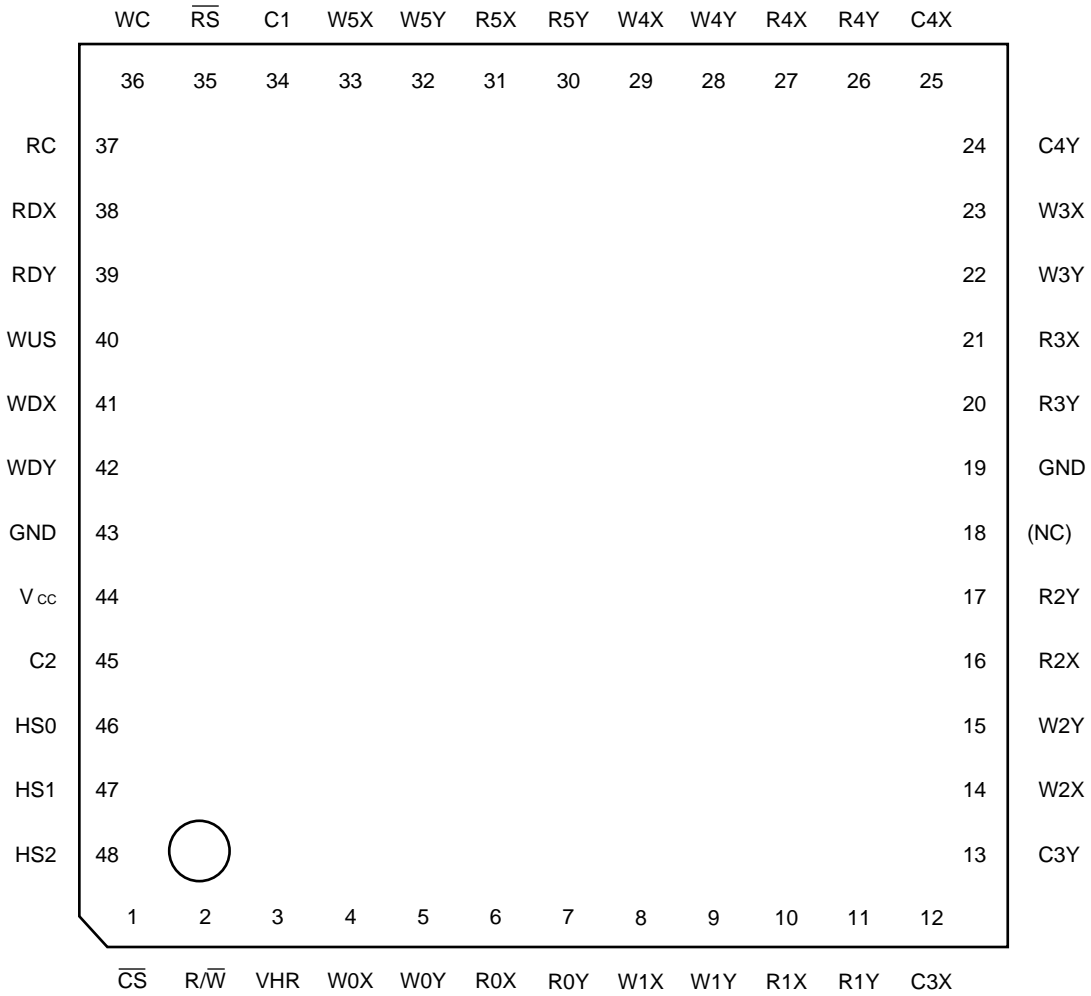
■ **PACKAGE**

48 pin, Plastic QFP

(FPT-48P-M13)

MB4138

■ PIN ASSIGNMENT

(TOP VIEW)

WC	$\overline{RS}$	C1	W5X	W5Y	R5X	R5Y	W4X	W4Y	R4X	R4Y	C4X
36	35	34	33	32	31	30	29	28	27	26	25

Left	Pin		Pin	Right
RC	37		24	C4Y
RDX	38		23	W3X
RDY	39		22	W3Y
WUS	40		21	R3X
WDX	41		20	R3Y
WDY	42		19	GND
GND	43		18	(NC)
V$_{CC}$	44		17	R2Y
C2	45		16	R2X
HS0	46		15	W2Y
HS1	47		14	W2X
HS2	48		13	C3Y

1	2	3	4	5	6	7	8	9	10	11	12
$\overline{CS}$	R/$\overline{W}$	VHR	W0X	W0Y	R0X	R0Y	W1X	W1Y	R1X	R1Y	C3X

(FPT-48P-M13)

MB4138

■ PIN DESCRIPTION

Pin no.	Symbol	Description
1	$\overline{CS}$	Chip select pin. Control signal input pin. Sets the IC to the operating or idle state. An "L" level input sets the IC to "operating".
2	R/$\overline{W}$	Read/write mode selection pin
3	VHR	Output pin for the MR head voltage function. Outputs the same voltage as the bias voltage for the MR heads.
4 to 11, 14 to 17, 20 to 23, 26 to 33	W0X, W0Y R0X, R0Y W1X, W1Y R1X, R1Y to W5X, W5Y R5X, R5Y	Head connection pins for channels 0 to 5. Pins W0X, W0Y, etc. are for the thin film write heads for each channel. Pins R0X, R0Y, etc. are for the MR read heads for each channel. The MR head bias current flows from the R0X pin to the R0Y pin. The read signals are input to a differential amplifier.
12	C3X	Capacitor connection pins. A 0.033 µF capacitor is typically connected between these pins. The capacitor cuts the DC component that occurs when a bias current flows through an MR head.
13	C3Y	
19	GND	Ground pin. Connect to ground.
24	C4X	Capacitor connection pins. Connect a 0.033 µF capacitor between these pins. The capacitor cuts the DC component due to the bias current flowing through the MR heads.
25	C4Y	
34	C1	Capacitor connection pin. Connect a 0.1 µF capacitor between this pin and ground. The capacitor stabilizes the current source circuit and reduces noise.
35	$\overline{RS}$	ON/OFF switching pin for the MR head bias current in write mode. Normally fix this pin at the "L" level (bias current ON) to reduce the duration of the transient when switching from write mode to read mode.
36	WC	Resistor connection pin for setting the write current.
37	RC	Resistor connection pin for setting the MR head bias current.
38	RDX	Differential amplifier output pins for the read data. As the output is an open-collector type, connect 100W resistors between each of these pins and Vcc.
39	RDY	
40	WUS	Write fault detect pin. Outputs an "H" level when a write fault occurs. As the output is an open-collector type, connect a pull-up resistor.
41	WDX	Write data differential input pins. The input level is pseudo-ECL. Input the differential signals to these pins.
42	WDY	
43	GND	Ground pin. Connect to ground.
44	Vcc	Power supply pin. Connect to a +5.0V supply.
45	C2	Capacitor connection pin. Connect a 0.1 mF capacitor between this pin and VCC. The capacitor stabilizes the current source circuit and reduces noise.
46 to 48	HS0, HS1, HS2	Channel 0 to 5 head select pins. See the "n Functions" section for the decoding logic. The input level is TTL.

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■ BLOCK DIAGRAM

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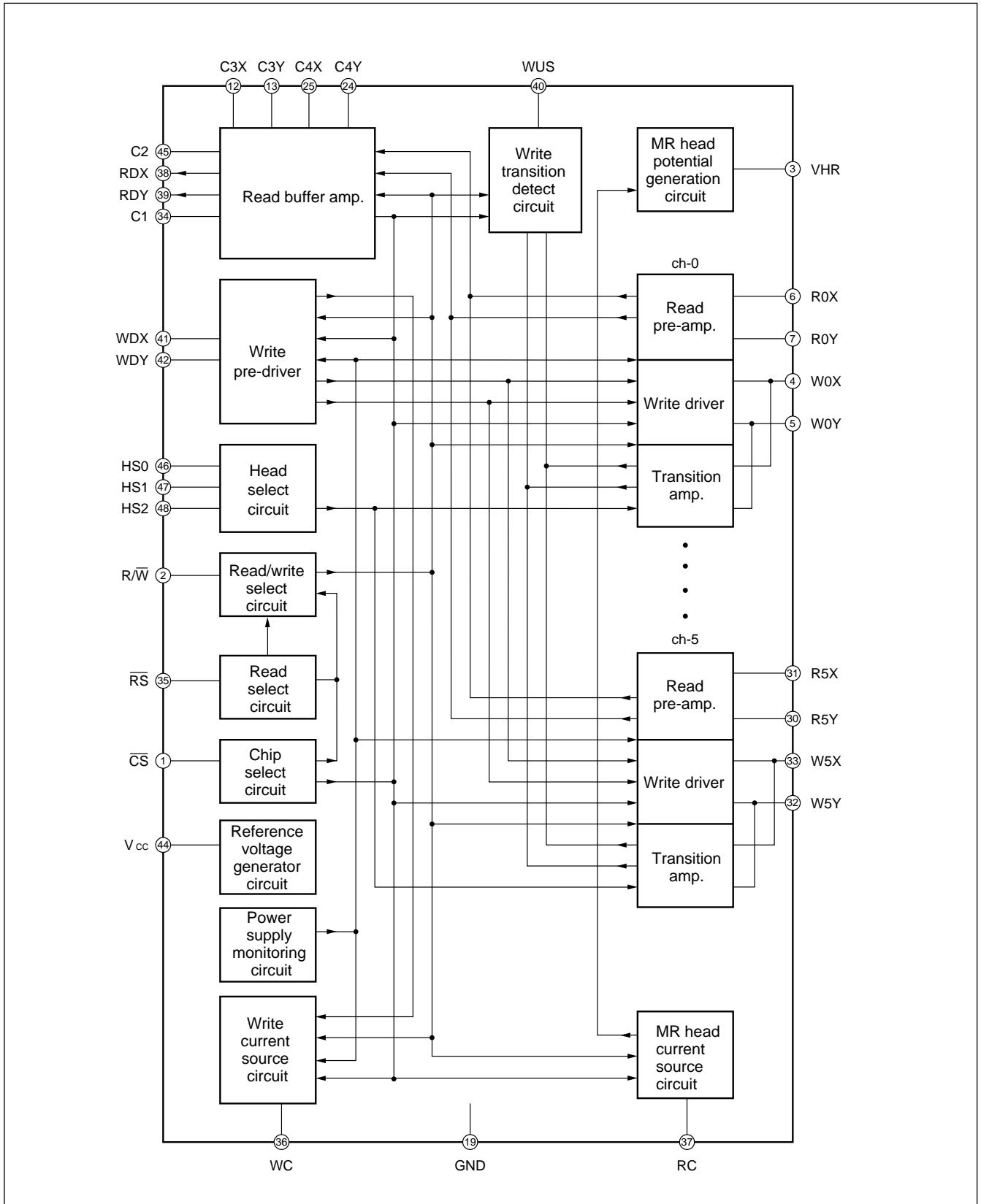
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	−0.3	+7.0	V	
Digital input voltage	V_{IN}	−0.3	V_{CC}+0.3	V	WDX/Y, HS0 to 2, $\overline{CS}$, R/$\overline{W}$, $\overline{RS}$
Head input voltage	V_{HEAD}	−0.3	V_{CC}+0.3	V	
RDX, RDY output voltage	V_{RDX}, V_{RDY}	−0.3	V_{CC}+0.3	V	
WUS output voltage	V_{WUS}	−0.3	V_{CC}+0.3	V	
WUS output current	I_{WUS}	—	10	mA	
Write current	I_W	—	45	mA	
MR head bias current	I_R	—	15	mA	
Storage temperature	T_{stg}	−55	+125	°C	

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	4.50	5.50	V	5.0V±10%
Write current	I_W	10	40	mA	
Write current setting resistor	R_{WC}	24	91	Ω	
MR head bias current	I_R	5	12	mA	
MR head resistor	R_{MR}	20	53	Ω	
MR head current setting resistor	R_{RC}	3k	7.5k	Ω	
Voltage between MR headpins	V_{MR}	0	0.5	V	$V_{MR}=I_R \times R_{MR}$
Operating temperature range	T_{op}	0	+75	°C	

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■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Unless otherwise specified, Vcc=5.0V ± 10%, Ta=+25°C, MR head resistance RMR=36Ω, thin film head Lh=240 nH, Rh=15Ω, C1=0.1 μF, C2=0.1 μF, C3=0.033 μF, C4=0.033 μF)

Parameter	Symbol	Condition	Mode	Values			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	ICCI	RRC=4.3 k	I	—	5.5	7.5	mA	
	ICCR	RRC=4.3 k	R	—	34	55	mA	
	ICCW1	$\overline{RS}$=H, RWC=32	W1	—	58	80	mA	
	ICCW2	$\overline{RS}$=L, RWC=32 RRC=4.3 k	W2	—	67	90	mA	
Power consumption	PDI	RRC=4.3 k	I	—	27.5	37.5	mW	
	PDR	RRC=4.3 k	R	—	220	325	mW	
	PDW1	RWC=32	W1	—	260	420	mW	
	PDW2	RWC=32, RRC=4.3k	W2	—	355	470	mW	
Operating voltages for supply voltage monitoring	VTHL	Vcc falling	R/W	3.45	3.90	4.30	V	
	VTHH	Vcc rising	R/W	3.45	4.10	4.46	V	
Hysteresis width	ΔVTH	VTHH − VTHL	R/W	—	200	—	mV	
WDX, WDY input voltage range	VWDX, YH	High level	—	Vcc−1.02	—	Vcc−0.5	V	
	VWDX, YL	Low level	—	Vcc−1.9	—	VWDX, YH−0.25	V	
WDX, WDY input voltage difference	ΔVWDX, Y	VWDX, YH − VWDX, YL	—	250	—	—	mV	
HS0 to 2, $\overline{CS}$, R/$\overline{W}$, $\overline{RS}$ input voltage range	V IH	High level	—	2.0	—	Vcc	V	
	V IL	Low level	—	−0.3	—	0.8	V	
WDX, WDY input current	IWDX	VWDX, Y=Vcc/−0.3V	I/R	−50	0	50	μA	
	IWDY	VWDX, Y=Vcc	W	—	2	50	μA	
HS input current	I HS	VHS0 to 2=Vcc	—	−50	0	50	μA	
		VHS0 to 2=−0.3V	—	−250	−120	—	μA	
$\overline{CS}$, R/$\overline{W}$, $\overline{RS}$ input current	ICS IR/W IRS	VCS, R/W, $\overline{RS}$=Vcc	—	−50	0	50	μA	
		VCS, R/W, $\overline{RS}$=−0.3V	—	−130	−60	—	μA	
Read head input current	IHR	—	I/W	−50	0	50	μA	
Read head current for non-selected heads	IHRF	—	R	−50	0	50	μA	
MR head current constant	KR	RRC=4.3 k	R	34.3	36.5	38.7	V	KR = IR × RRC
RC pin voltage	VRC	—	I/R/W	0.88	1.00	1.12	V	

(Continued)

(Continued)

Parameter	Symbol	Condition	Mode	Values			Unit	Remarks
				Min.	**Typ.**	**Max.**		
RDX, RDY output current	IRDX, Y	—	R/W	2.0	4.2	6.0	mA	
RDX, RDY output offset	ΔVOFF	ΔVOFF=V RDX – V RDY	R/W	–300	0	300	mV	
Selected read head voltage	VRSH	RRC=4.3 k	R/W2	—	Vcc–1.5	—	V	High potential side
Non-selected read head voltage	VRUS	RRC=4.3 k	I/R/W	—	Vcc–3.0	—	V	
VHR pin voltage	VVHR	RRC=4.3 k	I/R/W	—	Vcc–1.5	—	V	
Read head - VHR voltage difference	ΔVHR	ΔVHR=| V VHR – V RSH |	R/W2	—	0	180	mV	
C3X, C3Y read current	IC3X, Y	VC3X, Y=3V	W	—	0	3	µA	
Write head input current	IHW	—	I/R	–50	0	50	µA	
Write head current for non-selected heads	IHWF	—	W	–50	0	50	µA	
Write current constant	KW	RWC=32	W	0.93	0.98	1.05	V	KW = Ih × RWC
WC pin voltage	VWC1	—	I/R	—	0	100	mV	
	VWC2	—	W	0.93	1.05	1.17	V	
Head clip voltage	VCL1, 2	RWC=32	W	—	2.0	—	V	
Head clip voltage difference	ΔVCL	ΔVHR=| VCL1 – VCL2 |	W	—	0	250	mV	
WUS output current	IWUS	RWUS=1 k	I/R	—	0	50	µA	

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2. AC Characteristics

(Unless otherwise specified, V_{CC}=5.0V±10%, Ta=+25℃, MR head resistance RMR=36Ω, thin film head Lh=240 nH, Rh=15Ω, C1=0.1 μF, C2=0.1 μF, C3=0.033 μF, C4=0.033 μF)

Parameter	Symbol	Condition	Mode	Values			Unit	Remarks
				Min.	Typ.	Max.		
Differential voltage gain	G_D	Vin=1mVpp, fin=5 MHz	R	100	150	220	V/V	RL=100Ω
Frequency bandwidth	B_W	Vin=1mVpp, G_D=− 3 dB	R	55	75	—	MHz	RL=100Ω
Input capacitance	C_I	—	R	—	18	—	pF	
Input conversion noise voltage	Vn	BW=1 to 30MHz, pin short	R	—	0.51	0.69	nV/$\sqrt{\mathrm{Hz}}$	
Input dynamic range	DR	fin=5 MHz, 3fin=− 30 dB	R	5	—	—	mVpp	
Common mode rejection ratio	CMRR	Vin=100 mVpp, fin=5 MHz	R	40	—	—	dB	
Power supply rejection ratio	PSRR	Vin=100 mVpp, fin=5 MHz	R	40	—	—	dB	
Channel separation	CSP	Vin=100 mVpp, fin=5 MHz	R	40	—	—	dB	
$\overline{CS}$ delay	tdIR	RRC=4.3 k	IR	—	—	20	μs	
	tdRI	RRC=4.3 k	RI	—	—	1	μs	
	tdIW	RWC=24	IW	—	250	500	μs	
	tdWI	RWC=24	WI	—	100	500	μs	
R/$\overline{W}$ delay	tdWRR	RRC=4.3 k, RMR=36, RS=H	W1R	—	—	3.0	μs	tWG=1ms For a 1ms write time
		RRC=4.3 k, RMR=36, RS=L	W2R	—	—	3.0	μs	
		RRC=3.0 k, RMR=53, RS=L	W2R	—	—	3.5	μs	
	tdRWR	RRC=4.3 k	RW	—	—	1	μs	
	tdRWW	RWC=24	RW	—	250	500	ns	
	tdWRW	RWC=24	RW	—	100	500	ns	
RS delay	tdW12	RRC=4.3 k	W1W2	—	—	1	μs	
	tdW21	RRC=4.3 k	W2W1	—	—	3	μs	
HS delay	tdHSR	RMR=30 ↔ 41 (at head switching)	R	—	—	40	μs	
	tdHSW	RWC=24	W	—	—	500	ns	
WUS delay	tdSF	fWDX, Y=0 → 2 MHz	W	—	—	1	μs	
	tdUS	fWDX, Y=20 → 0 MHz	W	0.6	1.2	3.6	μs	
Write current transition time	tr1/tf1	RWC=24, Lh=240 nH, Rh=15	W	—	9	—	ns	
Transition time difference	Δtpd	| tr1 − tf1 |	W	—	—	1	ns	

(Continued)

(Continued)

Parameter	Symbol	Condition	Mode	Values			Unit	Remarks
				Min.	**Typ.**	**Max.**		
Write current delay	tpd1, 2	RWC=24, Lh=240 nH, Rh=15	W	—	4.5	—	ns	
Delay time difference	Δtrf	| tpd1 – tpd2 |	W	—	—	1	ns	
Write data input frequency	fWDX, Y	RWC=24, Lh=240nH, Rh=15	W	1.6	—	31.5	MHz	
WUS output voltage	VUSL	fWDX, Y=2MHz, IWUS=5mA	W	—	0.1	0.5	V	
WUS output current	IUSH	fWDX, Y=0MHz, Rh=15	W	—	0	50	μs	
		fWDX, Y=9MHz, Write head open	W	—	0	50	μs	IW=40mA

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■ FUNCTIONS

1. Mode Selection

Operation Mode	MR Bias Current	CS Pin Voltage	R/$\overline{\text{W}}$ Pin Voltage	$\overline{\text{RS}}$ Pin Voltage
Idle (I)	OFF	H	—	—
Read (R)	ON	L	H	—
Write 1 (W1)	OFF	L	L	H
Write 2 (W2)	ON	L	L	L

2. Head Selection

Head	HS0	HS1	HS2
0	L	L	L
1	H	L	L
2	L	H	L
3	H	H	L
4	L	L	H
5	H	L	H

3. WUS (Write Unsafe) Output Truth Table

Operation mode	Conditions	WUS
Idle (I)	—	H
Read (R)	—	H
Write (W)	Normal	L
	When one or more of the following faults is present: • Write data frequency too low. • Write head pin is open (fWD< 9MHz). • No write current, or current is too low.	H

■ OPERATION

1. Read Mode

In read mode, the MB4138 operates as a low noise differential amplifier. A bias current (sense current) flows through the MR head from the RiX pin to the RiY pin.

The MR head bias current (I_R) is determined by the MR head current constant (KR) and the resistance (RRC) connected between the RC pin and GND pin. The current is calculated as follows.

$$I_R = KR/RRC$$

The RiX and RiY pins are connected directly to the bias current circuit and to the bases of the two opposite transistors of the differential amplifier circuit (read amp). Therefore, differential amplification of the read signal from the MR head is performed directly. The emitters of the two opposite transistors of the differential amplifier circuit require capacitive coupling to cut the DC component generated by the MR head resistance and bias current. (Connect 0.033 μF capacitors across C3X - C3Y and C4X - C4Y).

RDX and RDY are open-collector output pins for the read buffer circuit. RiX and RDX, and RiY and RDY have the same phase.

The output voltages (DC) of RDX and RDY are almost the same for write and read modes. This reduces the transient time when switching from write to read mode.

Connect 0.1 μF capacitors across C1 - GND and C2 - Vcc to stabilize the current source circuit for the MR head bias current.

In all modes, the VHR pin outputs the same voltage as the RiX pin of the channel selected for read mode. The potential difference between the MR head and disk can be eliminated by biasing the disk with this voltage.

2. Write Mode

In write mode, the MB4138 switches the current through the thin film head (Ih) at high speed. The write current (IW) is determined by the write current constant (KW) and the resistance connected between the WC pin and ground (RWC). The currents are calculated as follows.

$$Iw = VWC/RWC$$

$$Ih = \frac{Iw \times 0.99}{1 + Rh/Rd} = KW/RWC$$

<div align="right">

Rh: Thin film head resistance
Rd: IC internal damping resistance

</div>

The write fault detection circuit detects abnormalities in the thin film head and its connection pins (WiX and WiY). The circuit generates an alarm on detecting a fault.

Normally, no bias current flows in the MR head during write mode. However, to reduce the transient time when switching from write to read mode, a bias current can be flowed by setting the RS pin at the "L" level.

3. Idle Mode

Neither the read nor write circuits operate in idle mode.

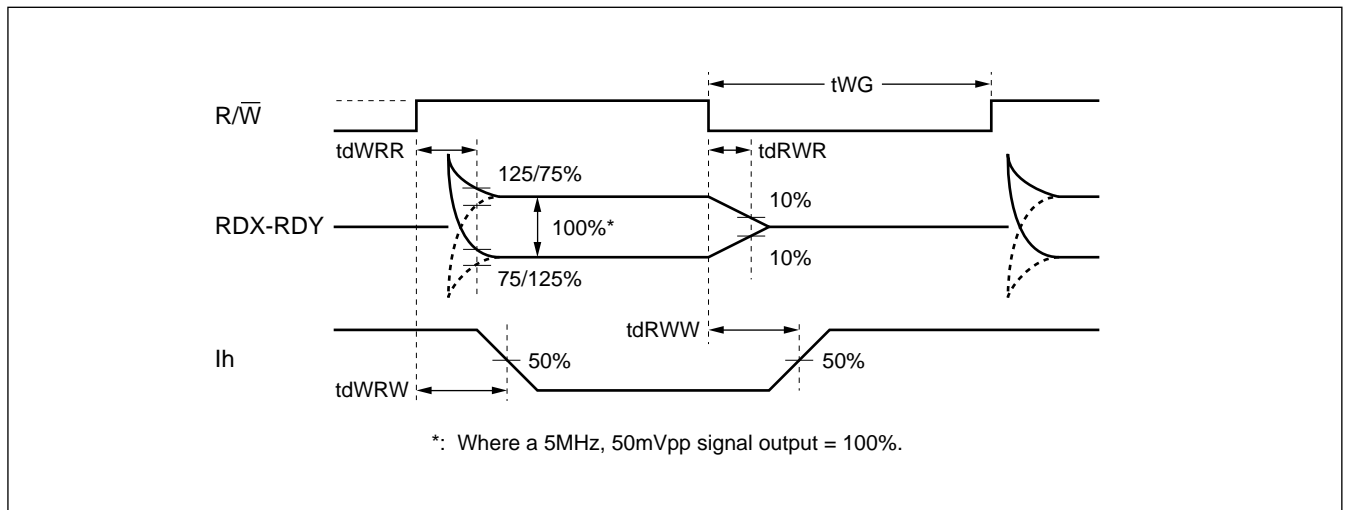However, the VHR pin continues to operate and output a voltage in idle mode.
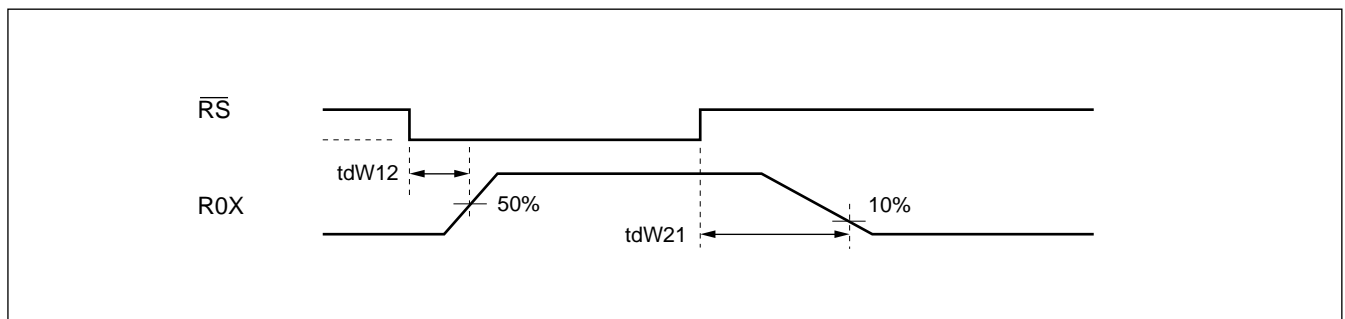
MB4138

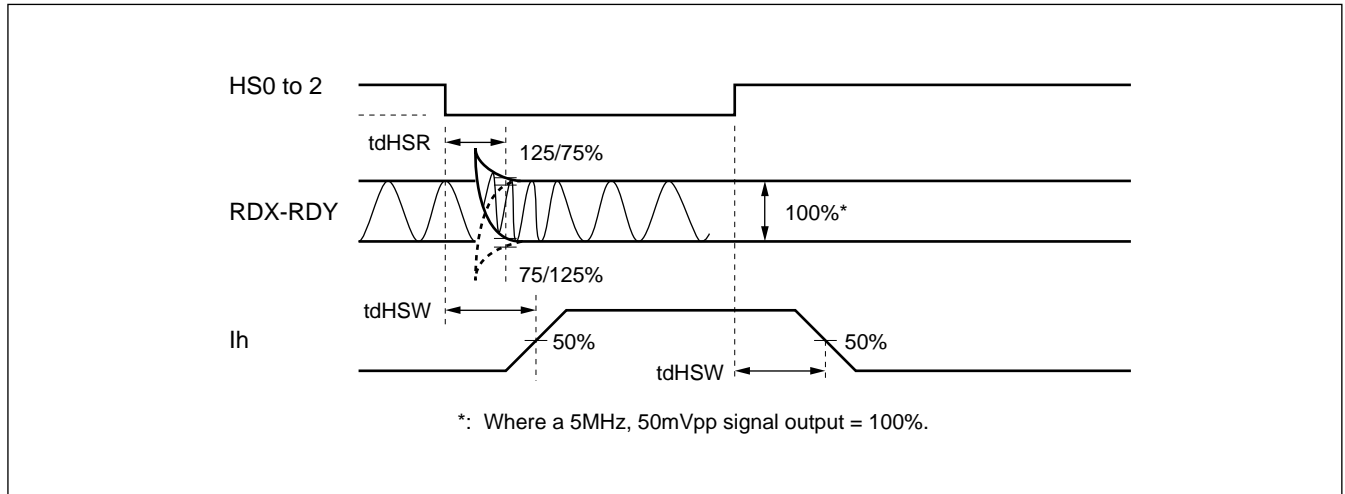## ■ TIMING CHART

1. $\overline{\text{CS}}$ Delay

*: Where a 5MHz, 50mVpp signal output = 100%.

2. R/$\overline{\text{W}}$ Delay

*: Where a 5MHz, 50mVpp signal output = 100%.

3. $\overline{\text{RS}}$ Delay

4. HS Delay

HS0 to 2

tdHSR
125/75%

RDX-RDY
100%*

75/125%

tdHSW

Ih
50%
50%
tdHSW

*: Where a 5MHz, 50mVpp signal output = 100%.

5. WUS Delay

WDX
(=$\overline{\text{WDY}}$)

tdUS
tdSU

WUS
50%
50%
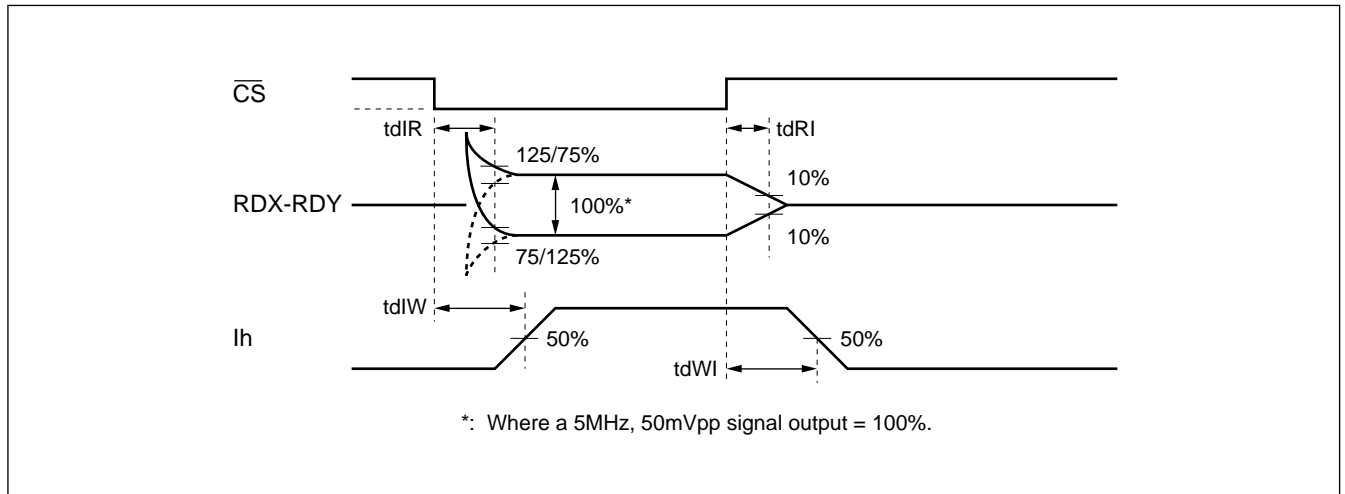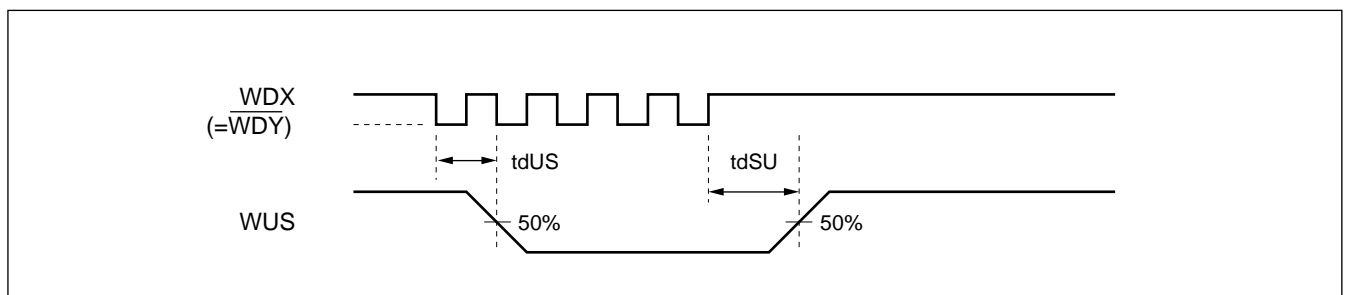
6. Write Current Transition Time, Write Current Delay

WDX
(=$\overline{\text{WDY}}$)

tf1

tpd1
90%
50%
10%
50%
10%

tr1
tpd2
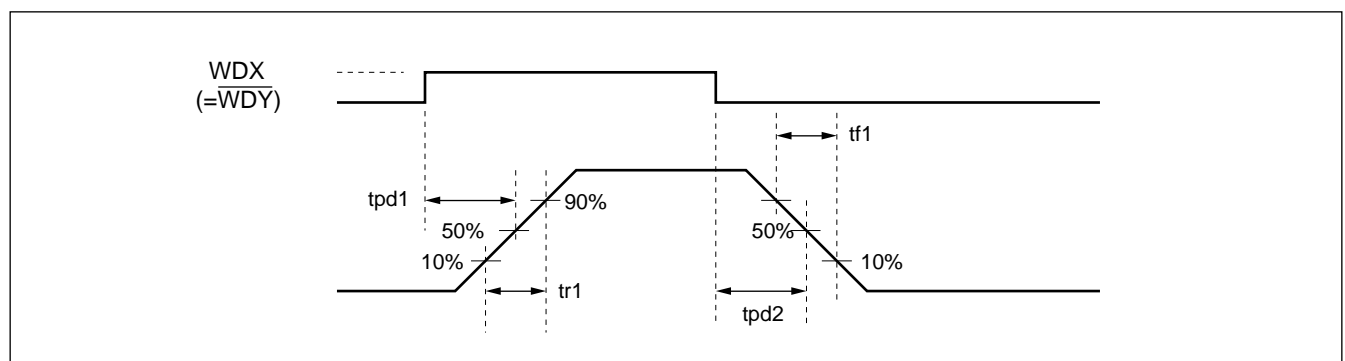
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■ APPLICATION CIRCUIT EXAMPLE
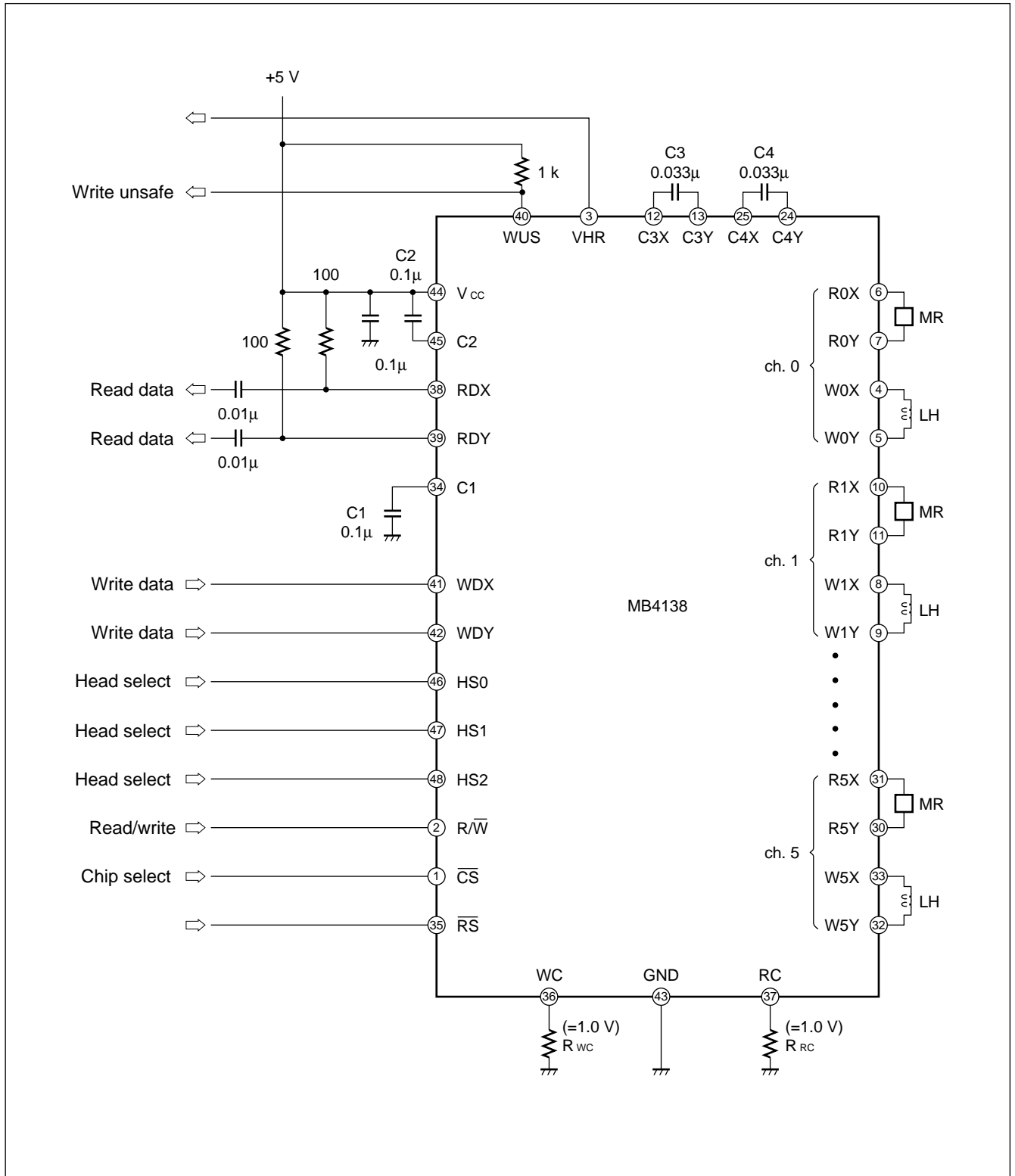
■ ORDERING INFORMATION

Part Number	Package	Remarks
MB4138PFQ	48-pin, Plastic QFP (FPT-48P-M13)	

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■ PACKAGE DIMENSION

48-pin, Plastic QFP
(FPT-48P-M13)

13.10±0.40 SQ
(.516±.016)

10.00±0.20 SQ
(.394±.008)

36   25

37   24

INDEX

"A"

48   13

LEAD No. ① 1   12

0.80(.0315)TYP

0.30±0.10
(.012±.004) ⊕ 0.16(.006) Ⓜ

"B"

☐ 0.10(.004)

2.35(.093)MAX

0(0)MIN
(STAND OFF)

8.80
(.346)
REF

11.50±0.30
(.453±.012)

0.15±0.05
(.006±.002)

Details of "A" part

0.15(.006)

0.20(.008)

0.18(.007)MAX

0.53(.021)MAX

Details of "B" part

0~10°

0.80±0.30
(.031±.012)
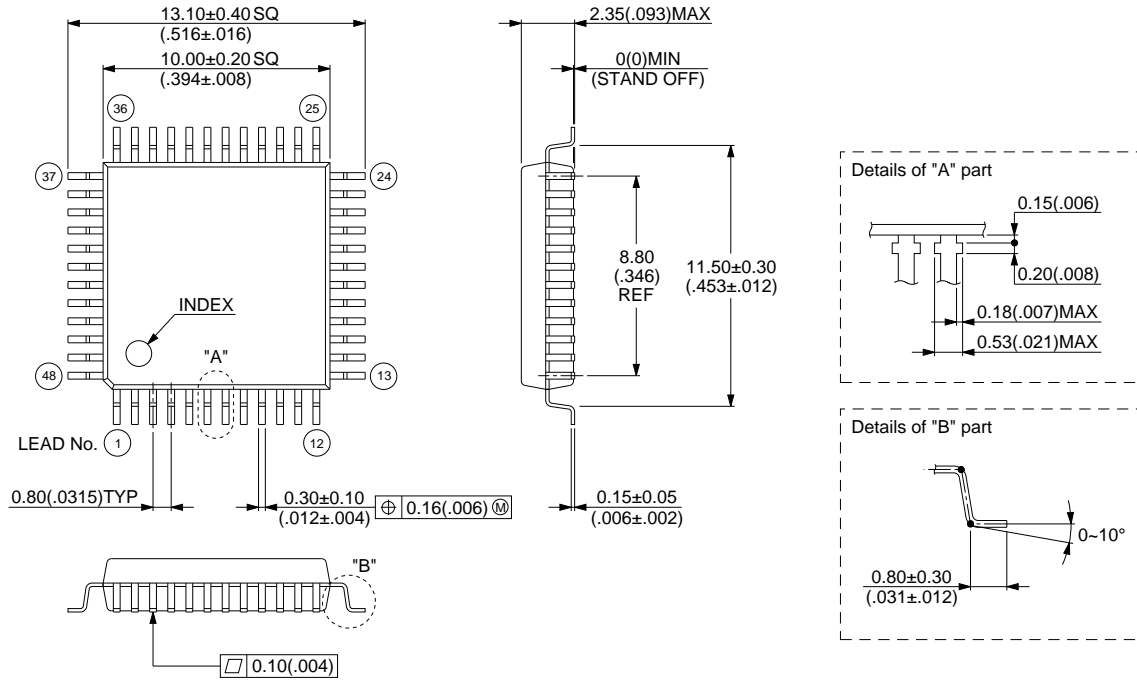
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Dimensions in mm (inch).

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FUJITSU LIMITED

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