

ASSP

AD/DA CONVERTER

MB40166/MB40176

1-CHANNEL 6-BIT AD/DA CONVERTER WITH CLAMP CIRCUIT

The Fujitsu MB40166 and MB40176 are low power 6-bit AD/DA converter which is fabricated with Fujitsu Advanced Bipolar Technology. MB40166 and MB40176 have the same basic circuits and functions, with the only difference being that MB40166 has an independent analog input terminal for the A/D section and a clamp voltage output terminal, while MB40176 has an analog input in the A/D section internally connected with the clamp circuit.

Since both models contain a single-chip clamp circuit and a reference voltage circuit, they are ideal for video signal processing.

- Resolution :6 bits
- Linearity Error :±0.8% max.
- Maximum Conversion Rate :20 MSPS min.
- Analog Input Voltage Range :VREF to VCCA (MB40166)
0 to 1.0 V (MB40176)
- Analog Output Voltage Range :VCC to VCC -1 V
- Digital I/O Level :TTL Level
- Power Supply Voltage :+5 V
- Power Dissipation:300 mW typ.
- Package

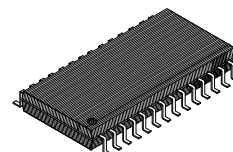
28pin Plastic FLAT Package (Suffix : -PF)
28pin Plastic DIP Package (Suffix : -P)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

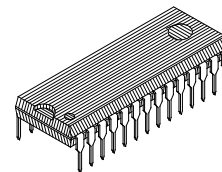
Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCCA, VCCD	-0.5 to +7.0	V
Digital Input Voltage	VIND	-0.5 to +7.0	V
Analog Input Voltage	VINA	-0.5 to VCCA +0.5	V
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

28 pin, Plastic SOP
(FPT-28P-M01)



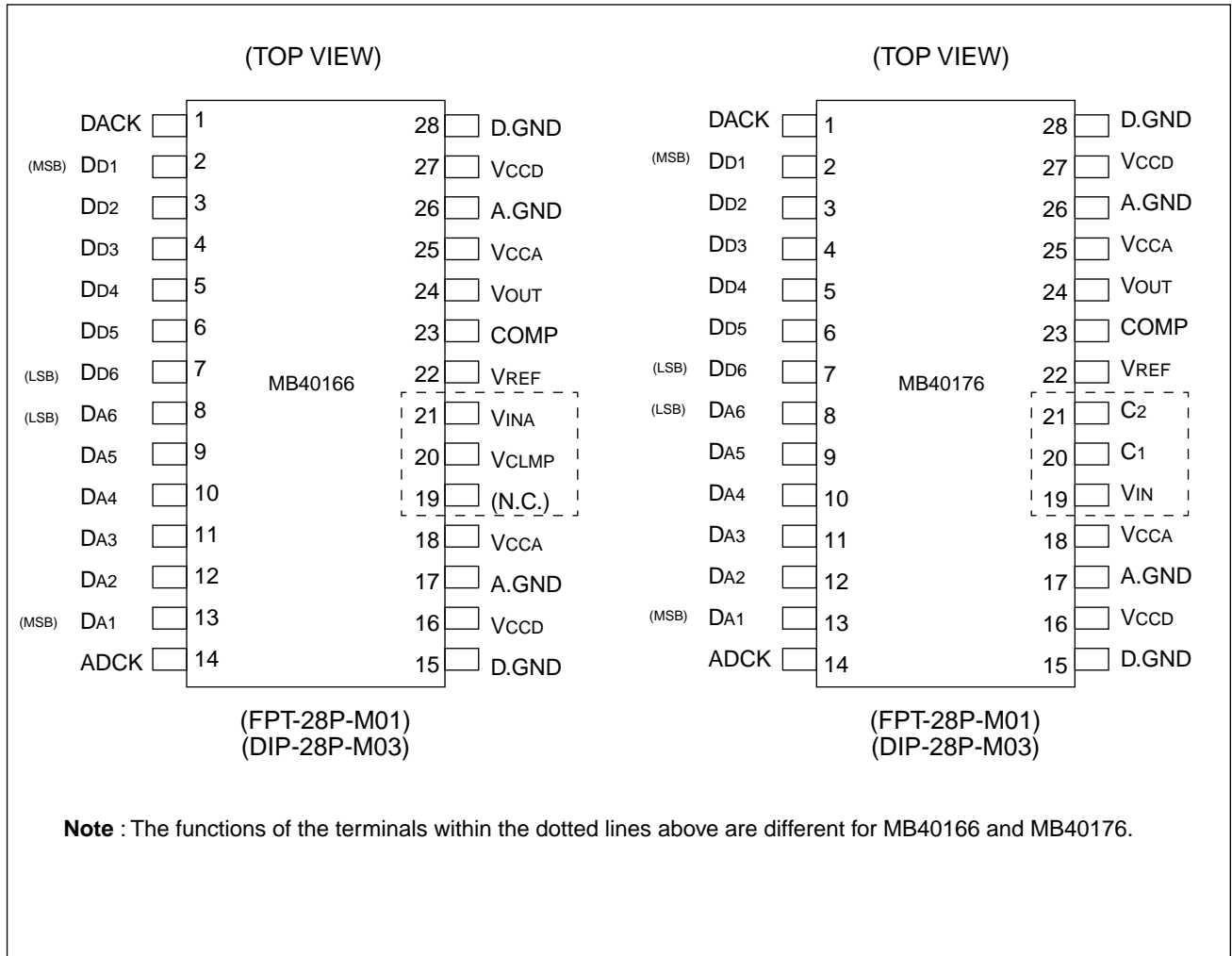
28 pin, Plastic SH-DIP
(DIP-28P-M03)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

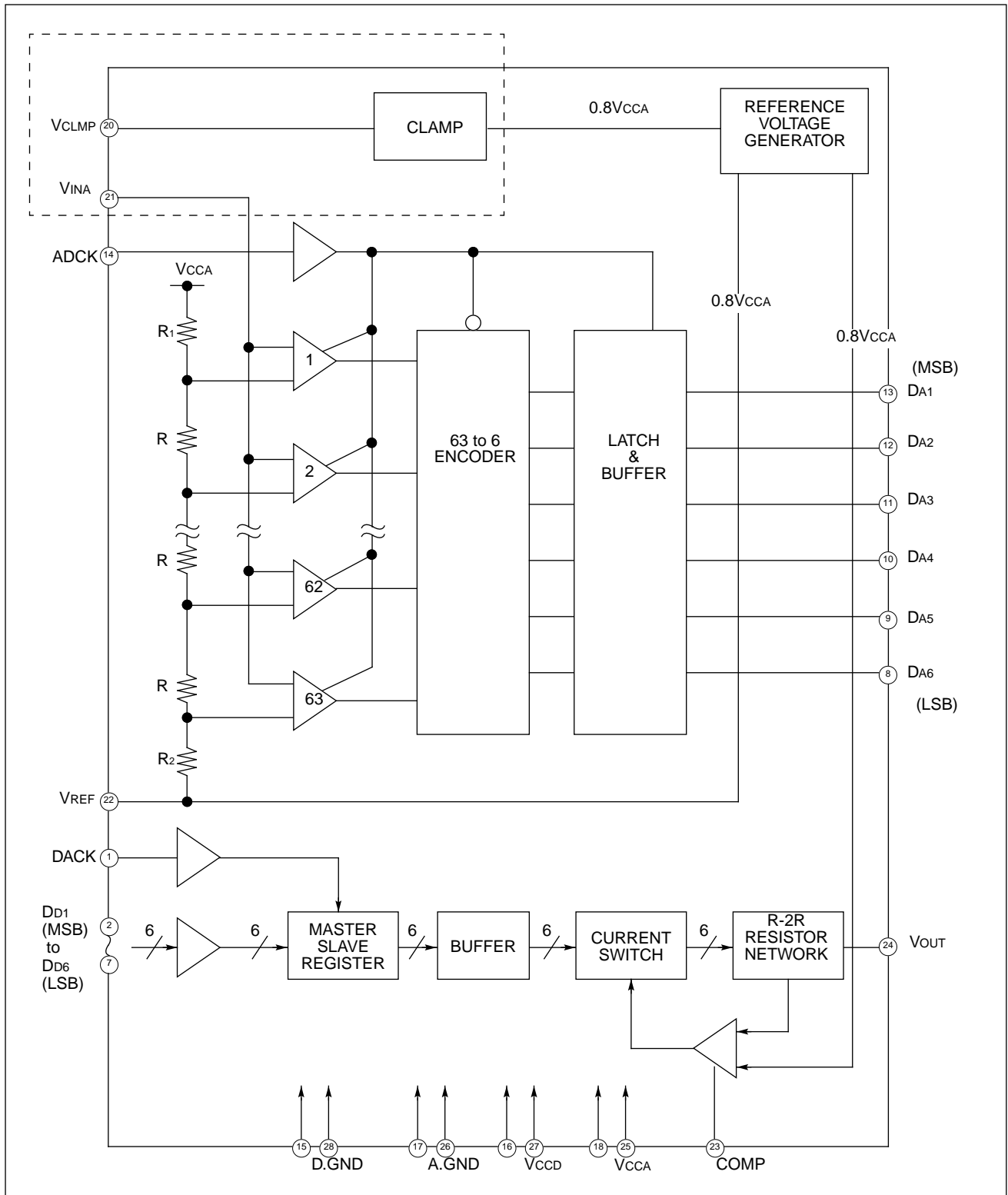
MB40166/40176

■ PIN ASSIGNMENT



■ BLOCK DIAGRAM

• MB40166

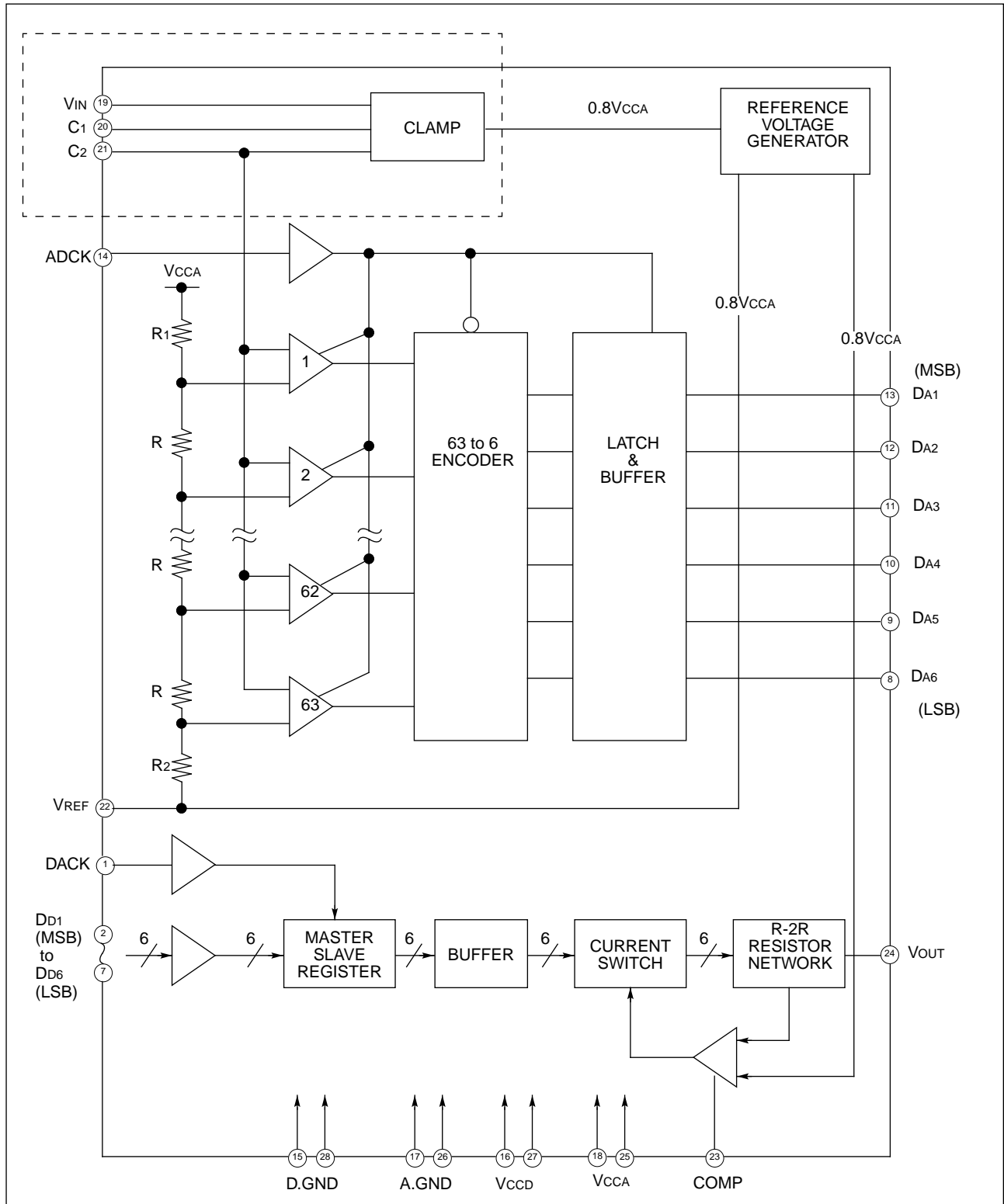


Note : The circuits within the dotted lines above are different for MB40166 and MB40176.

MB40166/40176

■ BLOCK DIAGRAM (Continued)

• MB40176



Note : The circuits within the dotted lines above are different for MB40166 and MB40176.

■ PIN DESCRIPTIONS

Section	Pin No.		Symbol	I/O	Function
	40166	40176			
A/D	21	–	VINA	I	Analog signal input.
	–	19	VIN	I	
	22		VREF	O	Reference voltage output. Reference voltage divided by the resistors, with the output voltage set to 0.8 x VCCA (V).
	8 to 13		DA1 to DA6	O	Digital signal outputs. (DA1: MSB, DA6: LSB)
	20	–	VCLMP	O	Clamp voltage output.
	–	20	C1	–	Clamp capacitor is connected between these pins.
	–	21	C2	–	
	14		ADCK	I	A/D conversion clock input.
D/A	24		VOUT	O	Analog signal output.
	2 to 7		DD1 to DD6	I	Digital signal input. (DD1: MSB, DD6: LSB)
	23		COMP	–	Phase compensation capacitor is connected. Insert a capacitor of 1 μ F or more between this pin and A.GND.
	1		DACK	I	D/A conversion clock input.
Common	18, 25		VCCA	–	Power supply for analog circuit. (+5 V)
	16, 27		VCCD	–	Power supply for digital circuit. (+5 V)
	17, 26		A.GND	–	Ground for analog circuit. (0 V)
	15, 28		D.GND	–	Ground for digital circuit. (0 V)
Other	19	–	(N.C.)	–	No connection.

MB40166/40176

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power Supply Voltage	VCCA, VCCD	4.75	5.00	5.25	V	
Analog Input Voltage	VINA	VREF	–	VCCA	V	MB40166
	VIN	0	–	1	V	MB40176
Digital High-level Input Voltage	VIHD	2.0	–		V	
Digital Low-level Input Voltage	VILD	–	–	0.8	V	
Clock Frequency	fCLK	–	–	20	MHz	
Clock Pulse Width at High Level	tw ⁺	20	–	–	ns	
Clock Pulse Width at Low Level	tw ⁻	20	–	–	ns	
Set-up Time	ts	12.5	–	–	ns	
Hold Time	th	7.5	–	–	ns	
Phase Compensation Capacitance	CCOMP	1.0	–	–	μF	
Clamp Capacitance	CCLAMP	1.0	–	–	μF	
Reference Voltage Capacitance	CVREF	1.0	–	–	μF	
Operating Temperature	Ta	0	–	70	°C	

■ ELECTRICAL CHARACTERISTICS

ANALOG CIRCUIT DC CHARACTERISTICS

(VCCA=VCCD=5V±5%, Ta=0 to 70°C)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–		–	–	6	Bits	
Linearity Error	LE	DC	–	–	±0.8	%	
Analog High Level Input Current	I _{IHA}	V _{INA} = V _{CCA}	–	8.5	25	μA	MB40166
Analog Low Level Input Current	I _{IILA}	V _{INA} = V _{REF}	–	7.5	23	μA	MB40166
Equivalent resistance for Analog Input	R _{INA}	$\frac{V_{CCA} - V_{REF}}{I_{IHA} - I_{IILA}}$	400	–	–	kΩ	MB40166
Analog Input Current	I _{IN}		-400	–	–	μA	MB40176
Reference Voltage	V _{REF} *		3.9	4.0	4.1	V	
Clamp Voltage	V _{CLMP}		–	V _{REF}	–	V	
Full-Scale Output Voltage	V _{OFS}		–	V _{CCA}	–	V	
Zero-Scale Output Voltage	V _{OZS}		–	V _{REF}	–	V	
Output Resistance	R _O		–	240	–	Ω	
Power Supply Current	I _{CC}		–	60*	90	mA	

Note : *V_{CCA}=V_{CCD}=5.0V

■ ELECTRICAL CHARACTERISTICS (Continued)

DIGITAL CIRCUIT DC CHARACTERISTICS

(VCCA=VCCD=5V±5%, Ta=0°C to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Digital High-level Output Voltage	VOHD	I _{OH} =-400 μA	2.7	–	–	V
Digital Low-level Output Voltage	VOLD	I _{OL} =1.6mA	–	–	0.4	V
Digital High-level Input Voltage	VIHD		2.0	–	–	V
Digital Low-level Input Voltage	VILD		–	–	0.8	V
Digital High-level Input Current	IIHD		–	–	20	μA
Digital Low-level Input Current	IILD		-100	–	–	μA

SWITCHING CHARACTERISTICS

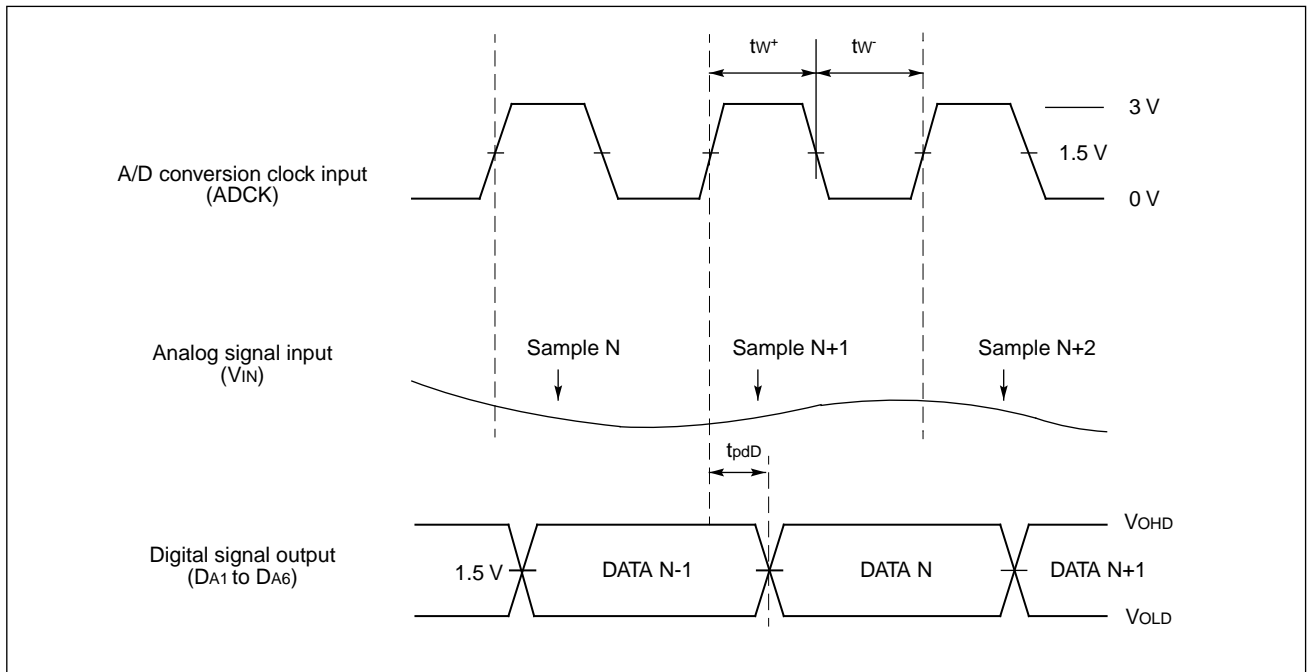
(VCCA=VCCD=5V±5%, Ta=0°C to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	F _S		20	–	–	MSPS
Digital Output Delay Time	t _{PDD}		8	15	30	ns
Analog Output Delay Time	t _{PDA}		–	13	–	ns
Analog Output Rise Time	t _r		–	15	–	ns
Analog Output Fall Time	t _f		–	15	–	ns

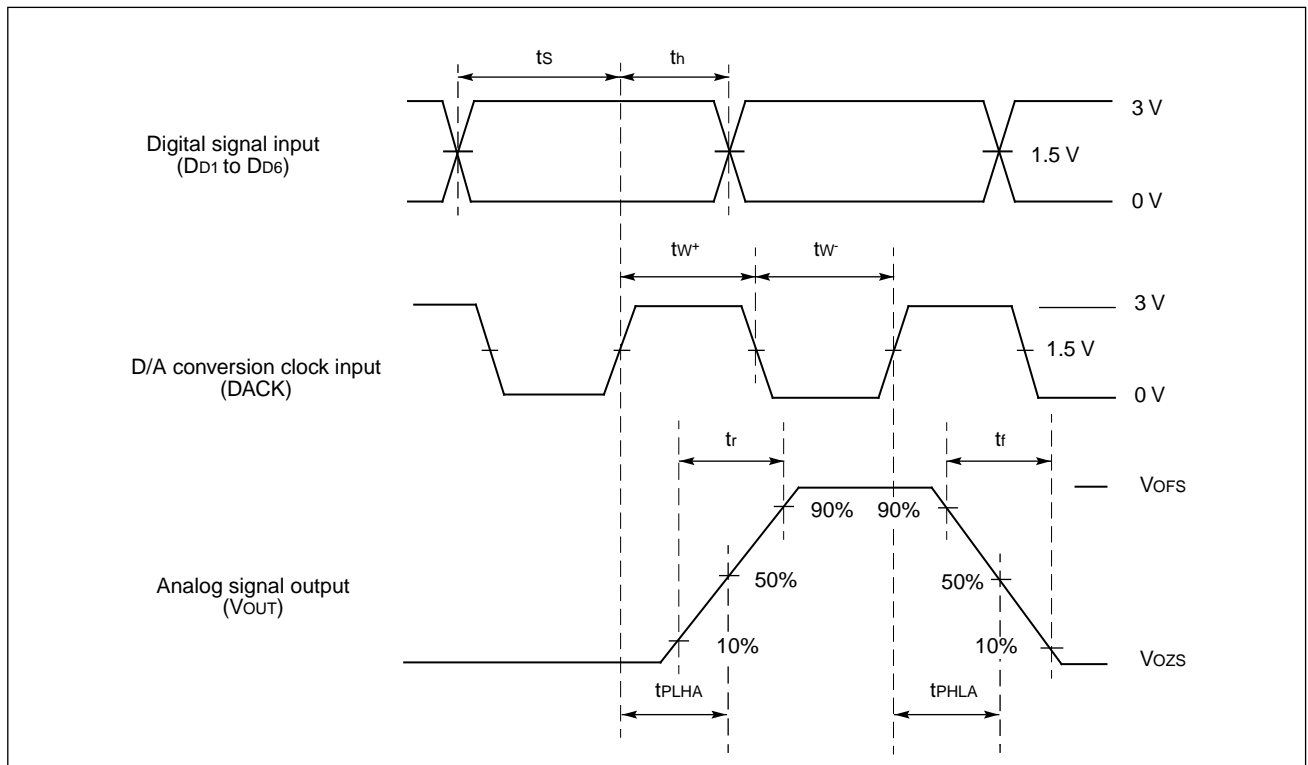
MB40166/40176

■ TIMING CHART

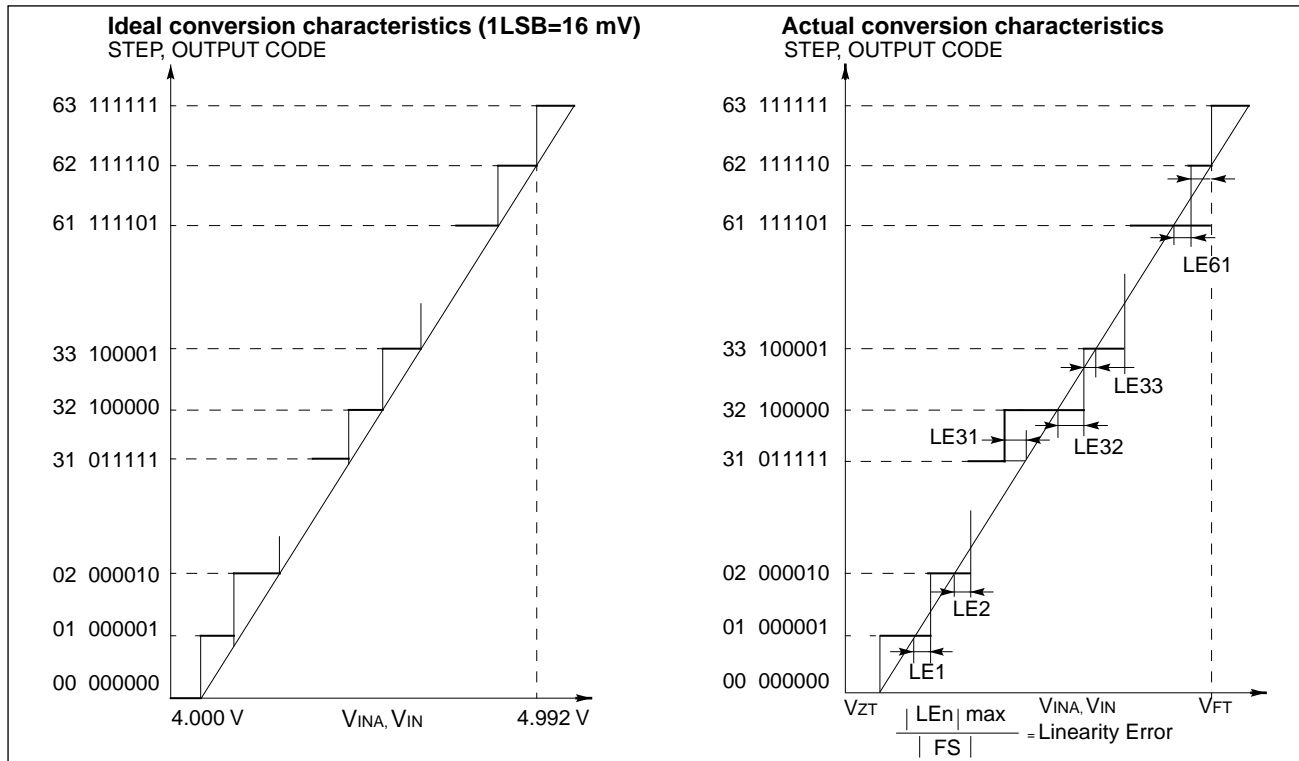
1. Timing Chart for A/D Conversion



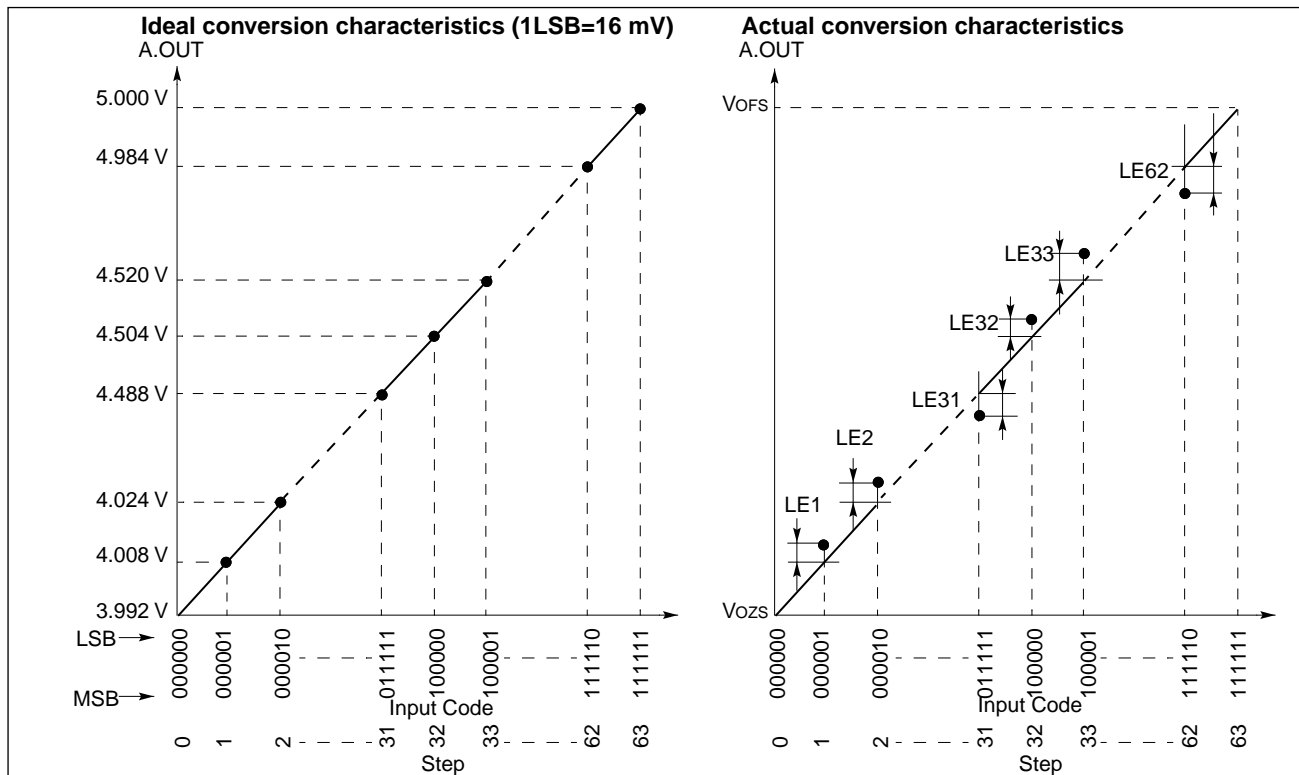
2. Timing Chart for D/A Conversion



■ A/D CONVERSION CHARACTERISTICS



■ D/A CONVERSION CHARACTERISTICS



MB40166/40176

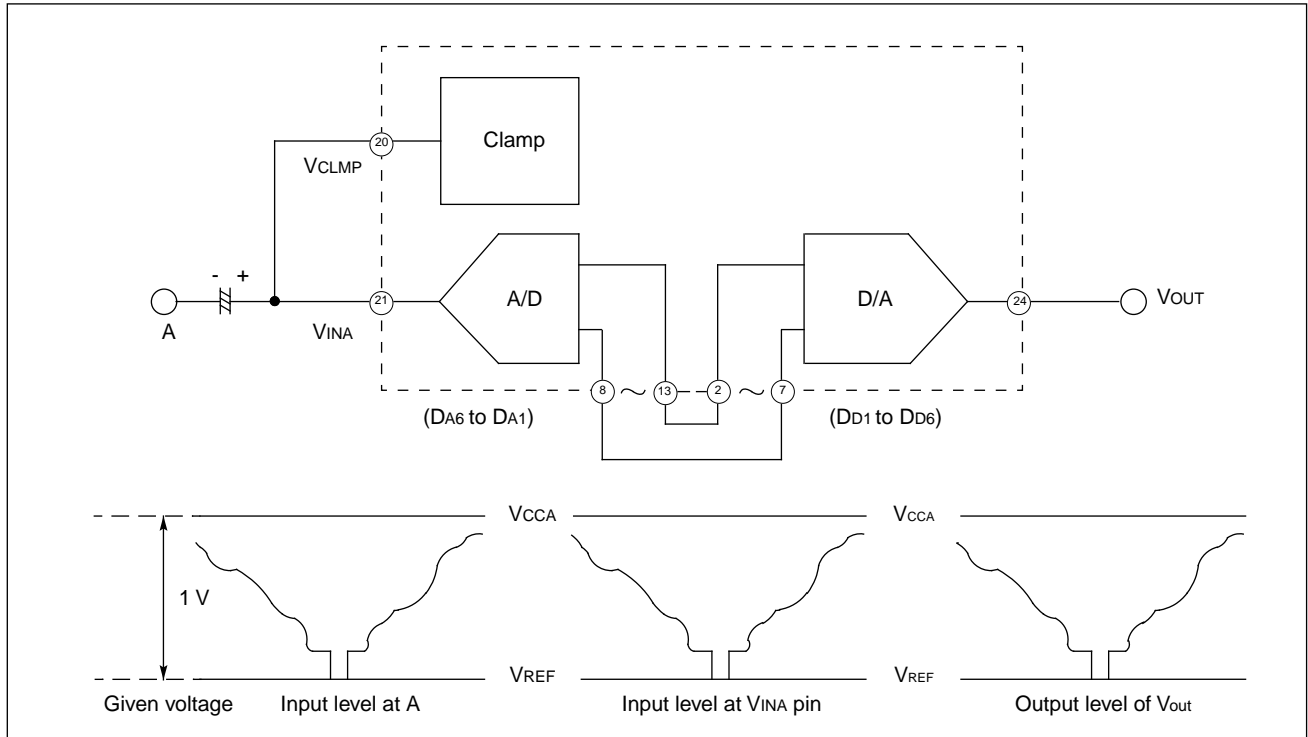
FUNCTIONAL DESCRIPTIONS CLAMP CIRCUIT

The clamp circuit contained in MB40166/MB40176 is a peak detector type, in which the top of the sync of the composite sync signal is clamped.

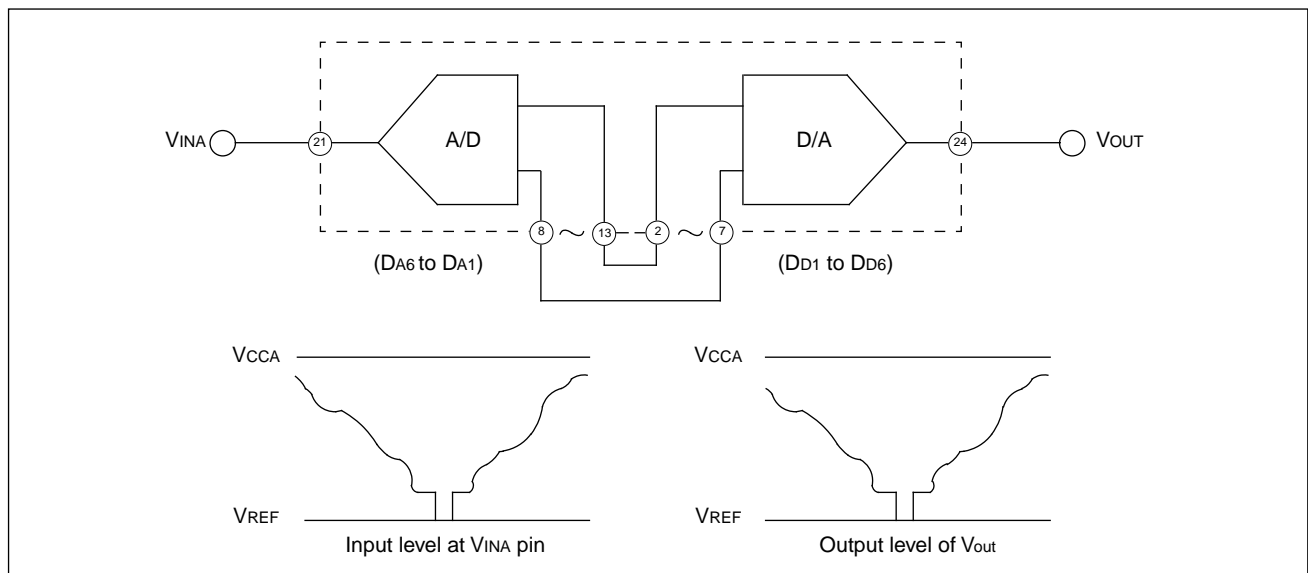
Clamp voltage is common to the reference voltage ($0.8 \times V_{CC}$) of A/D and D/A circuits.

• MB40166

(1) Providing a clamp circuit

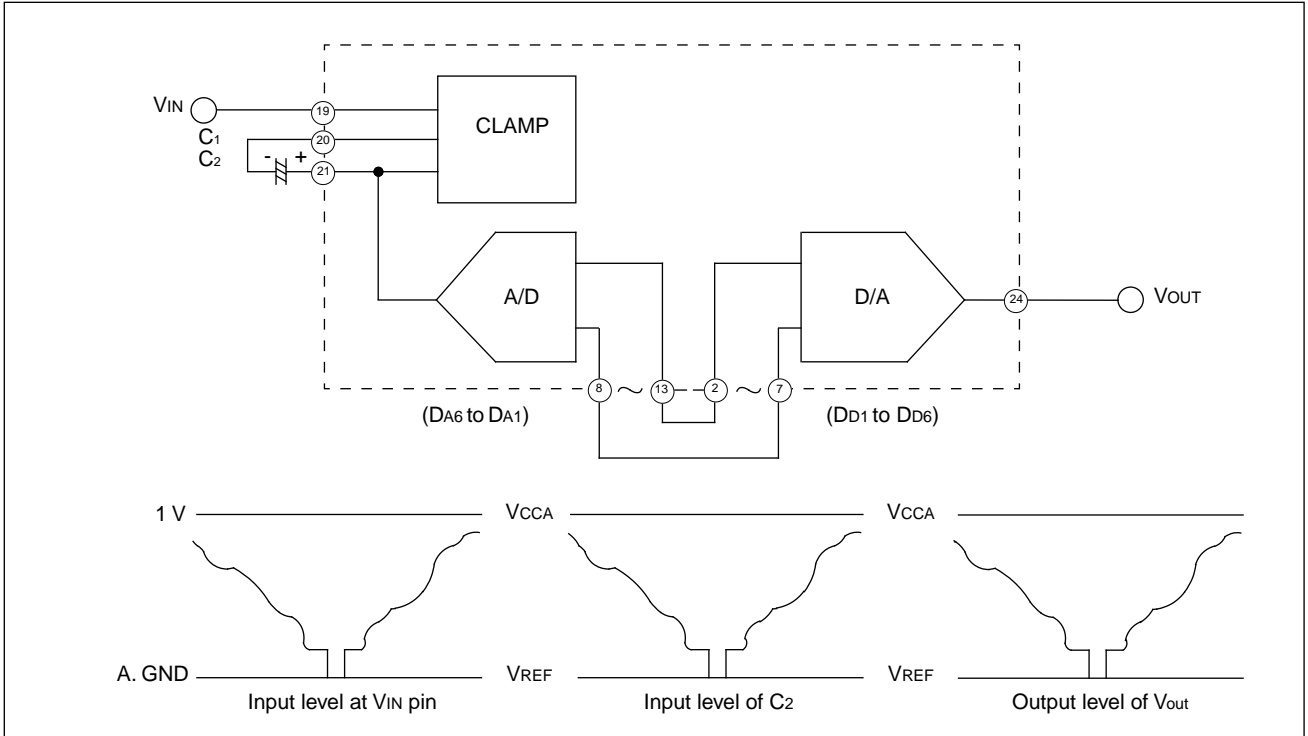


(2) Directly feeding the signal at the VINA pin



MB40166/MB40176

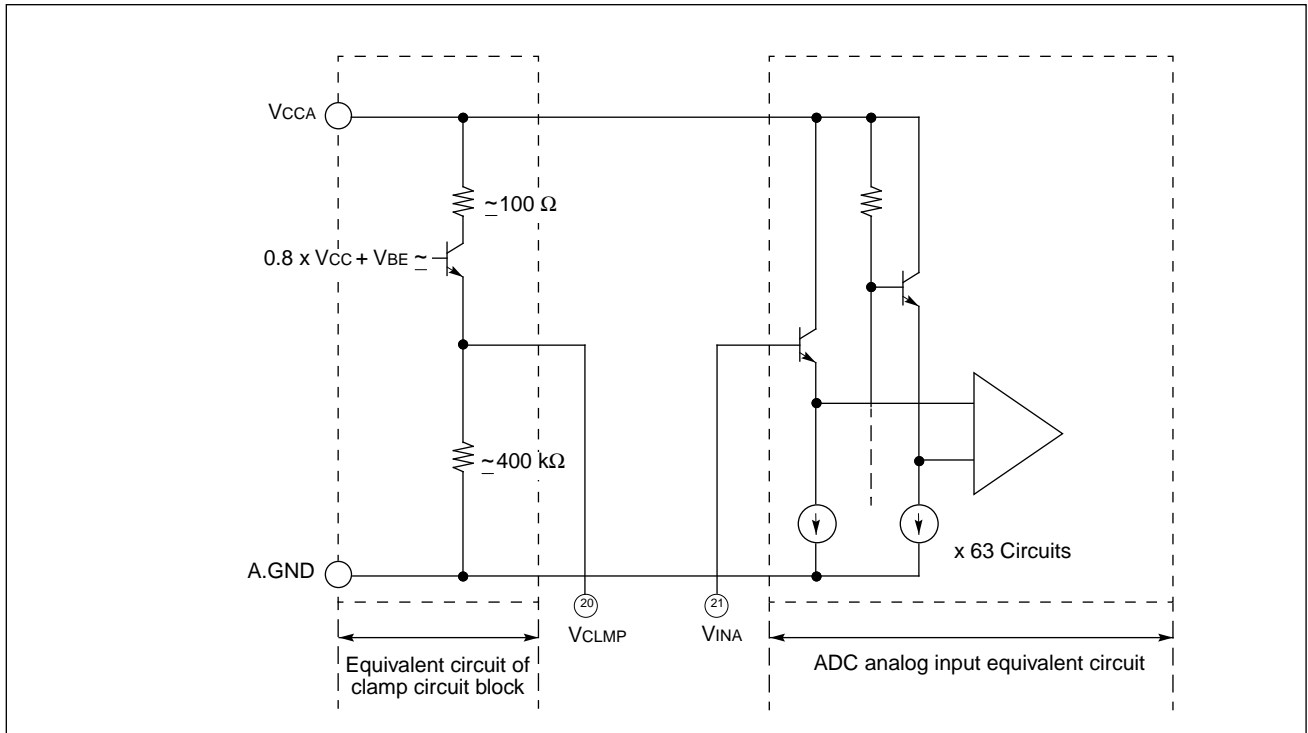
- MB40176



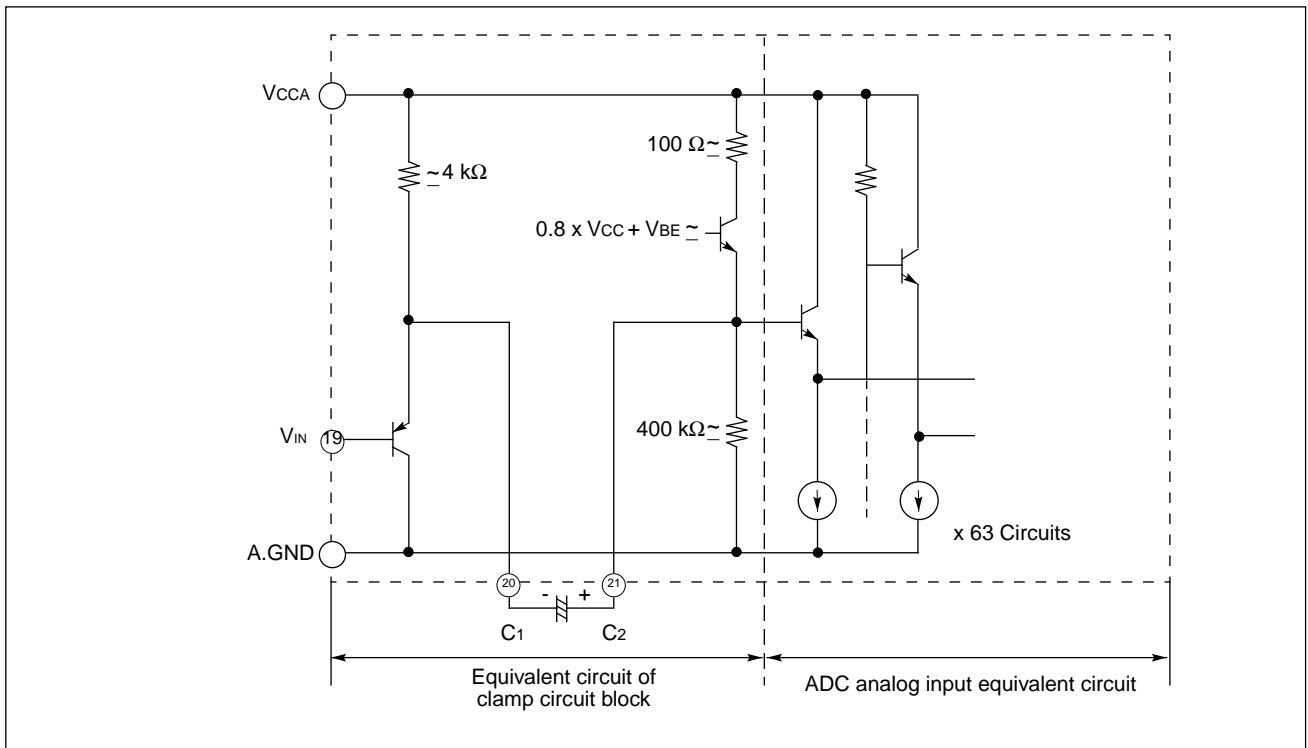
MB40166/40176

■ ANALOG INPUT EQUIVALENT CIRCUIT

• MB40166



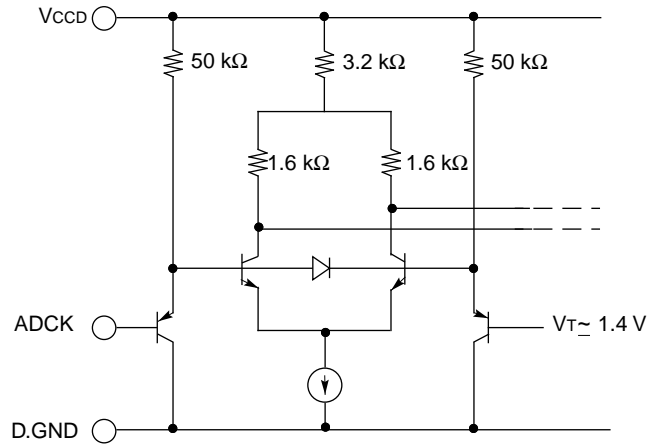
• MB40176



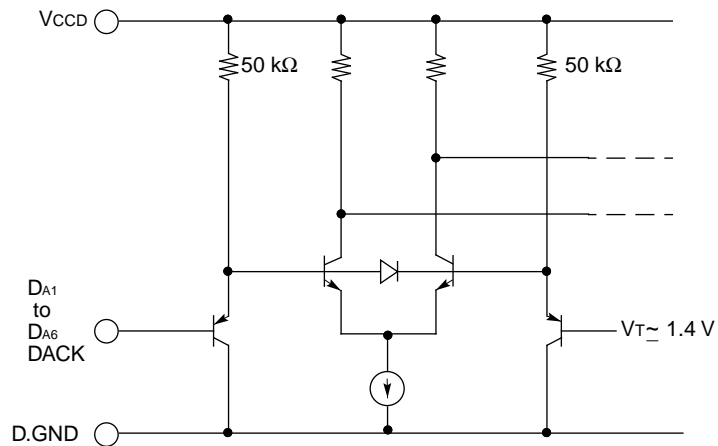
■ DIGITAL INPUT EQUIVALENT CIRCUITS

- MB40166/MB40176

Digital input equivalent circuit of A/D converter block



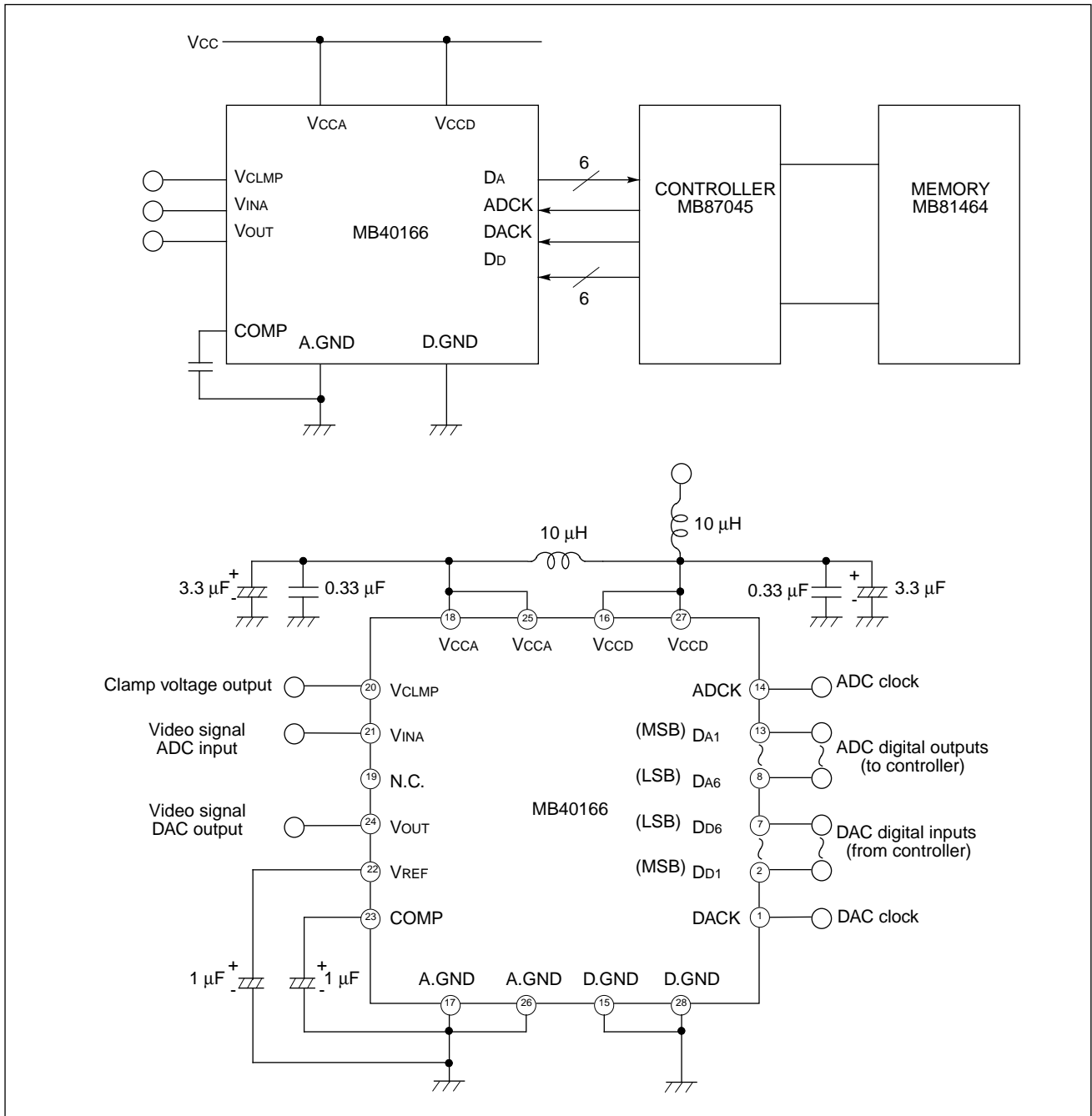
Digital input equivalent circuit of D/A converter block



MB40166/40176

■ TYPICAL CONNECTION EXAMPLE

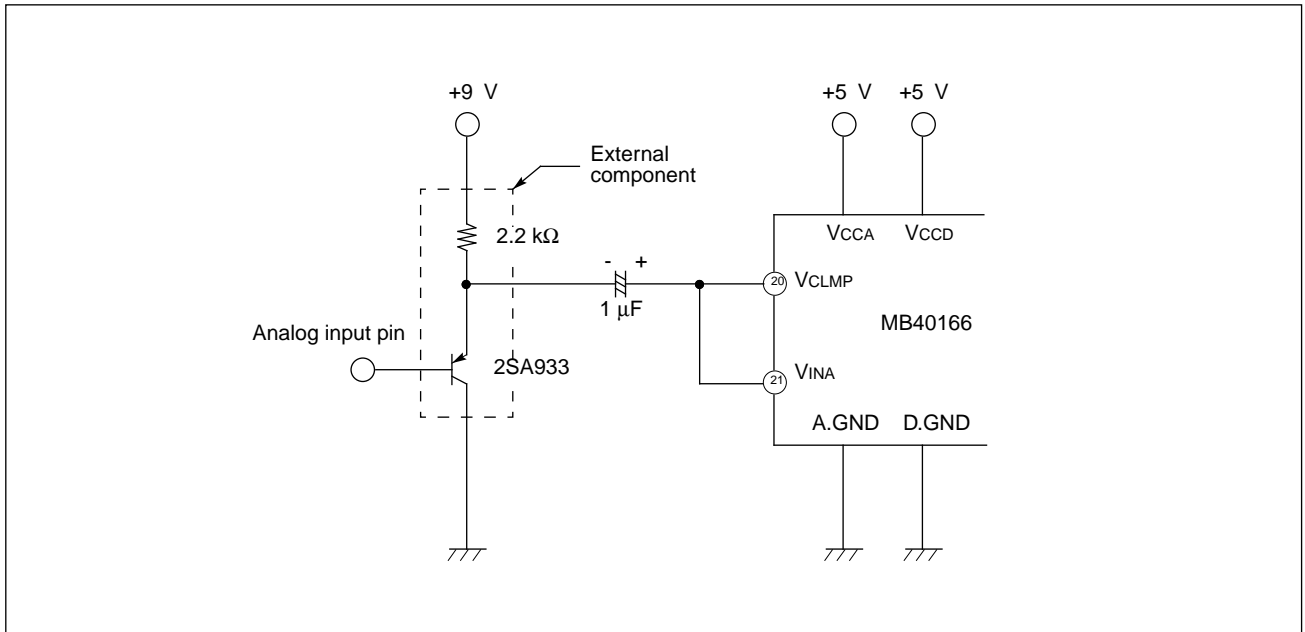
• MB40166



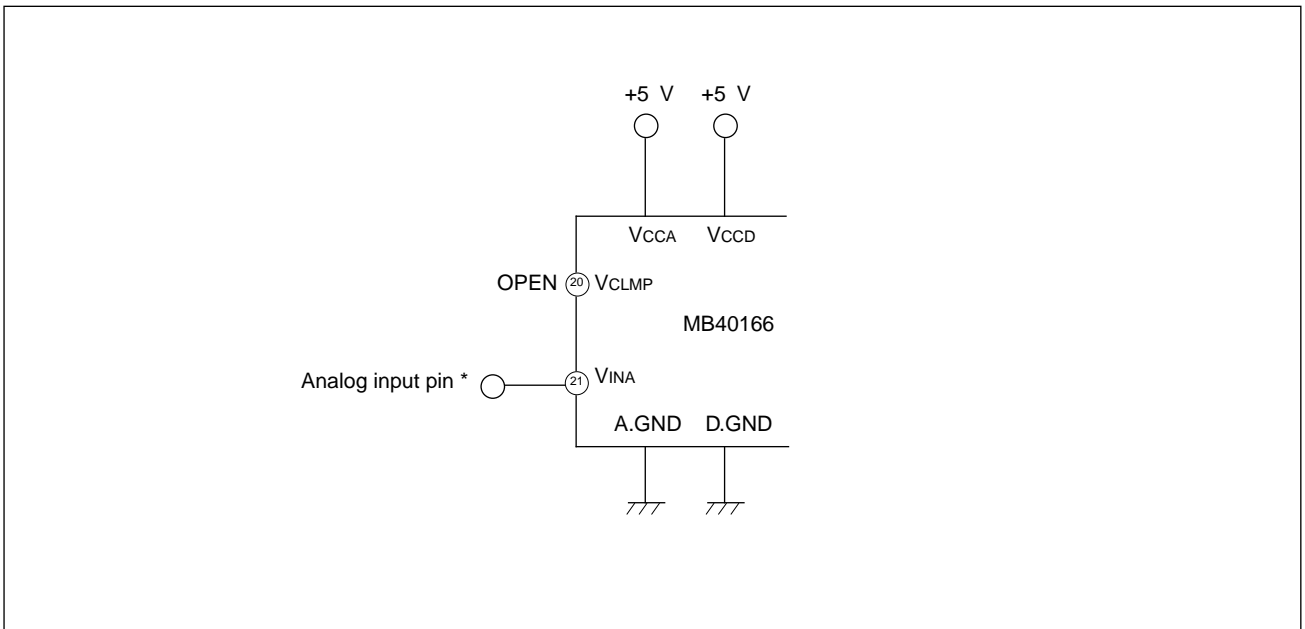
Note : If the clamp circuit is used, connect VINA with VCLMP.
If the clamp circuit is not used, do not connect VINA with VCLMP.

■ TYPICAL CONNECTION EXAMPLE (continued)

(1) Internal clamp circuit is used.



(2) Internal clamp circuit is not used.

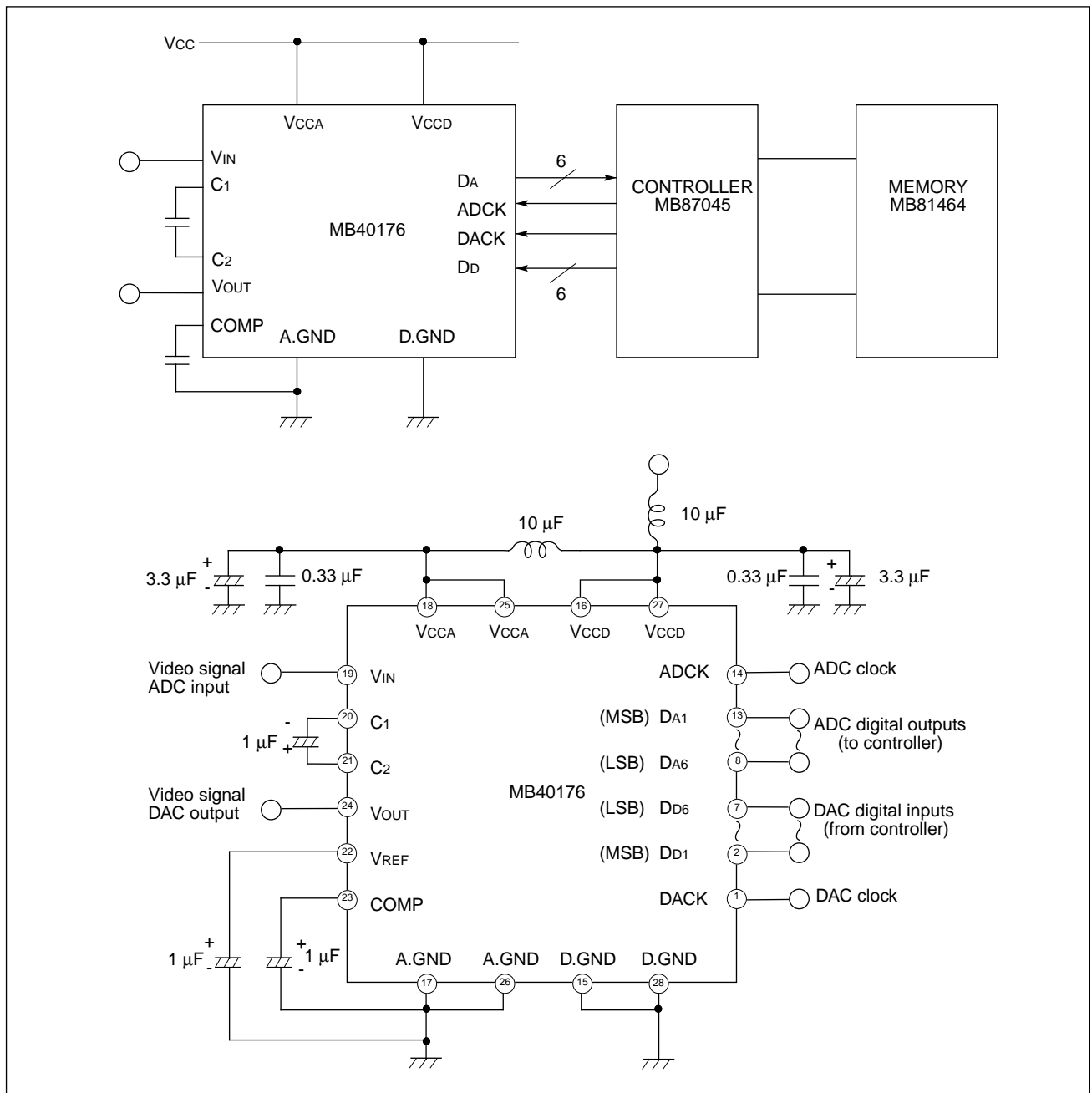


*: Input voltage range for the analog input pin is V_{REF} up to V_{CCA} .

MB40166/40176

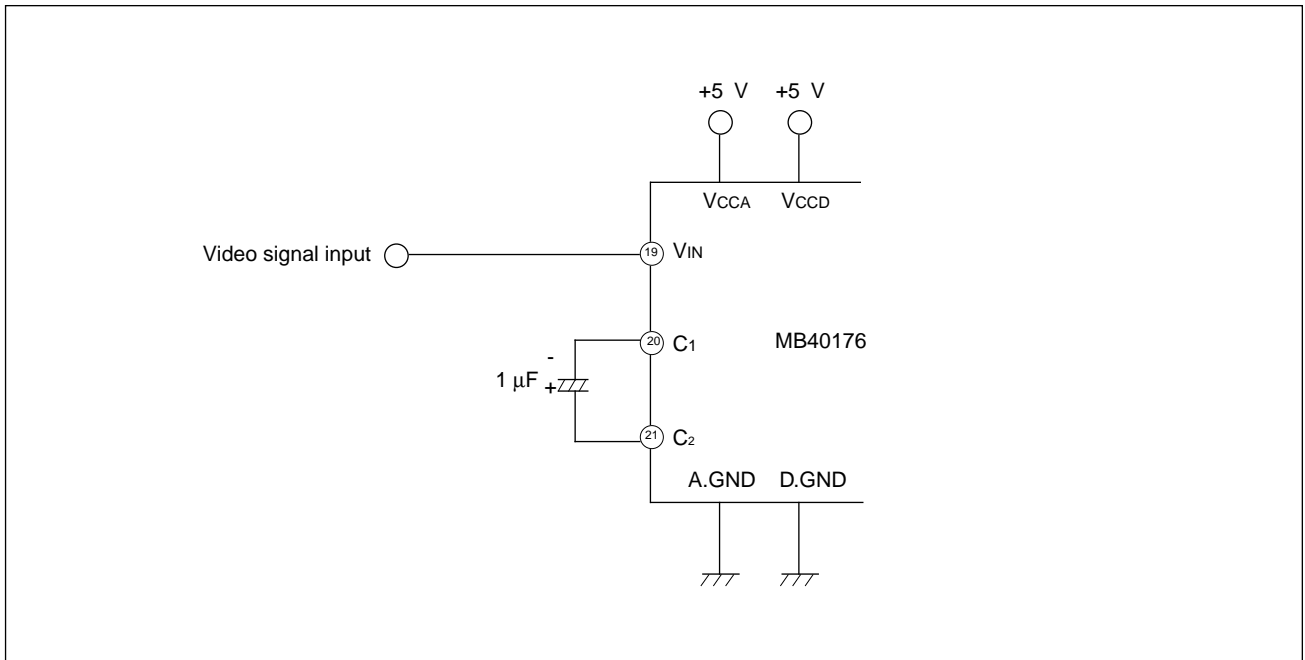
■ TYPICAL CONNECTION EXAMPLE (continued)

• MB40176



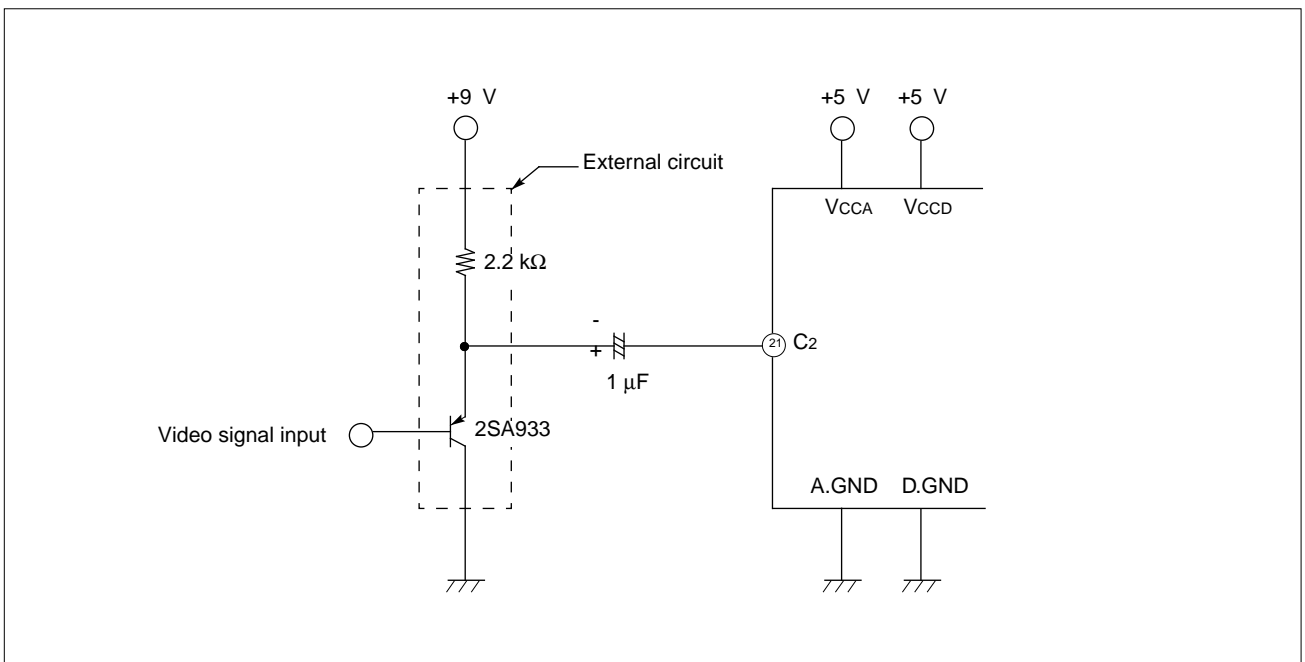
■ TYPICAL CONNECTION EXAMPLE (continued)

1. ON-CHIP Input PNP Transistor is utilized.



Note : Input impedance of V_{IN} input pin (19) is about 20 k Ω , please pay attention to output impedance of signal source.

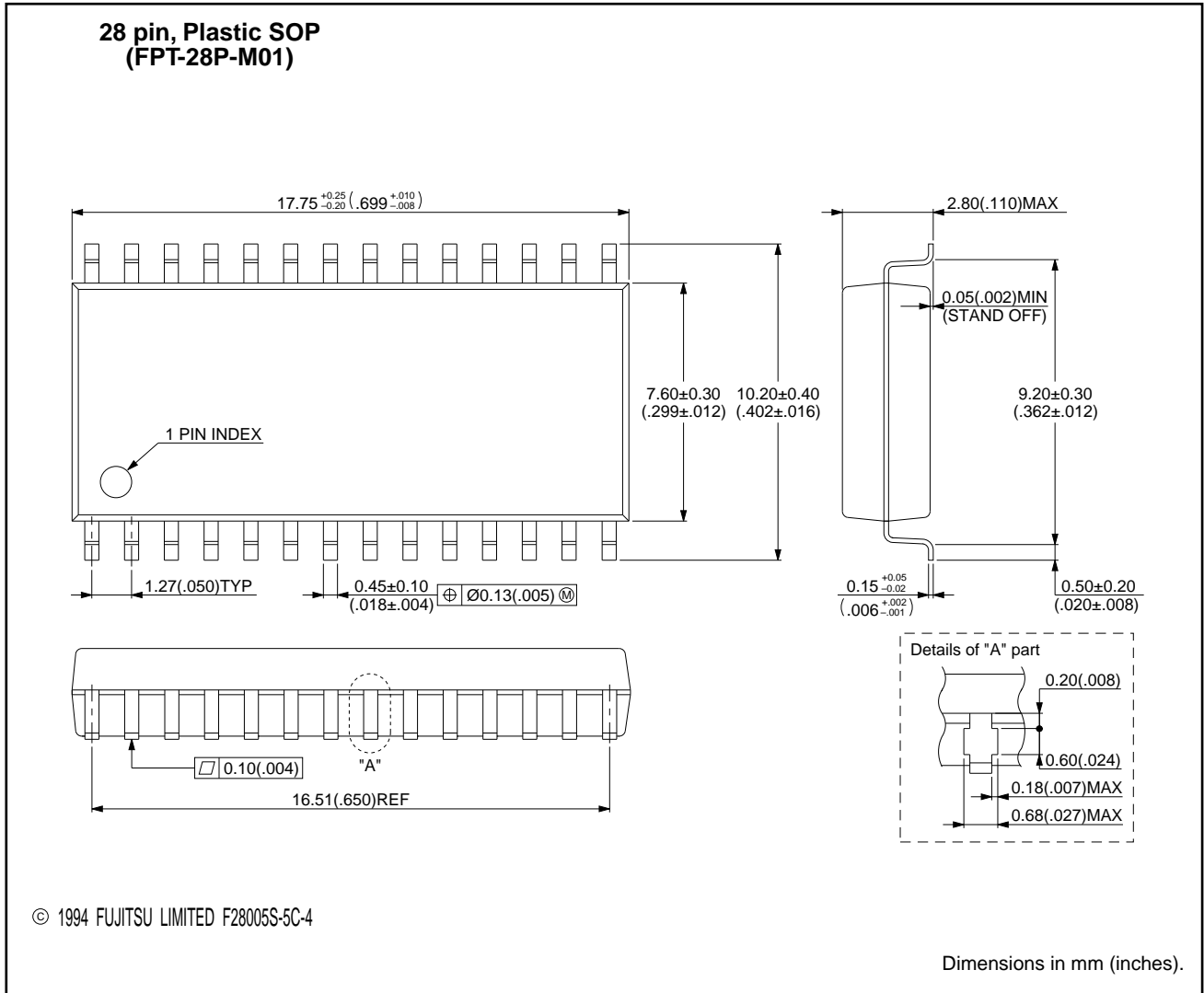
2. Input PNP Transistor of Clamp Circuit is put externally.



Note : Both V_{IN} (19) and C (20) are connected with VCCA.

MB40166/40176

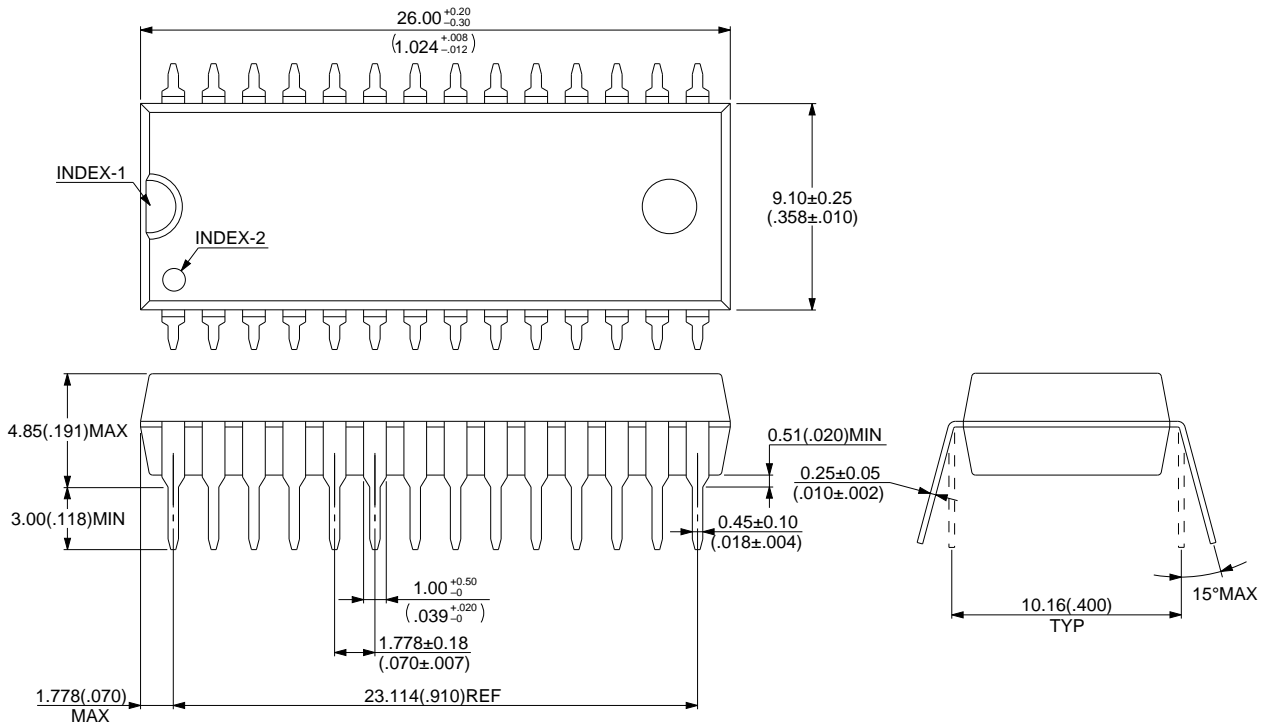
■ PACKAGE DIMENSIONS



(Continued)

(Continued)

28 pin, Plastic SH-DIP
(DIP-28P-M03)



© 1994 FUJITSU LIMITED D28012S-3C-3

Dimensions in mm (inches).

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3753
Fax: (044) 754-3329

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281 0770
Fax: (65) 281 0220

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.