

ASSP

Dual Serial Input PLL Frequency Synthesizer

On-Chip 1.1 GHz Prescaler

MB15U10

■ DESCRIPTION

The Fujitsu MB15U10 is a dual serial input phase-locked loop (PLL) frequency synthesizer and is ideally suitable for mobile communications such as cellular phones.

The MB15U10 has two PLL frequency synthesizer circuits on a single chip: one for transmission and the other for reception (PLL1 and PLL2).

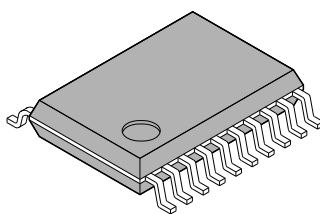
It can operate from a +2.6V to 5.5V supply. Fujitsu's advanced technology achieves an I_{CC} of 7 mA (typical) as well as 10 μ A (max.) at power saving mode.

■ FEATURES

- Two PLLs' for transmission/reception
- Low current consumption : $I_{CC} = 7$ mA typ. at 3 V
- Power saving function : $I_{PS} = 10$ μ A max.
- Divide ratio setting with serial data input :
Binary 12-bit reference counter: 6 to 4,095
Binary 17-bit main counter: 1,024 to 131,071
*Main counters can be programmed individually each other.
- On-chip constant current source charge pumps
- Adjustable charge pump output current with an external resistor
- Lock detection function
- Phase matching circuit helps fast intermittent operation
- Plastic 20-pin SSOP (shrink small outline) package

■ PACKAGE

20-pin, Plastic SSOP

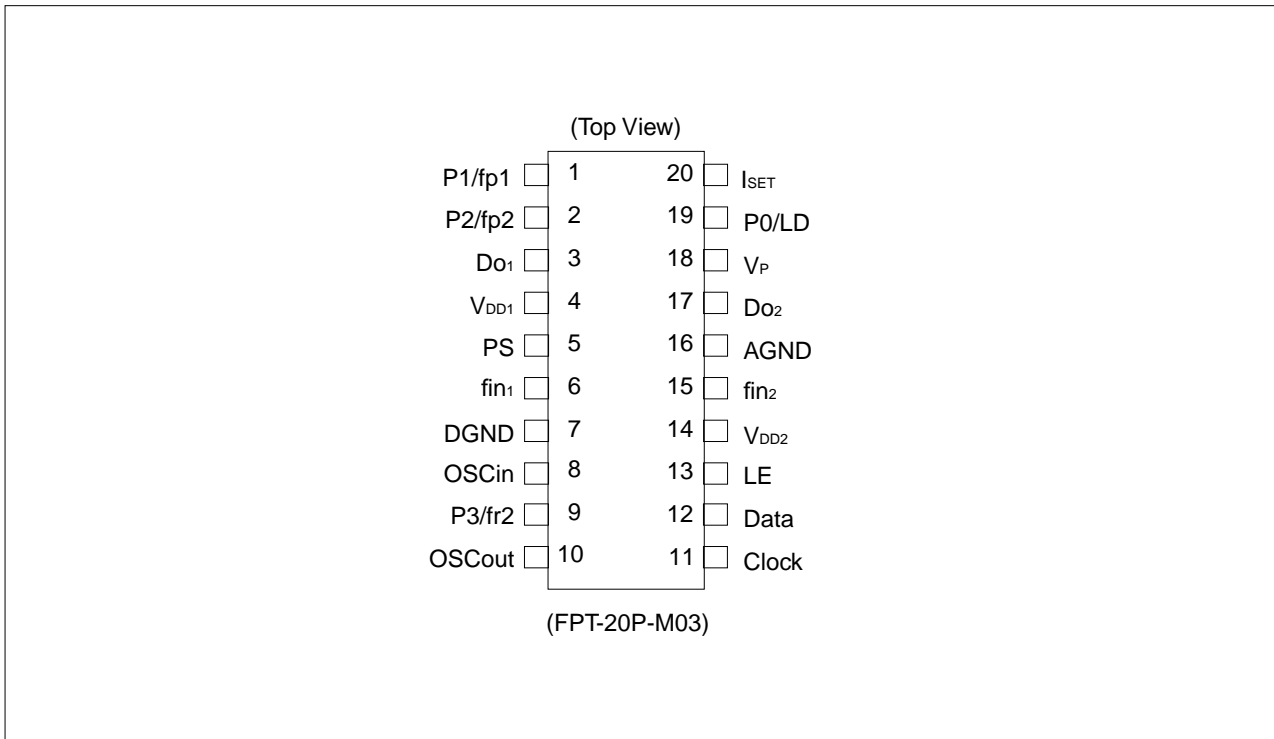


(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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■ PIN ASSIGNMENT

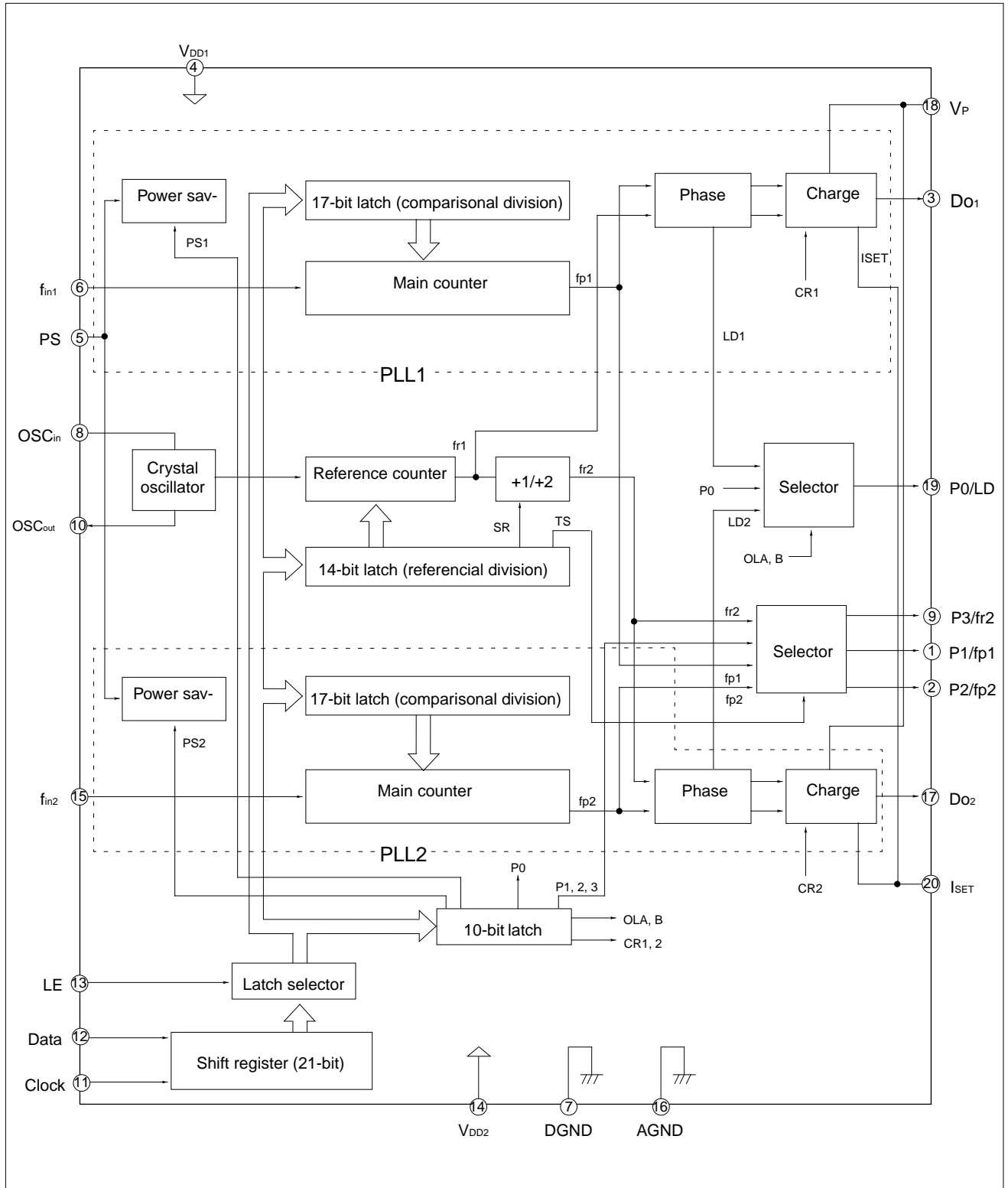


■ PIN DESCRIPTION

Pin No.	Pin name	Descriptions
1	P1/fp1	Data output / fp1 monitoring output (Open drain output)
2	P2/fp2	Data output / fp2 monitoring output (Open drain output)
3	Do ₁	Charge pump output (PLL1)
4	V _{DD1}	Power supply for digital blocks (PLL1)
5	PS	Power saving mode control (input "L" : power saving mode)
6	fin ₁	RF input (PLL1)
7	DGND	Ground for digital blocks
8	OSCI _n	Crystal oscillator or TCXO input
9	P3/fr2	Data output / fr2 monitoring output (Open drain output)
10	OSCO _{ut}	Crystal oscillator output (CMOS output)
11	Clock	Clock input
12	Data	Data input
13	LE	Load enable of serial input data (input "H" : Data is shifted into a latch.)
14	V _{DD2}	Power supply for digital blocks (PLL2)
15	fin ₂	RF input (PLL2)
16	AGND	Ground for the charge pumps
17	Do ₂	Charge pump output (PLL2)
18	V _P	Power supply for charge pump
19	P0/LD	Data output / lock detector output (Open drain output) Output is selected by "OLA" and "OLB" bits in a serial data
20	I _{SET}	Charge pump output current adjustment (A resistor is connected.)

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■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	$V_{DD1,2}$	-0.3 to +6.0	V	
	V_P	V_{DD} to 6.0	V	
Output voltage	V_O	-0.3 to $V_{DD} + 0.3$	V	
Output current	I_O	± 10	mA	
Open drain withstand voltage	V_{OOP}	-0.5 to 7.0	V	
Storage temperature	T_{stg}	-55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{DD1}, V_{DD2}	2.6	-	5.5	V	
	V_P	V_{DD}	-	6.0	V	
Input voltage	V_I	GND	-	V_{DD}	V	
Operating temperature	T_a	-30	-	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

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■ ELECTRICAL CHARACTERISTICS

Ta = 25°C

Parameter	Symbol	Value			Unit	Condition	
		Min	Typ	Max			
Power supply current (I _{DD1} + I _{DD2})	I _{DD}	–	7.0	9.0	mA	*1	
		–	11.0	13.5	mA	*2	
Stand by current	V _{DD1,2}	I _{PS}	–	–	10	μA	
Operating frequency	fin _{1,2}	f _{in} *3	90	–	1100	MHz	
	OSC _{in}	f _{OSC}	3	12.8	35	MHz	
Input sensitivity	fin _{1,2}	V _{fin}	–13	–	+1	dBm	50Ω, V _{CC} = 2.6 to 3.5V
	fin _{1,2}	V _{fin}	–7	–	+1	dBm	50Ω, V _{CC} = 3.5 to 5.5V
	OSC _{in}	V _{OSC}	0.5	–	–	Vp-p	
High-level input voltage	Data, Clock, LE, PS	V _{IH}	V _{DD} × 0.7	–	–	V	
Low-level input voltage		V _{IL}	–	–	V _{DD} × 0.3	V	
High-level input current	Data, Clock, LE, PS	I _{IH}	–	–	1.0	μA	
Low-level input current		I _{IL}	–1.0	–	–	μA	
Input current	OSC _{in}	I _{OSC}	–100	–	100	μA	
Low-level output voltage	P0 to P3	V _{OL}	–	–	0.4	V	Open drain output
Set output voltage	I _{SET}	V _{SET}	–	1.2	–	V	R _{SET} = 5kΩ to 60kΩ
High-impedance cut off current	D _O , P0 to P3	I _{OFF}	–	–	1.1	μA	
Output current	D _{O1,2}	I _{DOH1} *4	1.4	1.9	2.4	mA	R _{SET} = 7kΩ connected. CR1, 2 bits = "1" V _{DD} = 3.0V, V _P = 5.0V
		I _{DOL1} *4	1.4	1.9	2.4	mA	
	D _{O1,2}	I _{DOH0}	0.7	0.96	1.2	mA	R _{SET} = 7kΩ connected. CR1, 2 bits = "0" V _{DD} = 3.0V, V _P = 5.0V
		I _{DOL0}	0.7	0.96	1.2	mA	
	P0 to P3	I _{OL}	1.0	–	–	mA	Open drain

Note: *1 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 3.0 V. In locked state.

*2 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 5.0 V. In locked state.

*3 ; AC coupling with a 1000 pF capacitor connected.

*4 ; The symbol "–" (minus) means direction of current flow.

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b) Data setting description

- Table 1 : MA0 to MA16 : Divide ratio of the binary 17-bit main counter (PLL1)

Divide Ratio (MA)	MA16	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 1,024 are prohibited. (Divide ratio = 1,024 to 131,071)

- Table 2 : MB0 to MB16 : Divide ratio of the binary 17-bit main counter (PLL2)

Divide Ratio (MB)	MB16	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 1,024 are prohibited. (Divide ratio = 1,024 to 131,071)

- Table 3 : R0 to R11 : Divide ratio of the binary 12-bit reference counter

Divide Ratio (R)	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
6	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 6 are prohibited. (Divide ratio = 6 to 4,095)

- Table 4 : Divide ratio select bit of reference frequency (PLL1 and PLL2)

SR	Divide ratio of reference frequency (PLL1)	Divide ratio of reference frequency (PLL2)
0	R	R
1	R	2R

Note: R = Programmed value with R0 to R11 bits

- Table 5 : P0 to P3 ; P0 to P3 outputs control

PX bit	PX output (19, 1, 2, 9 pins)
0	ON ("L")
1	OFF ("Z")

Notes: X = 0 to 3

- Table 6 : OLA, OLB ; 19-pin output selection

OLA	OLB	19-pin output
0	0	P0 signal
0	1	Lock detect signal (PLL2)
1	0	Lock detect signal (PLL1)
1	1	Lock detect signal (PLL1 and PLL2)

- Table 7 : CR1, CR2 ; Charge pump output current selection

CR1, 2	Charge pump output current
0	I_{DO}
1	$2I_{DO}$

Notes: PLL1 and PL2 can be controlled individually.

- Table 8 : PS ; Power saving control

PS1, 2	Operating mode
0	Power saving mode
1	Operation

Notes: PLL1 and PL2 can be controlled individually.

- Table 9 : TS ; Test bit (Set to "0" at ordinary use.)

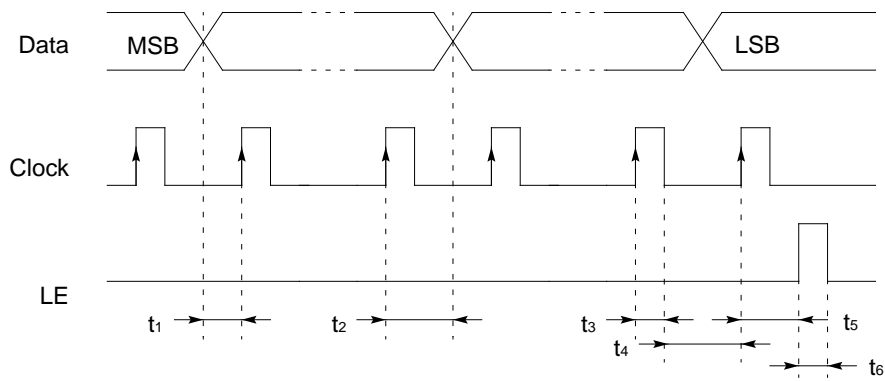
TS	1-pin	2-pin	9-pin
0	Output P1 signal	Output P2 signal	Output P3 signal
1	Outputs fp1	Outputs fp2	Outputs fp3

Notes: Reference frequency and comparison frequency can be monitored via P1 to P3 pins.

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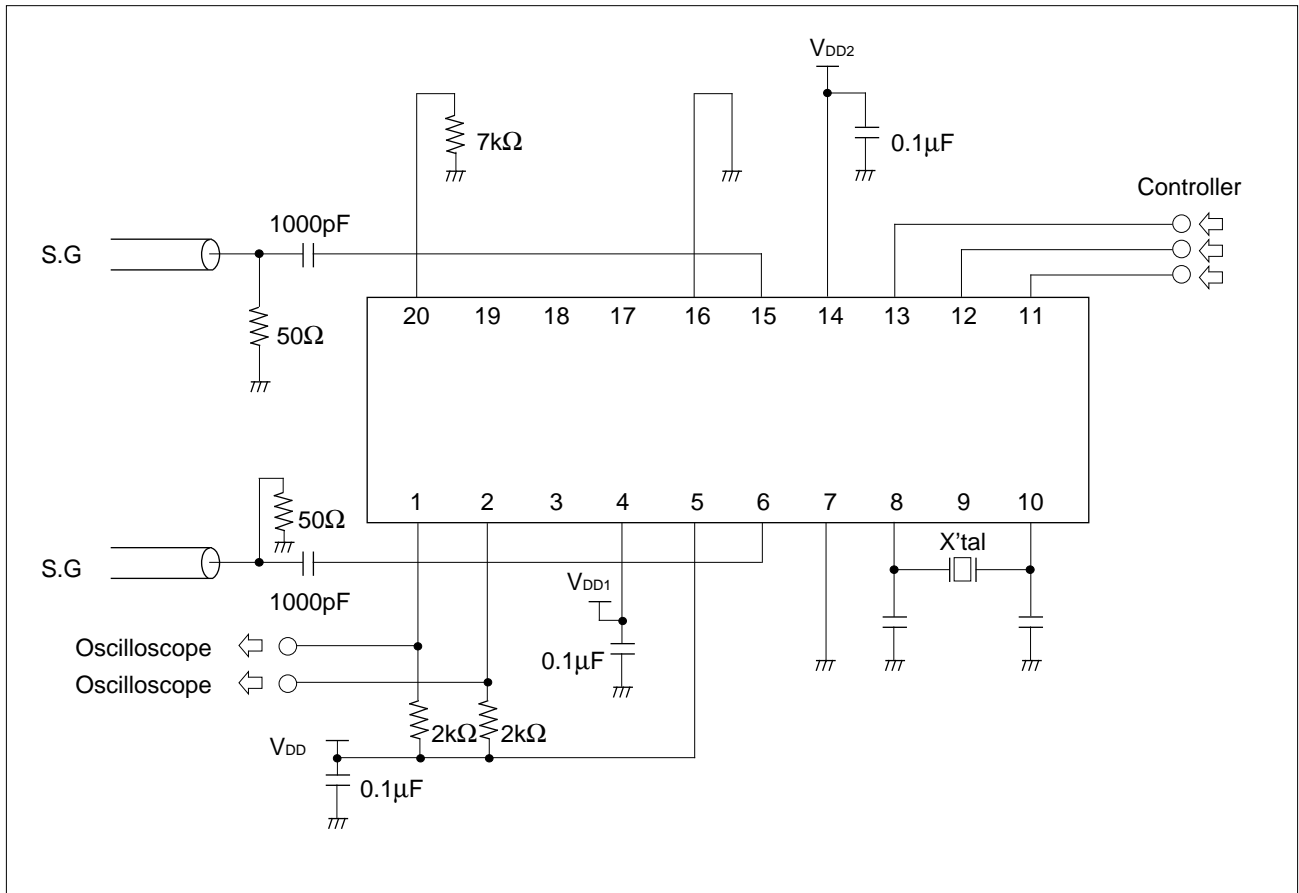
Serial Data Input Timing

- $t_1 (\geq 20 \text{ ns})$, $t_2 (\geq 20 \text{ ns})$, $t_3 (\geq 50 \text{ ns})$, $t_4 (\geq 50 \text{ ns})$, $t_5 (\geq 20 \text{ ns})$, $t_6 (\geq 1000 \text{ ns})$



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

■ TEST CIRCUIT (for Measuring fin Input Sensitivity)



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■ TYPICAL CHARACTERISTICS

Do Output Current

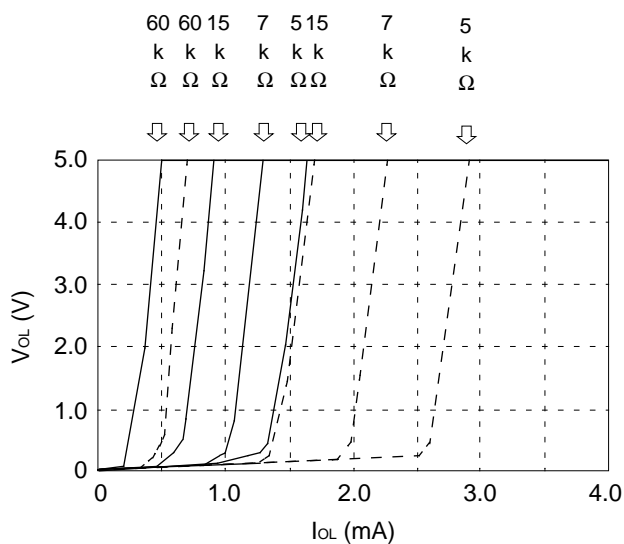
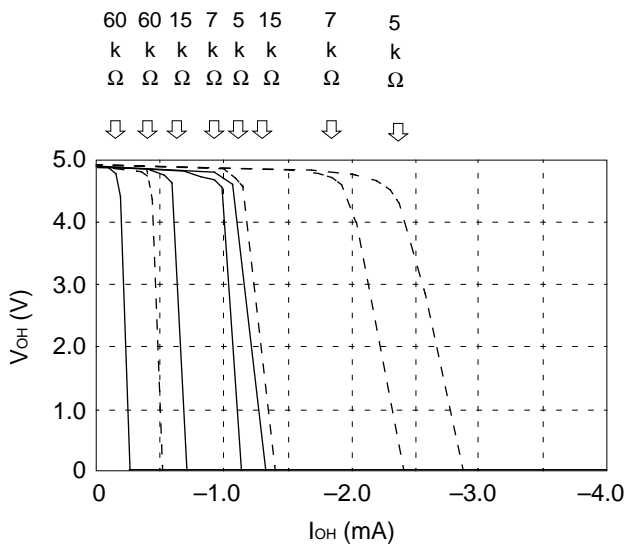
Conditions : Ta = +25°C

V_{DD} = 3 V

V_p = 5 V

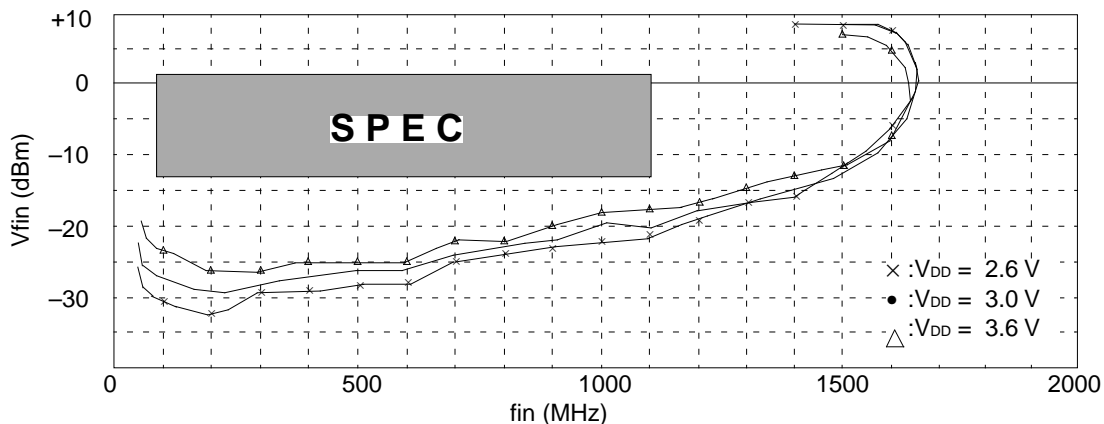
I_{SETR} = 5 k, 7 k, 15 k, 60 k

--- CR = "H"
— CR = "L"

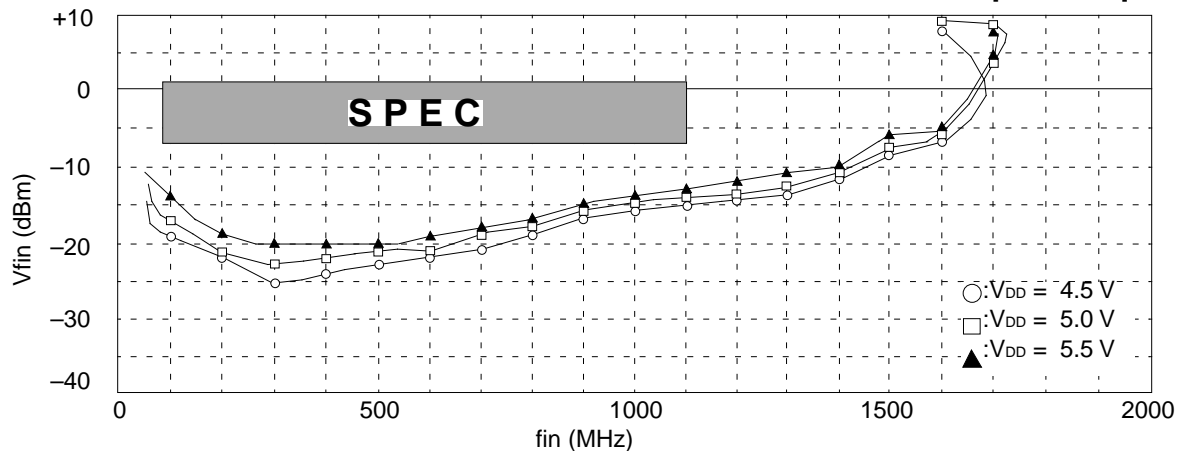


fin Input Sensitivity

[Ta = +25°C]



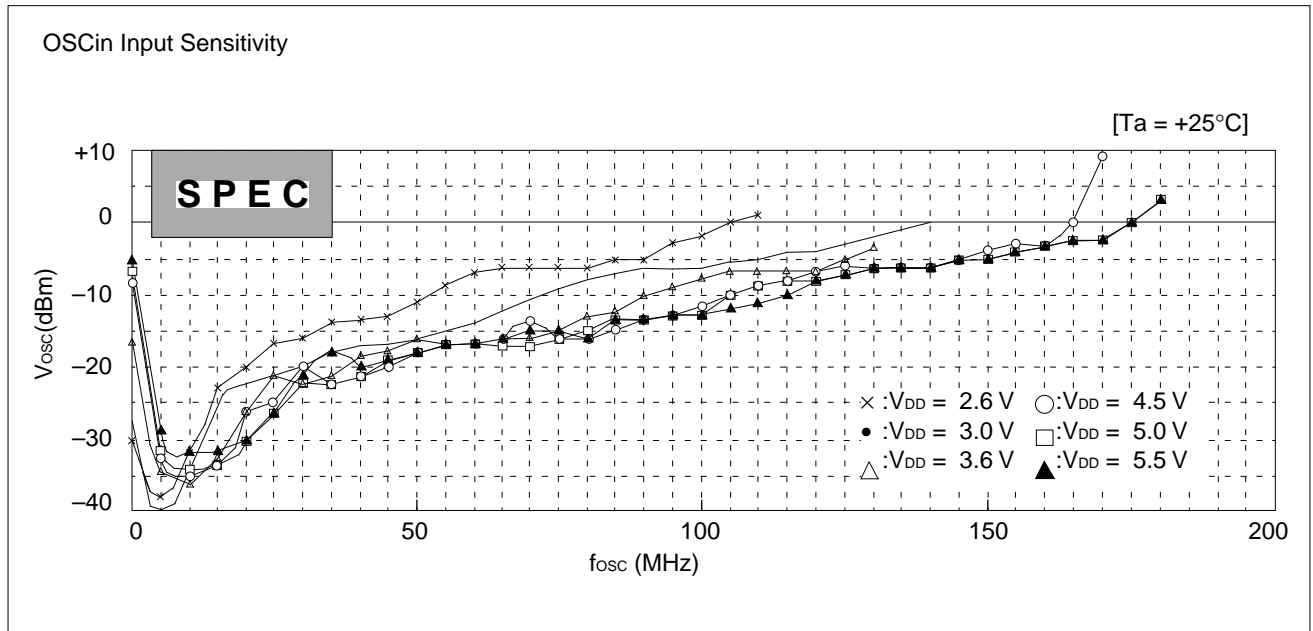
[Ta = +25°C]



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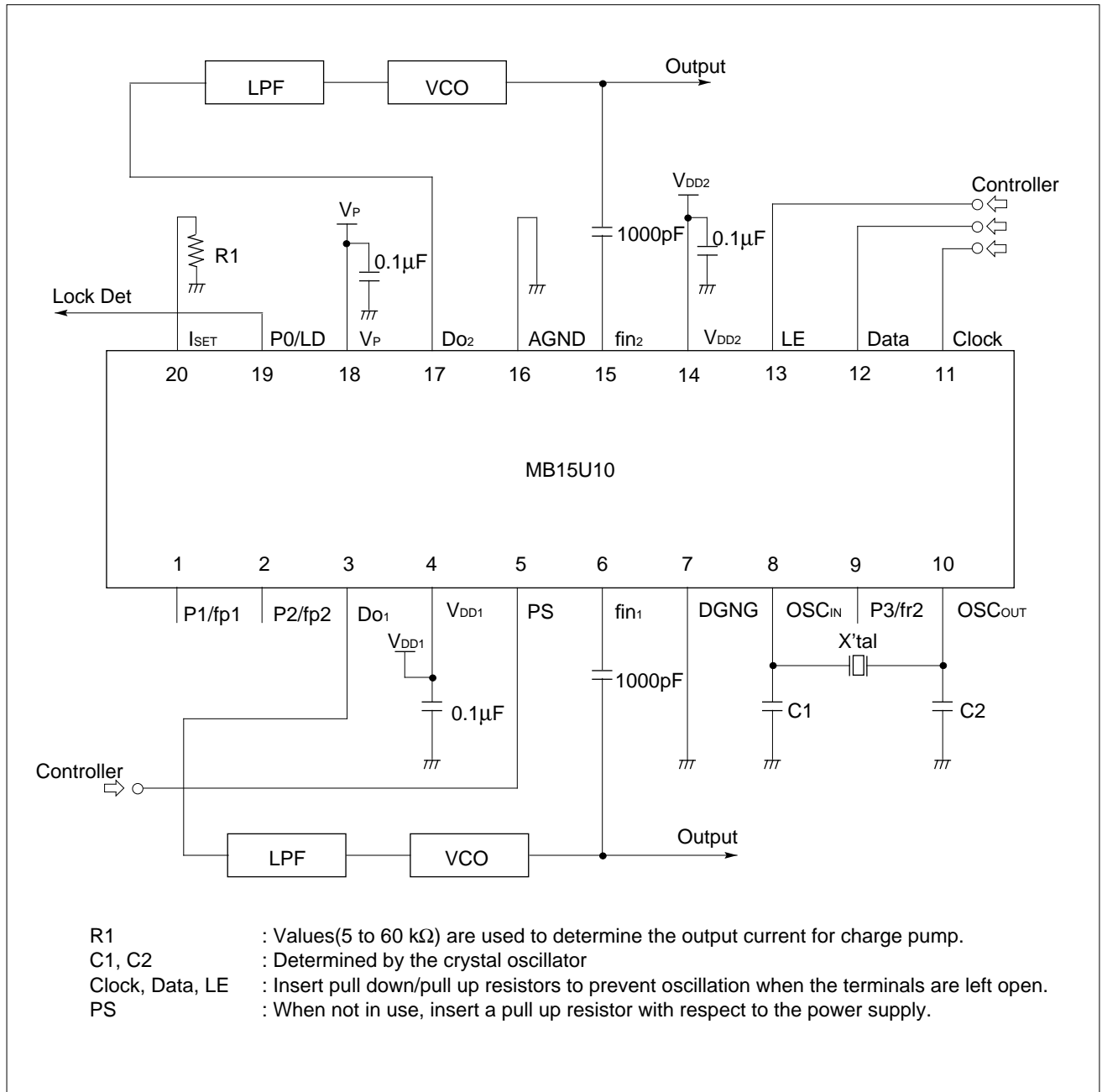
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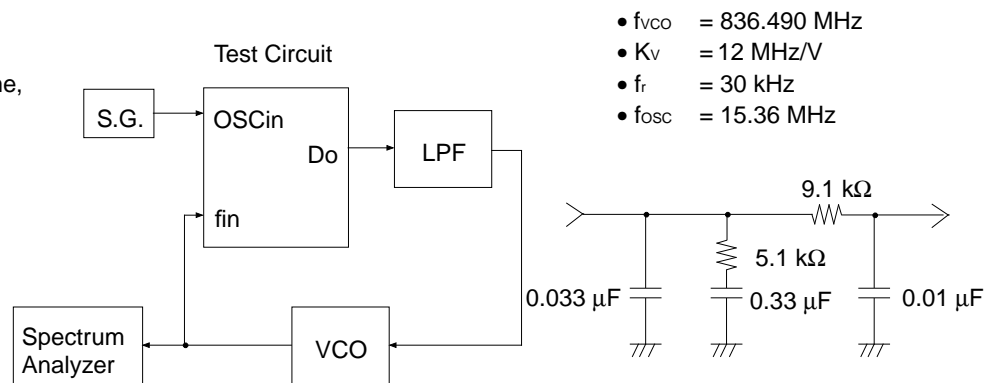
APPLICATION EXAMPLE



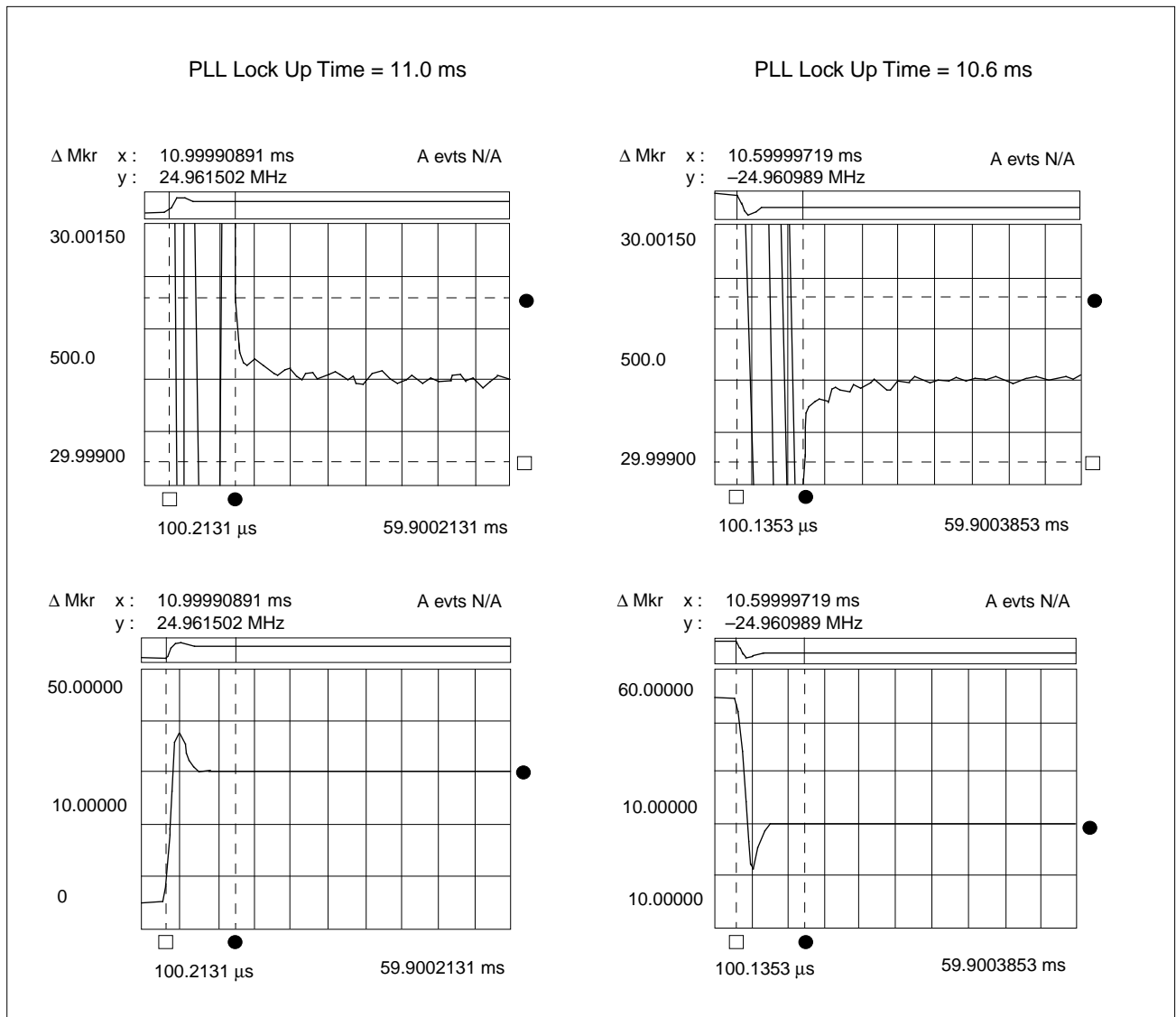
REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below.

Each plots shows lock up time, phase noise, and reference



- $f_{VCO} = 836.490 \text{ MHz}$
- $K_V = 12 \text{ MHz/V}$
- $f_r = 30 \text{ kHz}$
- $f_{osc} = 15.36 \text{ MHz}$



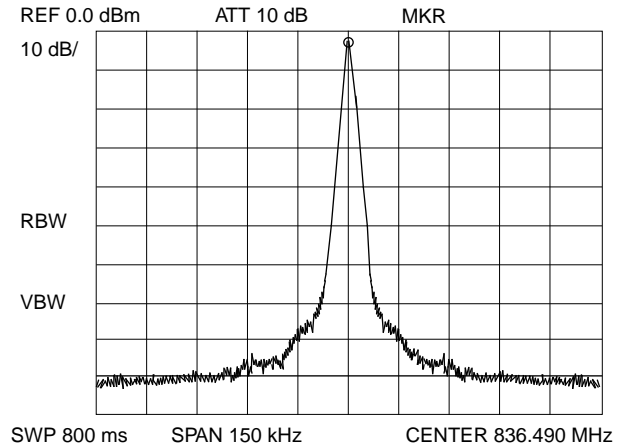
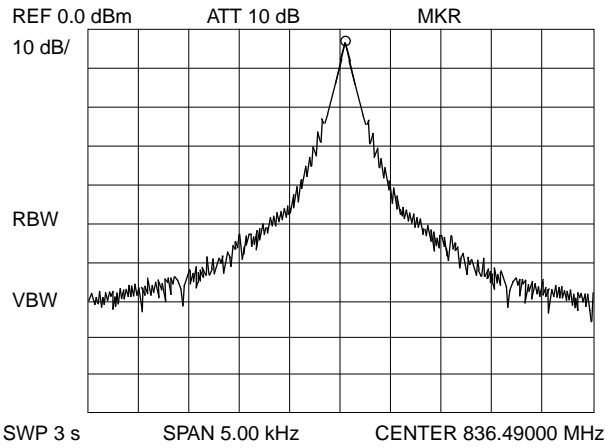
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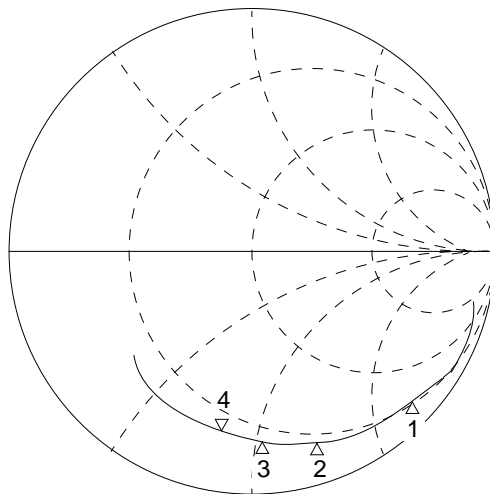
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PLL Phase Noise (Tx mode)

PLL Reference Leakage (Tx mode)

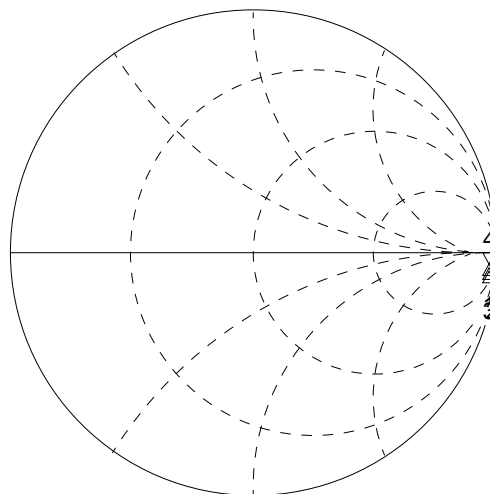


fin Input Impedance



- 1: 20.93 Ω
-130.75 Ω
500 MHz
- 2: 11.281 Ω
-71.824 Ω
800 MHz
- 3: 11.871 Ω
-51.166 Ω
1 GHz
- 4: 11.627 Ω
-42.119 Ω
3.4352 pF
1.1 GHz

OSCin Input Impedance



- 1: 1.5699 k Ω
-2.6509 k Ω
10 MHz
- 2: 889.63 Ω
-2.0951 k Ω
15 MHz
- 3: 537.31 Ω
-1.6434 k Ω
20 MHz
- 4: 342.19 Ω
-1.3733 k Ω
4.6357 pF
25 MHz

MB15U10**■ ORDERING INFORMATION**

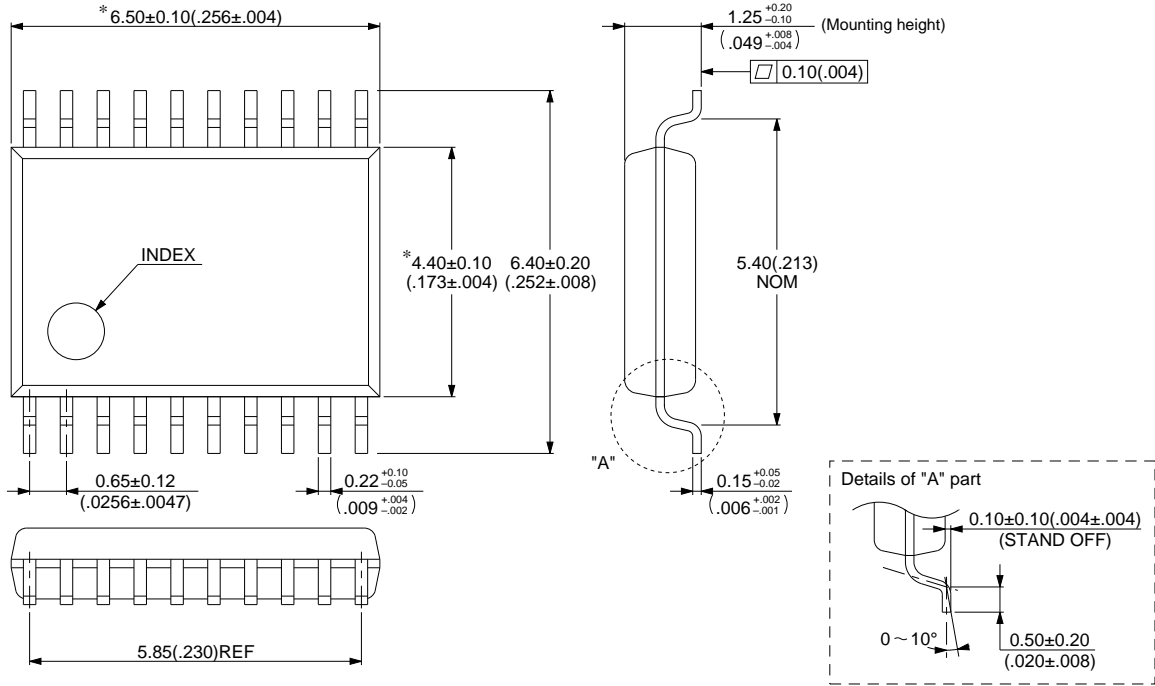
Part number	Package	Remarks
MB15U10PFV	20pin, Plastic SSOP (FPT-20P-M03)	

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■ PACKAGE DIMENSION

20 pin, Plastic SSOP
(FPT-20P-M03)

*: These dimensions do not include resin protrusion.



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