Ordering number : EN6094

Bi-CMOS IC

LV1110NM

Digital Surround Processor IC

Overview

The LV1110NM is a digital surround processor IC developed for miniature stereo components and radio-cassette combinations. The major features built into this Bi-CMOS single-chip solution are function switching, recording volume control, surround processing, karaoke processing, 3-band graphic equalizer, and master volume control.

Features

- The built-in delay functions include input and output filters, analog-to-digital and digital-to-analog converters, delay lines with built-in memory, and delay reverberation. Other functions available are fixed matrix (L+R and L-R) and front mixing (choice of level or phase). These functions may be freely combined to easily produce a variety of surround modes and thus simulate a wide range of acoustic environments.
- The built-in karaoke functions include a vocal canceler, microphone echo, key control I/O, and other support for audio multiplexing software.

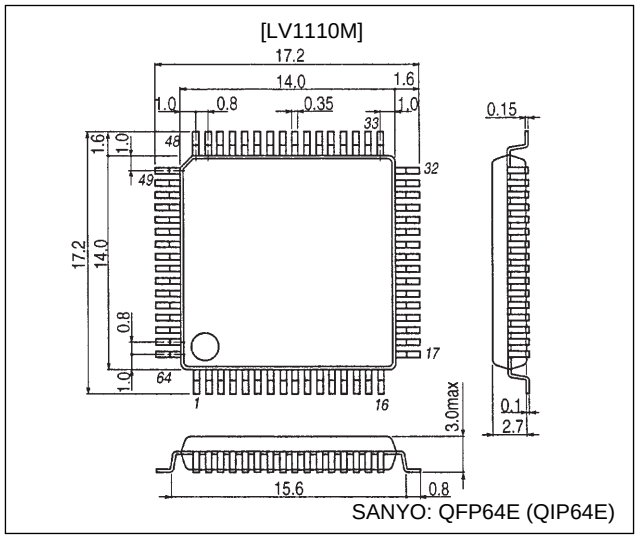
Functions

- Input function switching (Five channels with built-in 6-dB amplifier)
- Two REC output pins with volume controls (Two channels with on/off switches and choice of function output or mixer output)
- Input switching (choice of L+R, L–R, and L or R only)
- Microphone input (on/off)
- Vocal canceler
- Key control I/O pins
- Front addition (+3 dB, –3 dB, –5 dB, mute)
- I/O filters in delay block (choice of 2-, 5-, and 28-kHz low pass filters or through operation)
- Reverberation functions (with built-in volume control)
- Built-in SRAM (8 kilobytes)
- Variable delay (choice of 15, 20, 25, 30, 40, 50, 100, and 120 ms)
- Built-in V_{DD}
- I/O through or mute
- Three-band graphic equalizer (boost or cut with three steps each)
- Master volume control from 0 to –79 dB in 1-dB steps
- QIP-64E package with 0.8-mm pin pitch

Package Dimensions

unit: mm

3159-QFP64E



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SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{CC} max		12	V
Maximum power dissipation	Pd max	Ta ≤ 70°C 114.3 × 76.1 × 1.6 mm³ Mounted on glass epoxy circuit board	500	mW
Operating temperature	Topr		–25 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended power supply voltage	V_{CC}		9	V
Operating power supply voltage range	V_{CC} opg		8 to 11	V
Control data high-level voltage	V_{IH}		3.5 to 5.5	V
Comtrol data low-level voltage	V_{IL}		0 to 1.2	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 9 V, f_{IN} = 1 kHz, V_{IN} = 300 mVrms = 0 dB, R_L = 10 kΩ

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Qurescent current	I_{CCO}		19	28	42	mA
Input function switching (measured for function in input / function out)						
Output level deviation	VG_F1	IN A, D	–2	0	+2	dB
	VG_F2	IN B, C, E	4	6	8	dB
Maximum output voltage	V_{OF}	V_{CC} = 8.5 V, THD = 1%	2.0	2.4		V
Distortion	THD_F	400 to 30 kHz BPF		0.005	0.03	%
Output noise voltage	V_{NOF}	Rg = 10 kΩ, JISA		–102	–95	dBV
Interchannel crosstalk	CT_F	Rg = 10 kΩ/V_O = 1 Vrms, JIS A	82	100		dB
L and R channel total throughput (measured for L and R inputs and L and R outputs)						
Output level deviation	VG_T		–2	0	+2	dB
Signal handling	SH_T	V_{CC} = 8.5 V, THD = 1%, 300 mVrms = 0 dB	15.0	16.5		dB
Distortion	THD_T	400 to 30 kHz BPF		0.005	0.03	%
Signal-to-noise ratio	SNT	Rg = 10 kΩ, CCIR-ARM, 300 mVrms = 0 dB	85	100		dB
Interchannel crosstalk	CT_T	Rg = 10 kΩ/V_O = 1 Vrms, JIS A	82	94		dB
S channel (measured for delay = 20 ms, reverb. off, L-R, S-IN input, S-OUT output)						
Output level deviation	VG_S		–3	0	+3	dB
Signal handling	SH_S	THD = 3%, 300 mVrms = 0 dB, V_{CC} = 8.5 V	15.0	16.5		dB
Distortion	THD_S	400 to 30 kHz BPF, OUT FILTER: 5 kHz LPF		0.1	0.7	%
Signal-to-noise ratio	SN_S	Rg = 10 kΩ, CCIR-ARM, 300 mVrms = 0 dB OUT FILTER: 5 kHz LPF	60	68		dB
Long delay (measured for delay = 100 ms, reverb. off, MIC-IN input, S-OUT output)						
Output level deviation	VG_D	OUT FILTER: 2 kHz LPF	–4.5	–1.5	+1.5	dB
Maximum output voltage	V_{OD}	THD = 3%, V_{CC} = 8.5 V	1.4	1.8		V
Distortion	THD_D	400 to 30 kHz BPF, OUT FILTER: 2 kHz LPF		2.0	3.0	%
Output noise voltage	V_{NOD}	Rg = 10 kΩ, JIS A, OUT FILTER: 2 kHz LPF		–75	–66	dBV
Vocal cut	VC		–16	–20	–24	dB
[REC output (measured for volume = 0 dB, function in, A input, REC OUT)]						
Output level deviation	VG_R		–2	0	+2	dB
Maximum output voltage	V_{OR}	THD = 1%, V_{CC} = 8.5 V	1.6	2.0		V
Distortion	THD_R	400 to 30 kHz BPF		0.006	0.03	%
Output noise voltage	V_{NOR}	Rg = 10 kΩ, JIS A		–106	–95	dBV
Interchannel crosstalk	CT_R	Rg = 10 kΩ/V_O = 1 Vrms, JIS A	82	100		dB
Mute attenuation ratio	MT_R	JIS A, V_{IN} = 1 Vrms = 0 dB	–75	–86		dB

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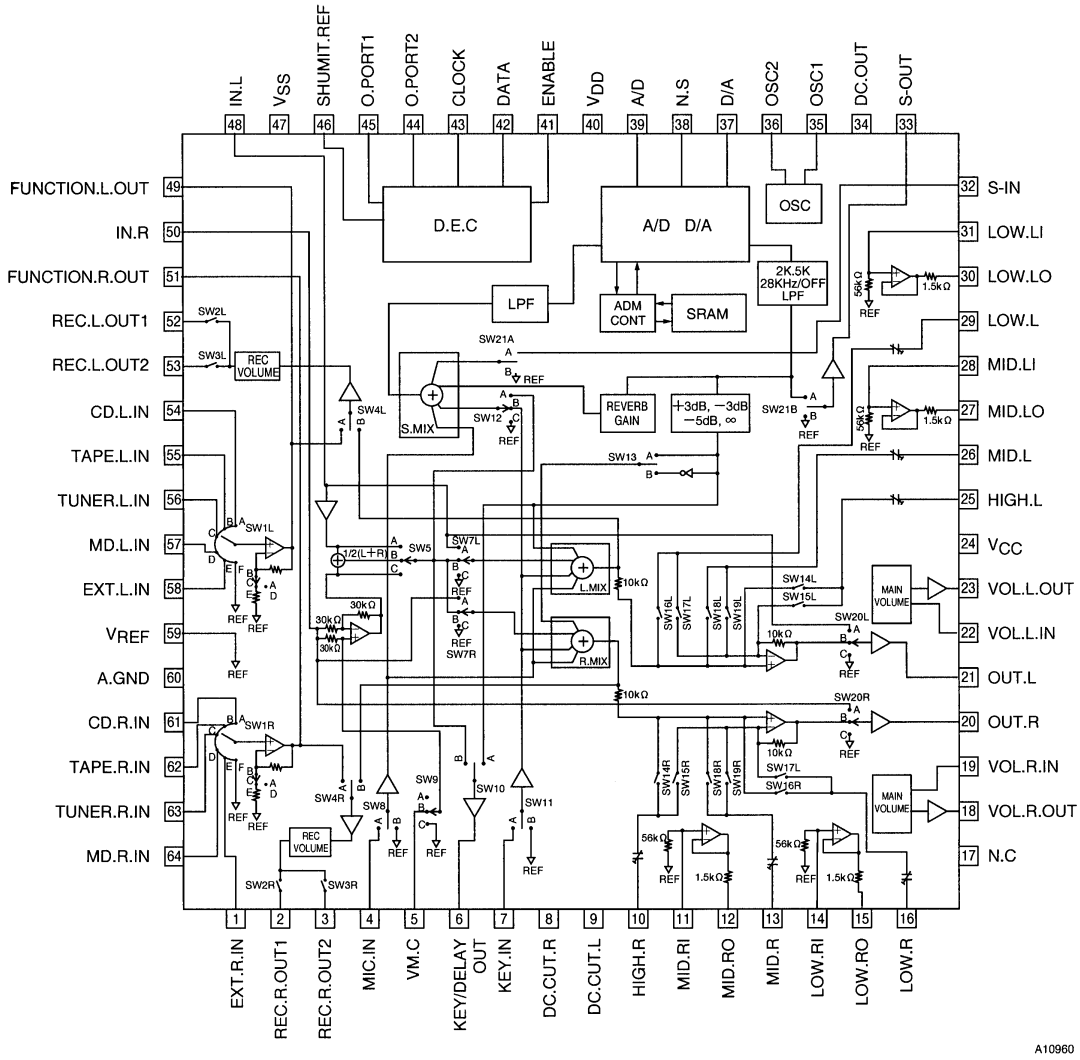
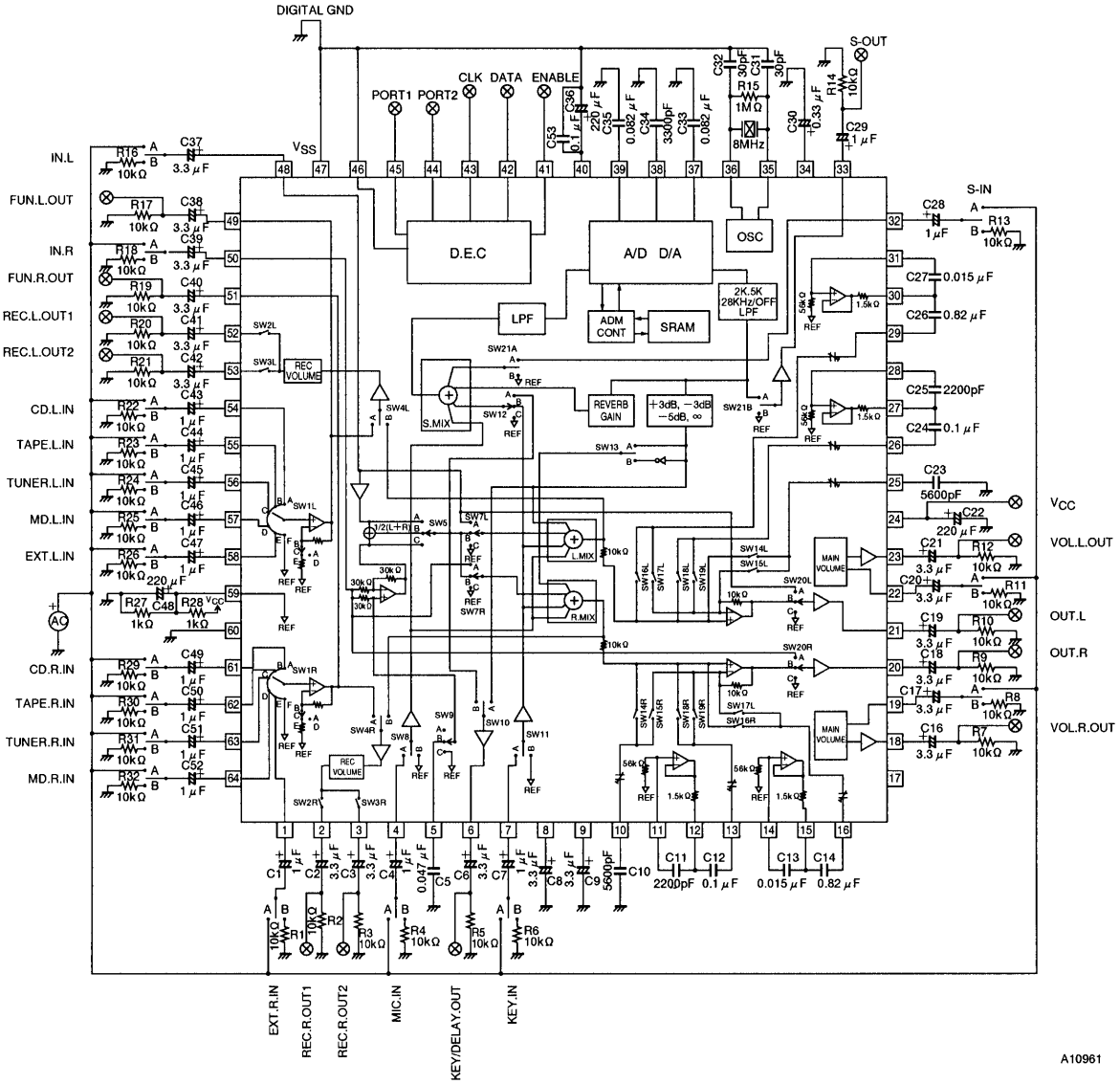
Electrical Characteristics at Ta = 25°C, V_{CC} = 9 V, f_{IN} = 1 kHz, V_{IN} = 300 mVrms = 0 dB, R_L = 10 kΩ

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Master volume control (measured for volume = maximum, VOL IN input, VOL OUT output)						
Output level deviation	VG_V		–2	0	+2	dB
Maximum output voltage	V_{OV}	V_{CC} = 8.5 V, THD = 1%	1.6	2.0		V
Distortion	THD_V	400 to 30 kHz BPF		0.006	0.03	%
Output noise voltage	V_{NOV}	Rg = 10 kΩ, JIS A		–107	–95	dBV
Interchannel crosstalk	CT_V	Rg = 10 kΩ/V_O = 1 Vrms = 0 dB, JIS A	85	103		dB
Mute attenuation ratio	MT_V	JIS A, V_{IN} = 300 mV = 0 dB	–70	–78		dB
Graphic equalizer (measured for IN,L,R input / OUT L,R)						
Boost amount	VGE_U1	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: BOOST1: f_{IN} = 10 kHz	1.7	3	4.3	dB
	VGE_U2	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: BOOST2: f_{IN} = 10 kHz	4.7	6	7.3	dB
	VGE_U3	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: BOOST3: f_{IN} = 10 kHz	8.5	10	11.5	dB
Cut amount	VGE_D1	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: CUT1: f_{IN} = 10 kHz	–4.3	–3	–1.7	dB
	VGE_D2	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: CUT2: f_{IN} = 10 kHz	–7.3	–6	–4.7	dB
	VGE_D3	BASS: f_{IN} = 100 Hz, MID: f_{IN} = 1 kHz, TREBLE: CUT3: f_{IN} = 10 kHz	–11.5	–10	–8.5	dB

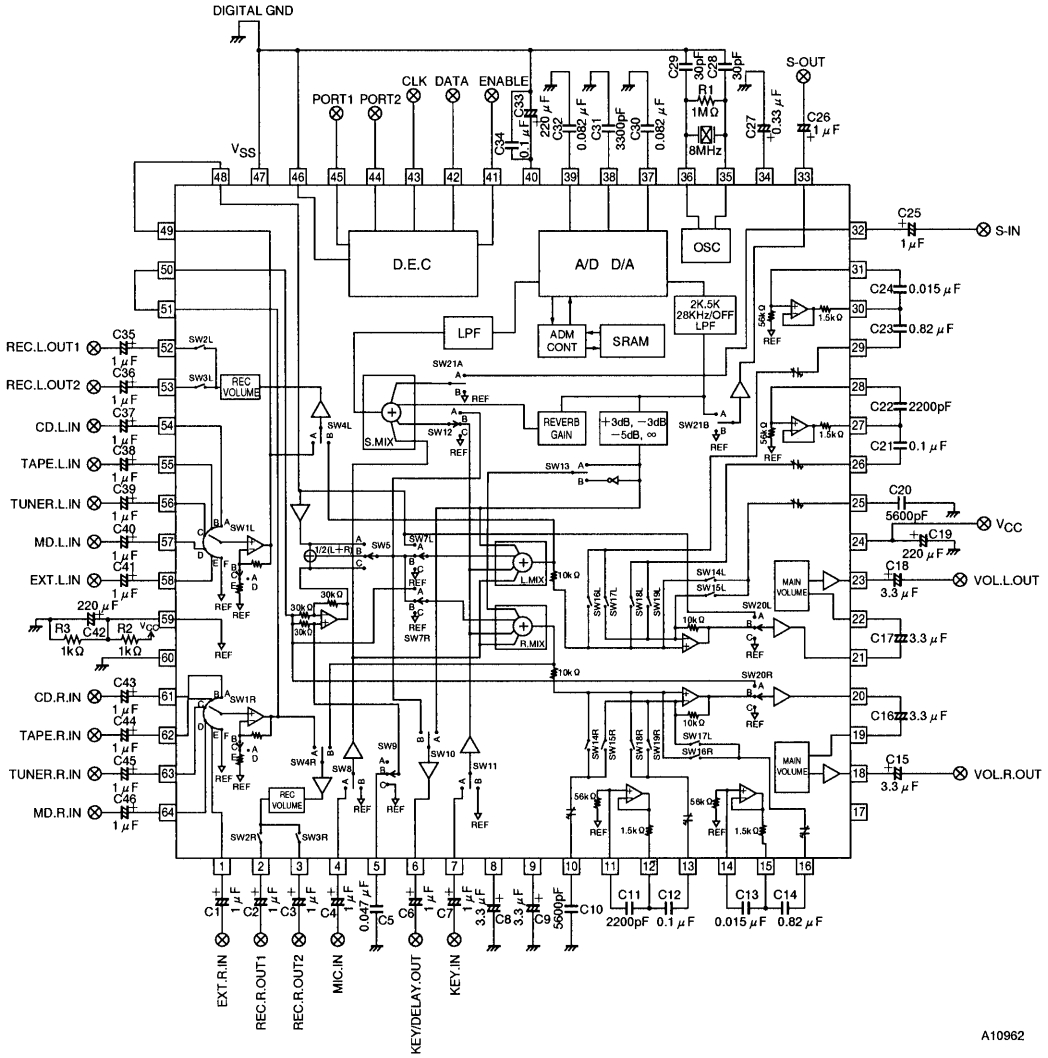
Block Diagram



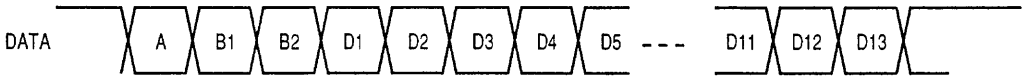
Measurement Circuit



Sample Application Circuit



Control Format



A = “Low” level selects the LV1110M.
B1 and B2 specify the data mode (LL, HL, LH, or HH).
D1 to D13 give the data.

A = L, B1 = L, B2 = L
Input function switching

D1, D2, D3	Function	Notes
L, L, L	MUTE	SW1 = F
L, L, H	CD.IN	SW1 = A
L, H, L	Tape.IN	SW1 = B, VG = 6 dB
L, H, H	Tuner.IN	SW1 = C, VG = 6 dB
H, L, L	MD.IN	SW1 = D
H, L, H	EXT.IN	Sw1 = E, VG = 6 dB

Input switching See the Block Diagram for the SW modes.

D4, D5, D6	Function	SW5	SW9	SW20
L, L, L	L + R	B	A	B
L, L, H	L – R	B	C	B
L, H, L	L Only	A	A	B
L, H, H	R Only	C	A	B
H, L, L	Matrix Through	B	A	B
H, L, H	Total Through	B	A	A

Vocal canceler (When on, set D4, D5, and D6 for L+R mode.)

	L	H
D7	OFF : SW9 = A	ON : SW9 = B

Microphone input

	L	H
D8	OFF : SW8 = B	ON : SW8 = A

Key control switching

D9	Function	SW7	SW10	SW11
L	OFF	A/B	A	B
H	ON	C	B	A

Stereo/matrix switching

	L	H
D10	SW7 = A	SW7 = B

S-IN/S-OUT switching

	L	H
D11	SW OFF	SW ON

Delay input switching

	Function
L, L	SW12 = C
L, H	SW12 = A
H, L	SW12 = B

A = L, B1 = H, B2 = L

Out filter switching

D1, D2	Level
L, L	Through
L, H	28 kHz L.P.F.
H, L	5 kHz, L.P.F
H, H	2 kHz L.P.F.

Reverberation level

D3, D4, D5	Level
L, L, L	–∞
L, L, H	–9 dB
L, H, L	–7 dB
L, H, H	–5 dB
H, L, L	–3 dB
H, L, H	–2 dB
H, H, L	–1 dB
H. H. H	0 dB

Delay

D6, D7, D8	Level
L, L, L	15 ms
L, L, H	20 ms
L, H, L	25 ms
L, H, H	30 ms
H, L, L	40 ms
H, L, H	50 ms
H, H, L	100 ms
H. H. H	120 ms

System muting

	L	H
D9	Muting on	Muting off

L and R muting

	L	H
D10	Muting on	Muting off

Effect R channel ADD

	L	H
D11	In-phase addition SW13 = A	Inverted phase addition SW13 = B

Front ADD effect volume

D12, D13	Level
L, L	–∞
L, H	–5 dB
H, L	–3 dB
H, H	+3 dB

A = L, B1 = L, B2 = H

Graphic equalizer BASS

D1, D2, D3	Level
L, L, L	–10 dB
L, L, H	–6 dB
L, H, L	–3 dB
L, H, H	0 dB
H, L, L	+10 dB
H, L, H	+6 dB
H, H, L	+3 dB
H. H. H	0 dB

Graphic equalizer MID

D4, D5, D6	Level
L, L, L	–10 dB
L, L, H	–6 dB
L, H, L	–3 dB
L, H, H	0 dB
H, L, L	+10 dB
H, L, H	+6 dB
H, H, L	+3 dB
H. H. H	0 dB

Graphic equalizer TREBLE

D7, D8, D9	Level
L, L, L	–10 dB
L, L, H	–6 dB
L, H, L	–3 dB
L, H, H	0 dB
H, L, L	+10 dB
H, L, H	+6 dB
H, H, L	+3 dB
H. H. H	0 dB

Port control (D10: PORT1, D11: PORT2)

	L	H
D10	L	H
D11	L	H

A = L, B1 = H, B2 = H, D1 = L

Left channel master volume control — Attenuation (dB)

D2	D3	D4	D5	D6	D7	D8	ATT	D2	D3	D4	D5	D6	D7	D8	ATT
L	L	L	L	L	L	L	0	L	H	L	H	L	H	L	–42
L	L	L	L	L	L	H	–1	L	H	L	H	L	H	H	–43
L	L	L	L	L	H	L	–2	L	H	L	H	H	L	L	–44
L	L	L	L	L	H	H	–3	L	H	L	H	H	L	H	–45
L	L	L	L	H	L	L	–4	L	H	L	H	H	H	L	–46
L	L	L	L	H	L	H	–5	L	H	L	H	H	H	H	–47
L	L	L	L	H	H	L	–6	L	H	H	L	L	L	L	–48
L	L	L	L	H	H	H	–7	L	H	H	L	L	L	H	–49
L	L	L	H	L	L	L	–8	L	H	H	L	L	H	L	–50
L	L	L	H	L	L	H	–9	L	H	H	L	L	H	H	–51
L	L	L	H	L	H	L	–10	L	H	H	L	H	L	L	–52
L	L	L	H	L	H	H	–11	L	H	H	L	H	L	H	–53
L	L	L	H	H	L	L	–12	L	H	H	L	H	H	L	–54
L	L	L	H	H	L	H	–13	L	H	H	L	H	H	H	–55
L	L	L	H	H	H	L	–14	L	H	H	H	L	L	L	–56
L	L	L	H	H	H	H	–15	L	H	H	H	L	L	H	–57
L	L	H	L	L	L	L	–16	L	H	H	H	L	H	L	–58
L	L	H	L	L	L	H	–17	L	H	H	H	L	H	H	–59
L	L	H	L	L	H	L	–18	L	H	H	H	H	L	L	–60
L	L	H	L	L	H	H	–19	L	H	H	H	H	L	H	–61
L	L	H	L	H	L	L	–20	L	H	H	H	H	H	L	–62
L	L	H	L	H	L	H	–21	L	H	H	H	H	H	H	–63
L	L	H	L	H	H	L	–22	H	L	L	L	L	L	L	–64
L	L	H	L	H	H	H	–23	H	L	L	L	L	L	H	–65
L	L	H	H	L	L	L	–24	H	L	L	L	L	H	L	–66
L	L	H	H	L	L	H	–25	H	L	L	L	L	H	H	–67
L	L	H	H	L	H	L	–26	H	L	L	L	H	L	L	–68
L	L	H	H	L	H	H	–27	H	L	L	L	H	L	H	–69
L	L	H	H	H	L	L	–28	H	L	L	L	H	H	L	–70
L	L	H	H	H	L	H	–29	H	L	L	L	H	H	H	–71
L	L	H	H	H	H	L	–30	H	L	L	H	L	L	L	–72
L	L	H	H	H	H	H	–31	H	L	L	H	L	L	H	–73
L	H	L	L	L	L	L	–32	H	L	L	H	L	H	L	–74
L	H	L	L	L	L	H	–33	H	L	L	H	L	H	H	–75
L	H	L	L	L	H	L	–34	H	L	L	H	H	L	L	–76
L	H	L	L	L	H	H	–35	H	L	L	H	H	L	H	–77
L	H	L	L	H	L	L	–36	H	L	L	H	H	H	L	–78
L	H	L	L	H	L	H	–37	H	L	L	H	H	H	H	–79
L	H	L	L	H	H	L	–38	H	L	H	L	L	L	L	–∞
L	H	L	L	H	H	H	–39	:	:	:	:	:	:	:	–∞
L	H	L	H	L	L	L	–40	:	:	:	:	:	:	:	–∞
L	H	L	H	L	L	H	–41	H	H	H	H	H	H	H	–∞

REC volume

D9, D10, D11	Level
L, L, L	0 dB
L, L, H	–2 dB
L, H, L	–4 dB
L, H, H	–6 dB
H, L, L	–8 dB
H, L, H	–10 dB
H, H, L	–12 dB
H. H. H	–14 dB

A = L, B1 = H, B2 = H, D1 = L

Right channel master volume control

D2	D3	D4	D5	D6	D7	D8	ATT	D2	D3	D4	D5	D6	D7	D8	ATT
L	L	L	L	L	L	L	0	L	H	L	H	L	H	L	–42
L	L	L	L	L	L	H	–1	L	H	L	H	L	H	H	–43
L	L	L	L	L	H	L	–2	L	H	L	H	H	L	L	–44
L	L	L	L	L	H	H	–3	L	H	L	H	H	L	H	–45
L	L	L	L	H	L	L	–4	L	H	L	H	H	H	L	–46
L	L	L	L	H	L	H	–5	L	H	L	H	H	H	H	–47
L	L	L	L	H	H	L	–6	L	H	H	L	L	L	L	–48
L	L	L	L	H	H	H	–7	L	H	H	L	L	L	H	–49
L	L	L	H	L	L	L	–8	L	H	H	L	L	H	L	–50
L	L	L	H	L	L	H	–9	L	H	H	L	L	H	H	–51
L	L	L	H	L	H	L	–10	L	H	H	L	H	L	L	–52
L	L	L	H	L	H	H	–11	L	H	H	L	H	L	H	–53
L	L	L	H	H	L	L	–12	L	H	H	L	H	H	L	–54
L	L	L	H	H	L	H	–13	L	H	H	L	H	H	H	–55
L	L	L	H	H	H	L	–14	L	H	H	H	L	L	L	–56
L	L	L	H	H	H	H	–15	L	H	H	H	L	L	H	–57
L	L	H	L	L	L	L	–16	L	H	H	H	L	H	L	–58
L	L	H	L	L	L	H	–17	L	H	H	H	L	H	H	–59
L	L	H	L	L	H	L	–18	L	H	H	H	H	L	L	–60
L	L	H	L	L	H	H	–19	L	H	H	H	H	L	H	–61
L	L	H	L	H	L	L	–20	L	H	H	H	H	H	L	–62
L	L	H	L	H	L	H	–21	L	H	H	H	H	H	H	–63
L	L	H	L	H	H	L	–22	H	L	L	L	L	L	L	–64
L	L	H	L	H	H	H	–23	H	L	L	L	L	L	H	–65
L	L	H	H	L	L	L	–24	H	L	L	L	L	H	L	–66
L	L	H	H	L	L	H	–25	H	L	L	L	L	H	H	–67
L	L	H	H	L	H	L	–26	H	L	L	L	H	L	L	–68
L	L	H	H	L	H	H	–27	H	L	L	L	H	L	H	–69
L	L	H	H	H	L	L	–28	H	L	L	L	H	H	L	–70
L	L	H	H	H	L	H	–29	H	L	L	L	H	H	H	–71
L	L	H	H	H	H	L	–30	H	L	L	H	L	L	L	–72
L	L	H	H	H	H	H	–31	H	L	L	H	L	L	H	–73
L	H	L	L	L	L	L	–32	H	L	L	H	L	H	L	–74
L	H	L	L	L	L	H	–33	H	L	L	H	L	H	H	–75
L	H	L	L	L	H	L	–34	H	L	L	H	H	L	L	–76
L	H	L	L	L	H	H	–35	H	L	L	H	H	L	H	–77
L	H	L	L	H	L	L	–36	H	L	L	H	H	H	L	–78
L	H	L	L	H	L	H	–37	H	L	L	H	H	H	H	–79
L	H	L	L	H	H	L	–38	H	L	H	L	L	L	L	–∞
L	H	L	L	H	H	H	–39	:	:	:	:	:	:	:	–∞
L	H	L	H	L	L	L	–40	:	:	:	:	:	:	:	–∞
L	H	L	H	L	L	H	–41	H	H	H	H	H	H	H	–∞

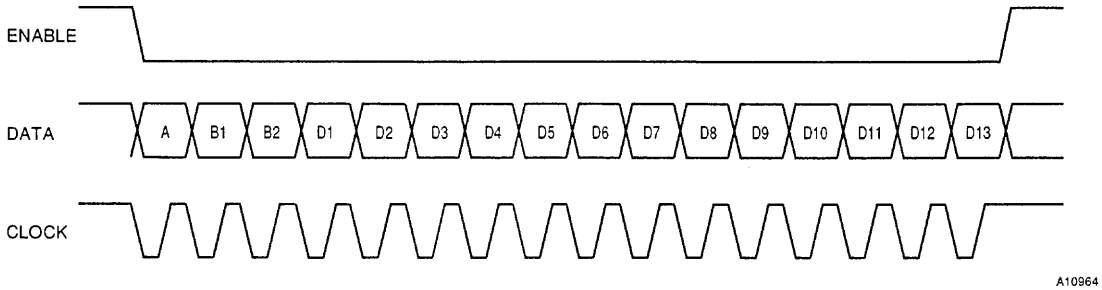
REC OUT input switching

	L	H
D9	Function output	Mixer output

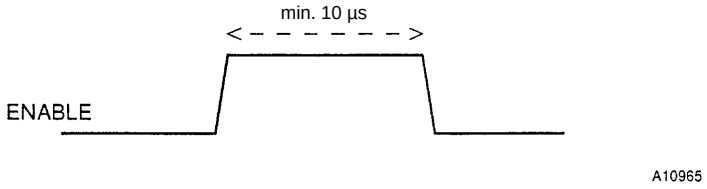
REC OUT on/off

	L	H
D10	OFF	ON
D11	OFF	ON

Notes on control data



- The device latches the individual data bits of the command at the rising edge of the clock signal.
- One frame consists of 16 bits (A to D13).
- The device latches the data for the command at the rising edge of the enable signal.
- Maintain the clock and enable signals at High level when not controlling the LV1110NM.
- Maintain the enable signal at High level for at least 10 µs between commands.

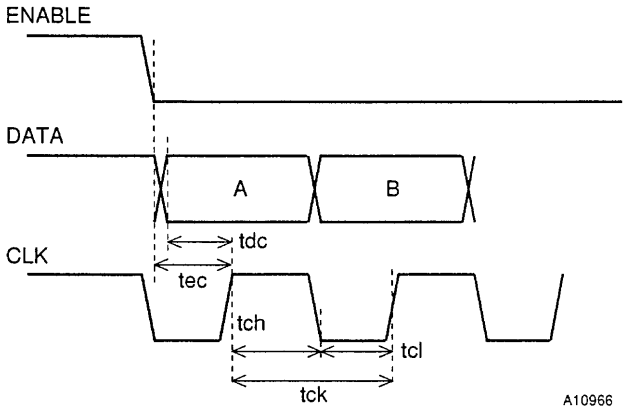


Important note on mode control and using system muting

- When the power is first applied, allow the IC sufficient time to initialize (approximately 2 seconds) and then send it commands to turn system muting off and then on.
- When changing the delay, always turn system muting on and then off—that is, send the new data with the command to turn system muting on and again with the command to turn it back off.

  Both operations enhance reliability by forcing the device to initialize its memory.

Data timing



Timing Characteristic

Parameter	Symbol	Ratings			Unit
		min	typ	max	
Enable-to-clock delay	tec	5			µs
Data-to-clock delay	tdc	5			µs
Clock high-level hold time	tch	5			µs
Clock high-level hold time	tcl	5			µs
Clock period	tck	10			µs

Control Commands

A = L, B1 = L, B2 = L

- D1, D2, and D3: Function input switching. In CD and MD modes an output buffer is used, but the 6-dB amplifier output is used for tape, tuner, and EXT modes. The input impedance is 50 kΩ.
- D4, D5, and D6: Matrix mode switching and total through switching. The signal selected by the matrix is mixed to the left and right channels according to D10 and used to form the surround signal according to the D11 and D12 delay signal selection bits. In total through mode, the left and right signals are directly output with the matrix and graphic equalizer blocks bypassed to provide a high signal-to-noise ratio output.
- D7: Audio rejection on/off. When this bit is set to 1, L+R mode must be selected with D4, D5, and D6.
- D8: Microphone mixing on/off.
- D9: Key control interface on/off. The signal (BGM) set up by the matrix block is output from pin 6 and the signal processed by key control is mixed into the left and right channels by inputting it to pin 7.
- D10: Left and right channel bypass/matrix switching. When matrix is selected, monaural and karaoke multi-sound software L/R only modes can be set up.
- D11: Surround signal I/O (input: pin 32, output: pin 33) on/off.
- D12 and D13: Delay line signal input switching. When SW = B, the signal processed by key control can be input to the delay line.

A = L, B1 = H, B2 = L

- D1 and D2: Delay line output filter switching: A 5-kHz or higher low-pass filter cutoff frequency is recommended for delay times of 15 to 50 ms, and a 2-kHz low-pass filter for 100 and 120 ms delay times.
- D3, D4, and D5: Reverb volume switching. Since oscillation may occur at the 0 dB setting, always use a setting of -1 dB or lower.
- D6, D7, and D8: Delay time setting.
- D9: System muting on/off. Always use the system muting function (D9) when changing the delay time. Turning the muting function on and the off again initializes memory and prevents incorrect operation.
- D10: Left and right channel output (pins 20 and 21) muting on/off.
- D11: Front mix right channel phase switching. Selects whether the delayed signal is added into the right channel in phase or out of phase relative to the left channel.
- D12 and D13: Front mix level switching.

A = L, B1 = L, B2 = H

- D1, D2, and D3: Graphic equalizer bass boost/cut level setting.
- D4, D5, and D6: Graphic equalizer mid boost/cut level setting.
- D7, D8, and D9: Graphic equalizer treble boost/cut level setting.
- D10 and D11: Port output high/low level settings. When set to high, the corresponding port pin is pulled up to VDD through a 51-kΩ resistor, and when set to low, the pin is pulled down with an npn transistor (about 1 kΩ).

A = L, B1 = H, B2 = H, D1 = L

- D2, D3, D4, D5, D6, D7, and D8: Left channel master volume setting.
- D9, D10, and D11: Record volume setting.

A = L, B1 = H, B2 = H, D1 = H

- D2, D3, D4, D5, D6, D7, and D8: Right channel master volume setting.
- D9: Record output signal switching. Selects function output or mixer output.
- D10 and D11: Record output on/off (muting). D10 controls the pin 2 and pin 52 outputs and D11 controls the pin 3 and 53 outputs.

Control Command Examples

The LV1110M provides the following functions required in digital surround systems: matrix, delay line, reverb volume, front mix (level and phase switching), and a graphic equalizer. It also provides microphone echo, a key control interface, vocal track removal, and multi-sound software support functions and associated settings as karaoke functions. The tables present examples of commands that control these functions.

MODE 1

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
BYPASS1	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	H	L	H	L	L	L	L	L	L	L
	L	H	L	H	L	L	L	L	L	L	L	H	H	L	L	L

Total Through

MODE 2

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
BYPASS2	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L
	L	H	L	H	L	L	L	L	L	L	L	H	H	L	L	L

Matrix Through

MODE 3

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
STADIUM1	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	H	L	L	L	L	L	L	H	L	H
	L	H	L	H	L	L	H	H	H	L	H	H	H	H	L	H

L + R Delay 50 ms, Reverb –5 dB, Front add –5 dB: Inverted phase, 5 kHz LPF

MODE 4

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
HALL	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	H
	L	H	L	H	L	L	H	H	L	H	L	H	H	H	L	H

L + R Delay 50 ms, Reverb –5 dB, Front add –5 dB: Inverted phase, 5 kHz LPF

MODE 5

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
STAGE	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	H	L	L	L	L	H	L	H
	L	H	L	H	L	L	H	H	H	L	L	H	H	H	H	L

L – R Delay 40 ms, Reverb –5 dB, Front add –3 dB: Inverted phase, 5 kHz LPF

MODE 6

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
DISCO	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	H	L	L	L	L	H	L	H
	L	H	L	H	L	L	H	H	L	H	L	H	H	H	H	L

L – R Delay 25 ms, Reverb –5 dB, Front add –3 dB: Inverted phase, 5 kHz LPF

MODE 7

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
LIVE	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	H
	L	H	L	H	L	L	L	L	L	H	L	H	H	H	H	L

L – R Delay 25 ms, Reverb off, Front add –3 dB: Inverted phase, 5 kHz LPF

MODE 8

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
MIC ECHO	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	L	L	H	L	L	L	L	L
	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H

MIC Mix: Echo, Delay 100 ms, Reverb –1 dB, Front add +3 dB: 2 kHz LPF

MODE 9

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
MIC ECHO Vocal canceler	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	L	H	H	L	H	L	L	L
	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H

MIC Mix: Echo, Vocal Cancel, Delay 100 ms, Reverb –1 dB, Front add +3 dB: 2 kHz LPF

MODE 10

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
MIC ECHO With the key control interface enabled	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	L	L	L	H	L	L	L	L	L
	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H

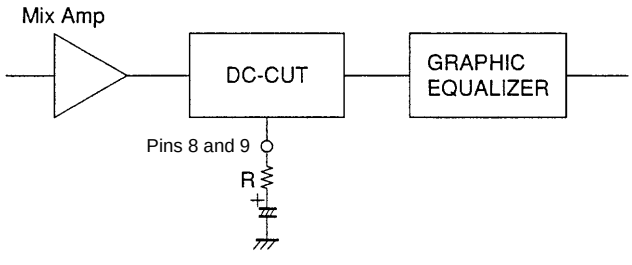
MIC Mix: Echo, Key Control Interface On, Delay 100 ms, Reverb –1 dB, Front add +3 dB: 2 kHz LPF

MODE11

	A	B1	B2	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13
MIC ECHO Multi-sound software Left channel only	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	L	L	L	H	L	H	L	L	H	L	H	L	L	L
	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H

MIC Mix: Echo, Lch Only, Delay 100 ms, Reverb –1 dB, Front add +3 dB: 2 kHz LPF

Graphic equalizer level attenuation technique

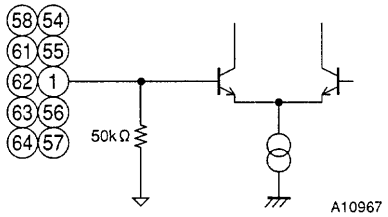
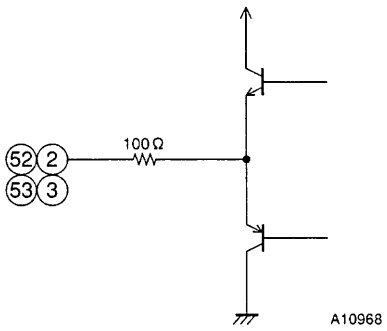
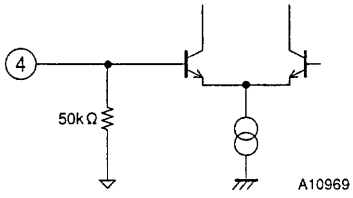


- Since the graphic equalizer provides a maximum boost of 10 dB, the head room is insufficient when this boost is used. Therefore, the signal level must be attenuated in the graphic equalizer block. One technique for providing this attenuation is to connect resistors in series with the external capacitors connected at pins 8 and 9 in the DC cut circuit. The formula below can be used to determine the amount of attenuation due to the value of the resistor.

  Attenuation: $V_G = 20 \times \log (1 - R/10\ K + R)$ dB

  Example: If R = 10 kΩ, the attenuation will be –6 dB.

Pin Functions

Pin No.	Pin Name	Pin voltage	Equivalent circuit	Description
1 54 55 56 57 58 61 62 63 64	EXT.R.IN CD.L.IN TAPE.L.IN TUNER.L.IN MD.L.IN EXT.L.IN CD.R.IN TAPE.R.IN TUNER.R.IN MD.R.IN	1/2 V_{CC}	• Function input pins. A TAPE, TUNER, or EXT inputs passes through an internal 6-dB amplifier; a CD or MD input, through a buffer amplifier.	
2 3 52 53	REC.R.OUT1 REC.R.OUT2 REC.L.OUT1 REC.L.OUT2	1/2 V_{CC}	• Recording output pins.	
4	MIC.IN	1/2 V_{CC}	• Microphone mixer and echo input pin.	

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Pin No.	Pin Name	Pin voltage	Equivalent circuit	Description
5	VM.C	1/2 V_{CC}		• Pin for connecting phase shifter capacitor for karaoke functions and voice canceler.
6	KEY/DELAY.OUT	1/2 V_{CC}		• Output pin for key control BGM output or delay signal.
7	KEY.IN	1/2 V_{CC}		• Key control processing signal input pin.
8 9 34	DC-CUT.R DC-CUT.L DC-CUT	1/2 V_{CC}		• Pins for connecting capacitors for DC-CUT function. The capacitances determine the low pass filter cutoff frequencies.
10 25	HIGH.R HIGH.L	1/2 V_{CC}		• Pins for connecting TREBLE capacitors.

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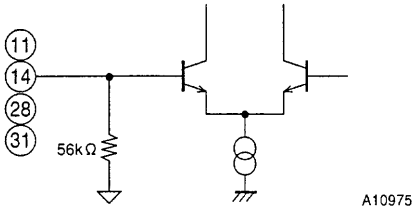
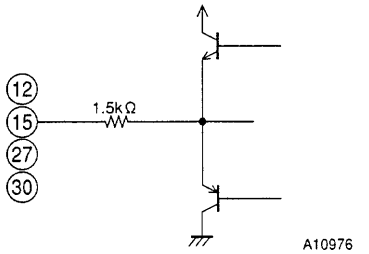
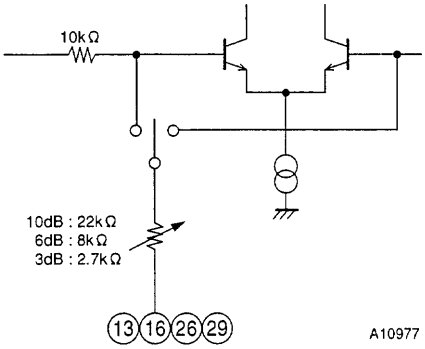
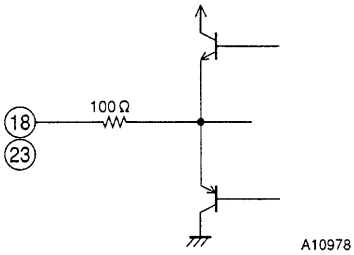
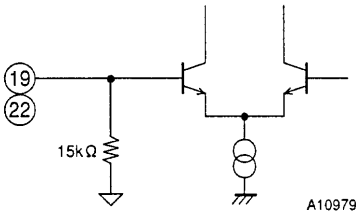
Pin No.	Pin Name	Pin voltage	Equivalent circuit	Description
11 14 28 31	MID.RI LOW.RI MID.LI LOW.LI	1/2 V_{CC}	• Semiconductor inductance buffer amplifier input pins.	
12 15 27 30	MID.RO LOW.RO MID.LO LOW.LO	1/2 V_{CC}	• Semiconductor inductance buffer amplifier output pins.	
13 16 26 29	MID.R LOW.R MID.L LOW.L	1/2 V_{CC}	• Pins for connecting BASS/MID semiconductor inductances.	
18 23	VOL.R.OUT VOL.L.OUT	1/2 V_{CC}	• Master volume control output pins.	
19 22	VOL.R.IN VOL.L.IN	1/2 V_{CC}	• Master volume control input pins.	

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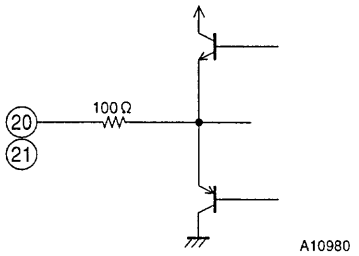
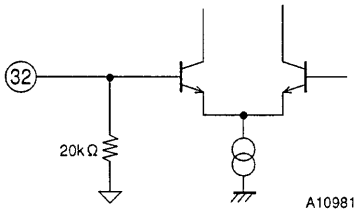
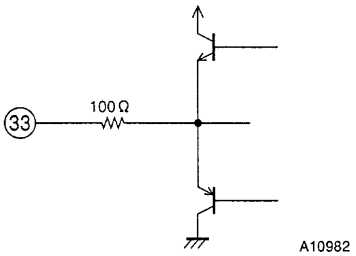
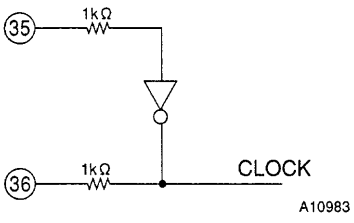
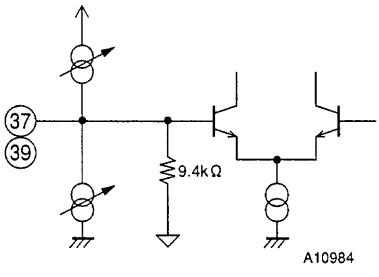
Pin No.	Pin Name	Pin voltage	Equivalent circuit	Description
20 21	OUT.R OUT.L	1/2 V_{CC}	• LINE OUT pins.	
32	S-IN	1/2 V_{CC}	• Surround signal input pin.	
33	S-OUT	1/2 V_{CC}	• Delay processing surround signal output pin.	
35 36	OSC1 OSC2	0/5 V	• Pins for connecting 8-MHz oscillator.	
37 39	D/A A/D	1/2 V_{CC}	• Pins for connecting variable integrator capacitors.	

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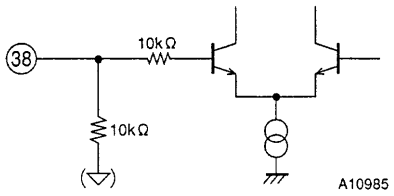
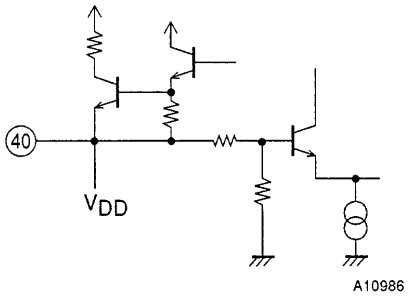
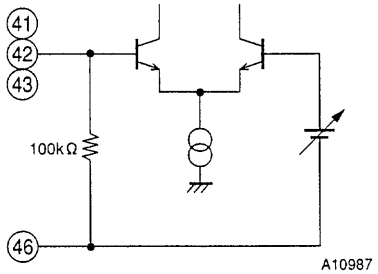
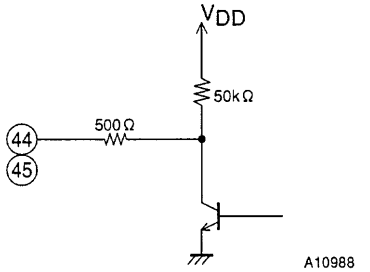
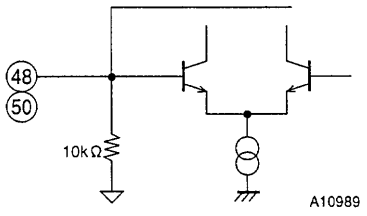
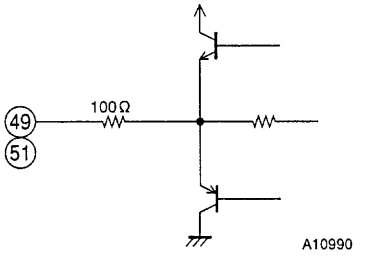
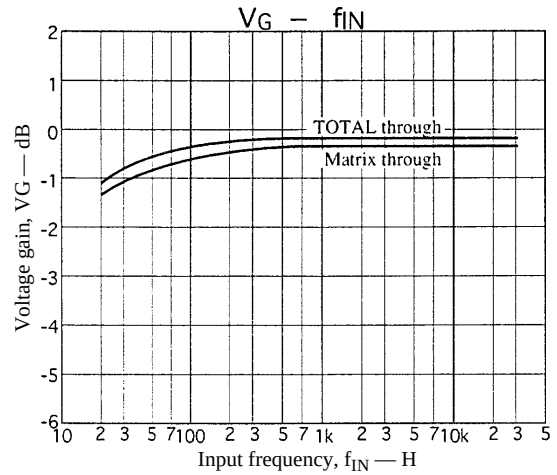
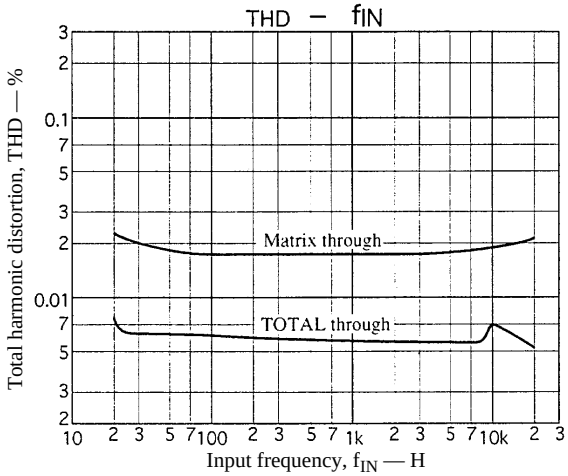
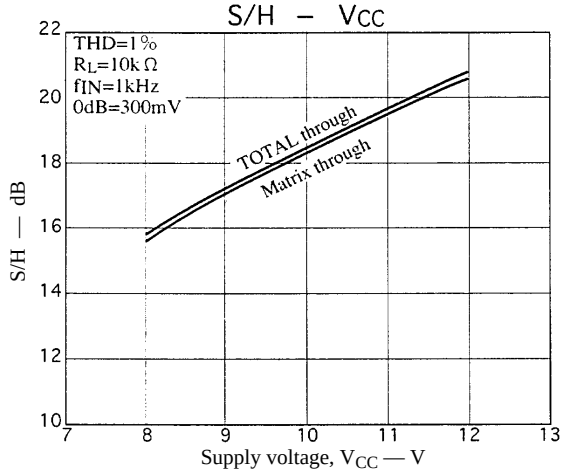
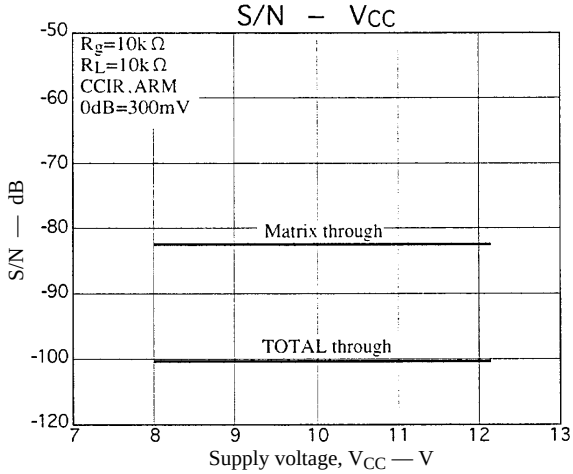
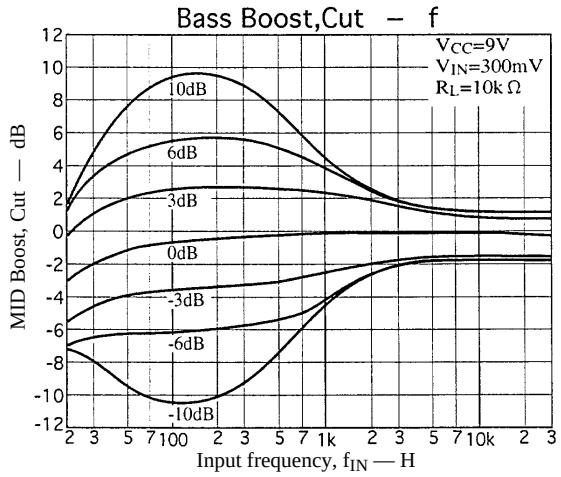
Pin No.	Pin Name	Pin voltage	Equivalent circuit	Description
38	N.S	1/2 V_{CC}	• Pins for connecting noise shaper capacitor.	
40	V_{DD}	5 V	• V_{DD} output from internal power supply.	
41 42 43 46	ENABLE DATA CLOCK SHUMIT.REF	0/5 V	• Serial control data input pins. Connect pin 46 to the Low level for the input data.	
44 45	O.PORT2 O.PORT1	0/5 V	• Output port pins. 1-mA current at Low level. Sink pin voltage: approximately 1 V.	
48 50	IN.L IN.R	1/2 V_{CC}	• LINE IN pins.	
49 51	FUNCTION.L OUT FUNCTION.R OUT	1/2 V_{CC}		

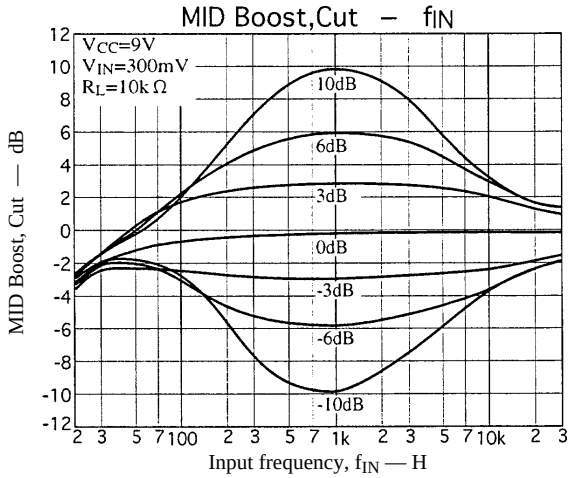

VG – fIN
Voltage gain, VG — dB
TOTAL through
Matrix through
Input frequency, fIN — H

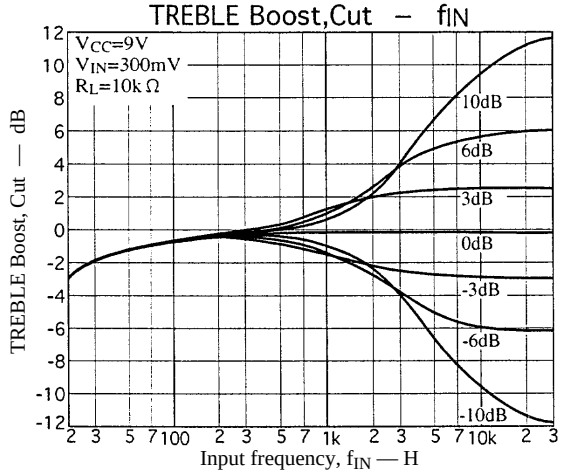

THD – fIN
Total harmonic distortion, THD — %
Matrix through
TOTAL through
Input frequency, fIN — H


S/H – VCC
THD=1%
RL=10kΩ
fIN=1kHz
0dB=300mV
TOTAL through
Matrix through
S/H — dB
Supply voltage, VCC — V


S/N – VCC
Rg=10kΩ
RL=10kΩ
CCIR.ARM
0dB=300mV
Matrix through
TOTAL through
S/N — dB
Supply voltage, VCC — V


Bass Boost,Cut – f
VCC=9V
VIN=300mV
RL=10kΩ
10dB
6dB
3dB
0dB
-3dB
-6dB
-10dB
MID Boost, Cut — dB
Input frequency, fIN — H


MID Boost,Cut – fIN
VCC=9V
VIN=300mV
RL=10kΩ
10dB
6dB
3dB
0dB
-3dB
-6dB
-10dB
MID Boost, Cut — dB
Input frequency, fIN — H


TREBLE Boost,Cut – fIN
VCC=9V
VIN=300mV
RL=10kΩ
10dB
6dB
3dB
0dB
-3dB
-6dB
-10dB
TREBLE Boost, Cut — dB
Input frequency, fIN — H

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