Ordering number : EN6108

CMOS IC

LC75397E

Single Chip Electronic Volume and Tone Control System

Overview

The LC75397 is an electronic volume control system providing control over volume, balance, 4-band equalizer, bass, and input switching based on serial inputs.

Functions

- Volume control:
  The chip provides 81 levels of volume attenuation: in 1-dB step between 0 dB and –79 dB and –∞.
  This circuit can control a total of 5 independent channels.
- Equalizer:
  The chip provides control in 2-dB steps over the range between +10 dB and –10 dB. Three of the four bands have peaking equalization; the remaining one, shelving equalization.
- Selector:
  The left and right channels each offer a choice of six inputs. The L6 and R6 inputs can be turned on and off independently. An external constant determines the amplification for the input signal.
- Input gain:
  The input signal can be amplified by 0 to +30 dB in 2-dB steps.
- Bass control:
  The bass can be controlled over a ±10 dB range in 2-dB steps.

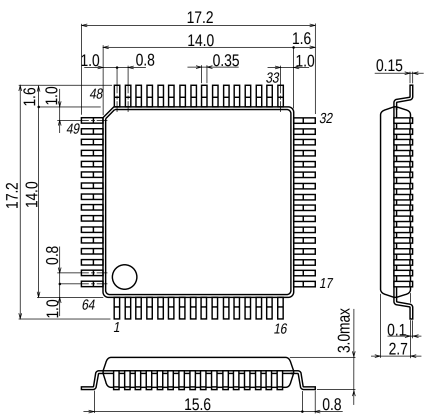
Features

- Built-in buffer amplifiers reduce the number of external parts required.
- Silicon gate CMOS process reduces the noise of built-in switch.
- Built-in analog ground reference voltage generator circuit
- All functions are controlled by serial input data. This IC supports the CCB standard.

Package Dimensions

unit: mm

3159-QFP64E



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	CL, DI, CE, L1 to L6, R1 to R6, LTIN, RTIN, LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C, with PC board*	1000	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Note : * Printed circuit board size: 76.1 × 114.3 × 1.6 mm, printed circuit board material: glass/Epoxy resin

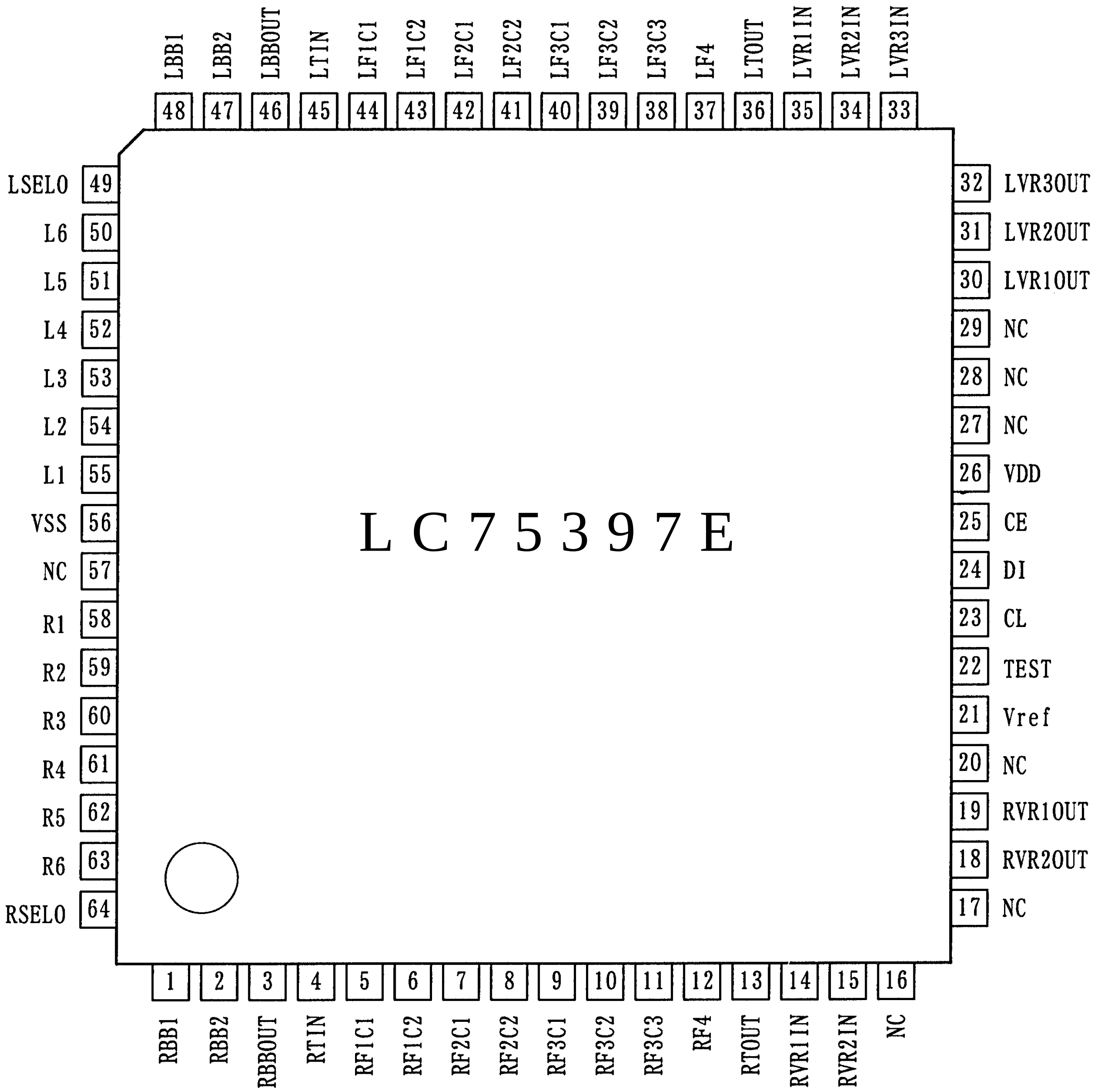
Allowable Operating Ranges at Ta = – 30 to + 75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	6.0		10.5	V
Input high level voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Input low level voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, L1 to L6, R1 to R6, LTIN, RTIN, LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN	V_{SS}		V_{DD}	Vp-p
Input pulse width	$t_{øW}$	CL	1.0			µs
Setup time	t_{SETUP}	CL, DI, CE	1.0			µs
Hold time	t_{HOLD}	CL, DI, CE	1.0			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 10 V, V_{SS} = 0 V

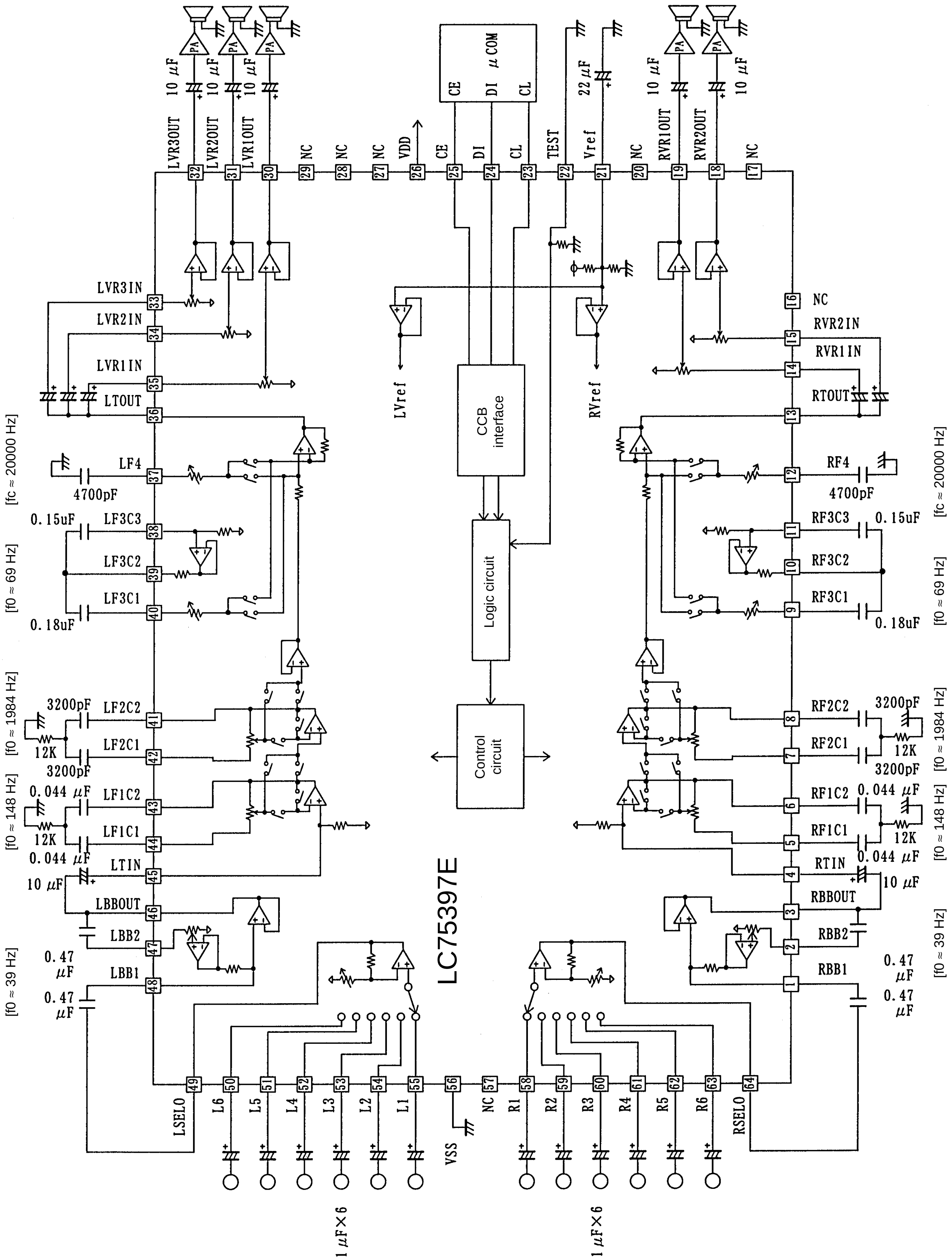
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Input block]						
Input resistance	Rin	L1 to L6, R1 to R6		50		kΩ
Clipping level	Vcl	LSELO, RSELO: THD = 1.0%		3.00		Vrms
Output load resistance	R_L	LSELO, RSELO	10			kΩ
[Volume control block]						
Input resistance	Rin	LVR1IN, RVR1IN, LVR2IN, RVR2IN, LVR3IN		50		kΩ
[Bass control block]						
Control range	Geq	Max, boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistance	Rbb1			1.3		kΩ
	Rbb2			58		
[F1/F2 band equalizer control block]						
Control range	Geq	Max. boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistor	Rfeed		31	51.8	73	kΩ
[F3/F4 band equalizer control block]						
Control range	Geq	Max. boost/cut	±8	±10	±12	dB
Step resolution	Estep		1	2	3	dB
Internal feedback resistor	Rfeed		17	28	39	kΩ
[Overall characteristics]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall			0.01	%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, with all controls flat overall, Rg = 1 kΩ	80			dB
Output noise voltage	V_N 1	With all controls flat overall, 80 kHz, L.P.F		10.2		µV
	V_N 2	Bass band = +10dB, With all controls overall, 80 kHz, L.P.F		10.6		µV
Output at maximum attenuation	V_O min	With all controls flat overall		–90		dB
Current drain	I_{DD}	V_{DD} – V_{SS} = 10.5 V		58		mA
Input high level current	I_{IH}	CL, DI, CE, V_{IN} = 10.5 V			10	µA
Input low level current	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			µA

Pin Assignment



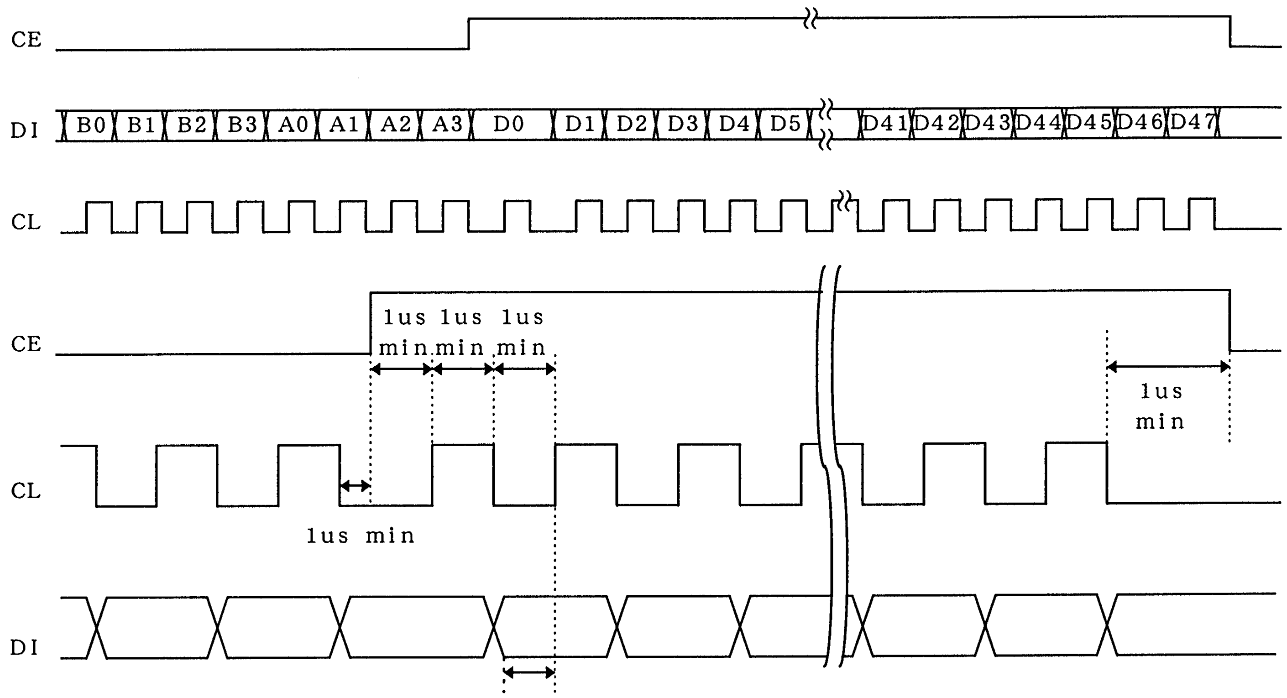
Top view

Sample Application Circuit



Control System Timing and Data Formats

To control the LC75397E, specified sequences are required to be input through the pins CE, CL, and DI. Each sequence consists of 48 bits: an 8-bit address followed by 56 bits of data.



1us ≤ T DEST

1. Address Code (B0 to A3)

   This product uses an 8-bit address code, and supports the same specifications as other Sanyo CCB serial bus products.

   Address code (LSB)

B0	B1	B2	B3	A0	A1	A2	A3
0	1	0	0	0	0	0	1

   (82HEX)

2. Control Code Allocations

   Input switching control (L1, L2, L3, L4, L5, R1, R2, R3, R4, R5)

D0	D1	D2	Operation
0	0	0	L1 (R1) ON
1	0	0	L2 (R2) ON
0	1	0	L3 (R3) ON
1	1	0	L4 (R4) ON
0	0	1	L5 (R5) OFF
1	0	1	Switch all OFF
0	1	1	Switch all OFF
1	1	1	Switch all OFF

   Input switching control (L6, R6)

D3	Operation
1	L6 (R6) OFF
0	L6 (R6) ON

Input gain control

D4	D5	D6	D7	Operation
0	0	0	0	0 dB
1	0	0	0	+2 dB
0	1	0	0	+4 dB
1	1	0	0	+6 dB
0	0	1	0	+8 dB
1	0	1	0	+10 dB
0	1	1	0	+12 dB
1	1	1	0	+14 dB
0	0	0	1	+16 dB
1	0	0	1	+18 dB
0	1	0	1	+20 dB
1	1	0	1	+22 dB
0	0	1	1	+24 dB
1	0	1	1	+26 dB
0	1	1	1	+28 dB
1	1	1	1	+30 dB

Bass and 4-band equalizer control

D8	D9	D10	D11	Bus
D12	D13	D14	D15	f1 band
D16	D17	D18	D19	f2 band
D20	D21	D22	D23	f3 band
D24	D25	D26	D27	f4 band
1	0	1	0	+10 dB
0	0	1	0	+8 dB
1	1	0	0	+6 dB
0	1	0	0	+4 dB
1	0	0	0	+2 dB
0	0	0	0	0 dB
1	0	0	1	–2 dB
0	1	0	1	–4 dB
1	1	0	1	–6 dB
0	0	1	1	–8 dB
1	0	1	1	–10 dB

Volume control

D28	D29	D30	D31	D32	D33	D34	D35	Operation
0	0	0	0	0	0	0	0	0 dB
1	0	0	0	0	0	0	0	–1 dB
0	1	0	0	0	0	0	0	–2 dB
1	1	0	0	0	0	0	0	–3 dB
0	0	1	0	0	0	0	0	–4 dB
1	0	1	0	0	0	0	0	–5 dB
0	1	1	0	0	0	0	0	–6 dB
1	1	1	0	0	0	0	0	–7 dB
0	0	0	1	0	0	0	0	–8 dB
1	0	0	1	0	0	0	0	–9 dB
0	1	0	1	0	0	0	0	–10 dB
1	1	0	1	0	0	0	0	–11 dB
0	0	1	1	0	0	0	0	–12 dB
1	0	1	1	0	0	0	0	–13 dB
0	1	1	1	0	0	0	0	–14 dB
1	1	1	1	0	0	0	0	–15 dB
0	0	0	0	1	0	0	0	–16 dB
1	0	0	0	1	0	0	0	–17 dB
0	1	0	0	1	0	0	0	–18 dB
1	1	0	0	1	0	0	0	–19 dB
0	0	1	0	1	0	0	0	–20 dB
1	0	1	0	1	0	0	0	–21 dB
0	1	1	0	1	0	0	0	–22 dB
1	1	1	0	1	0	0	0	–23 dB
0	0	0	1	1	0	0	0	–24 dB
1	0	0	1	1	0	0	0	–25 dB
0	1	0	1	1	0	0	0	–26 dB
1	1	0	1	1	0	0	0	–27 dB
0	0	1	1	1	0	0	0	–28 dB
1	0	1	1	1	0	0	0	–29 dB
0	1	1	1	1	0	0	0	–30 dB
1	1	1	1	1	0	0	0	–31 dB
0	0	0	0	0	1	0	0	–32 dB
1	0	0	0	0	1	0	0	–33 dB
0	1	0	0	0	1	0	0	–34 dB
1	1	0	0	0	1	0	0	–35 dB
0	0	1	0	0	1	0	0	–36 dB
1	0	1	0	0	1	0	0	–37 dB
0	1	1	0	0	1	0	0	–38 dB
1	1	1	0	0	1	0	0	–39 dB
0	0	0	1	0	1	0	0	–40 dB
1	0	0	1	0	1	0	0	–41 dB
0	1	0	1	0	1	0	0	–42 dB
1	1	0	1	0	1	0	0	–43 dB
0	0	1	1	0	1	0	0	–44 dB
1	0	1	1	0	1	0	0	–45 dB
0	1	1	1	0	1	0	0	–46 dB
1	1	1	1	0	1	0	0	–47 dB
0	0	0	0	1	1	0	0	–48 dB
1	0	0	0	1	1	0	0	–49 dB
0	1	0	0	1	1	0	0	–50 dB

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D28	D29	D30	D31	D32	D33	D34	D35	Operation
1	1	0	0	1	1	0	0	–51 dB
0	0	1	0	1	1	0	0	–52 dB
1	0	1	0	1	1	0	0	–53 dB
0	1	1	0	1	1	0	0	–54 dB
1	1	1	0	1	1	0	0	–55 dB
0	0	0	1	1	1	0	0	–56 dB
1	0	0	1	1	1	0	0	–57 dB
0	1	0	1	1	1	0	0	–58 dB
1	1	0	1	1	1	0	0	–59 dB
0	0	1	1	1	1	0	0	–60 dB
1	0	1	1	1	1	0	0	–61 dB
0	1	1	1	1	1	0	0	–62 dB
1	1	1	1	1	1	0	0	–63 dB
0	0	0	0	0	0	1	0	–64 dB
1	0	0	0	0	0	1	0	–65 dB
0	1	0	0	0	0	1	0	–66 dB
1	1	0	0	0	0	1	0	–67 dB
0	0	1	0	0	0	1	0	–68 dB
1	0	1	0	0	0	1	0	–69 dB
0	1	1	0	0	0	1	0	–70 dB
1	1	1	0	0	0	1	0	–71 dB
0	0	0	1	0	0	1	0	–72 dB
1	0	0	1	0	0	1	0	–73 dB
0	1	0	1	0	0	1	0	–74 dB
1	1	0	1	0	0	1	0	–75 dB
0	0	1	1	0	0	1	0	–76 dB
1	0	1	1	0	0	1	0	–77 dB
0	1	1	1	0	0	1	0	–78 dB
1	1	1	1	0	0	1	0	–79 dB
0	0	0	0	1	0	1	0	–∞

Channel selection control

D36	D37	Operation
0	0	Initial setting
1	0	Righ channel
0	1	Left channel
1	1	Simulataneous left and right

Volume 1 control

D38	Operation
0	Control off
1	Control enabled

Right channel control is enabled when D36 is set to 1.
Left channel control is enabled when D37 is set to 1.

Volume 2 control

D39	Operation
0	Control off
1	Control enabled

Right channel control is enabled when D36 is set to 1.
Left channel control is enabled when D37 is set to 1.

Volume 3 control

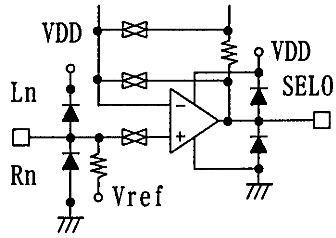
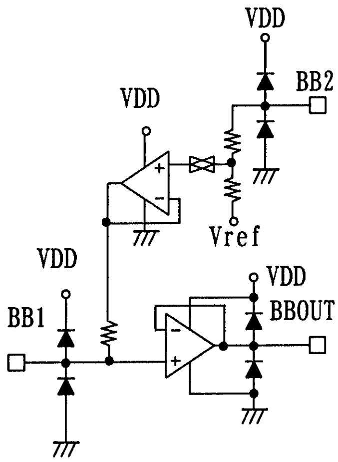
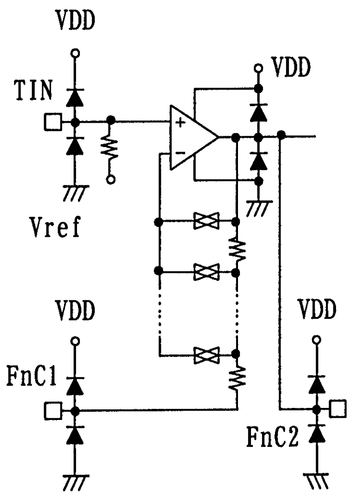
D40	Operation
0	Control off
1	Control enabled

Control of this function is enabled when D37 is set to 1.

Test mode control

D41	D42	D43	D44	D45	D46	D47
0	0	0	0	0	0	0
These bits are for chip testing and must all be set to 0 in application systems.						

Pin Functions

Pin No.	Pin	Function	Equivalent circuit
55 54 53 52 51 50 58 59 60 61 62 63	L1 L2 L3 L4 L5 L6 R1 R2 R3 R4 R5 R6	Signal inputs	
49 64	LSELO RSELO	Input selector outputs	
48 47 1 2 46 3	LBB1 LBB2 RBB1 RBB2 LBBOUT RBBOUT	Bass circuit inputs and outputs	
45 4	LTIN RTIN	Equalizer inputs	
44 43 5 6	LF1C1 LF1C2 RF1C1 RF1C2	Connections for the resistors and capacitors that form the F1 band equalizer.	
42 41 7 8	LF2C1 LF2C2 RF2C1 RF2C2	Connections for the resistors and capacitors that form the F2 band equalizer.	

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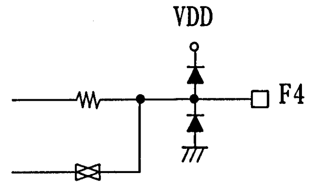
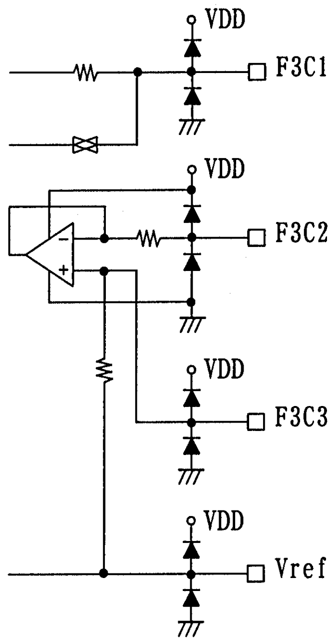
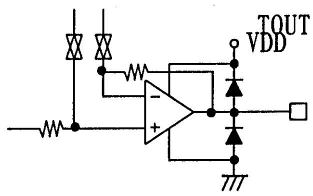
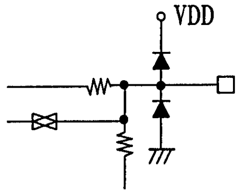
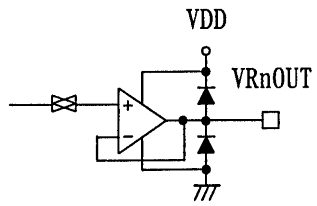
Pin No.	Pin	Function	Equivalent circuit
37 12	LF4 RF4	Connections for the capacitors that form the equqlizer F4 band filters Connections for external capacitors	
40 39 38 9 10 11	LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	Connections for the resistors and capacitors that form the F3 band equalizer.	
36 13	LTOUT RTOUT	Connections for the resistors and capacitors that form the F3 band equalizer.	
35 34 33 14 15	LVR1IN LVR2IN LVR3IN RVR1IN RVR2IN	• Left channel volume input 1 • Left channel volume input 2 • Left channel volume input 3 • Right channel volume input 1 • Right channel volume input 2	
32 31 30 18 19	LVR3OUT LVR2OUT LVR1OUT RVR2OUT RVR1OUT	• Left channel volume output 3 • Left channel volume output 2 • Left channel volume output 1 • Right channel volume output 2 • Right channel volume output 1	

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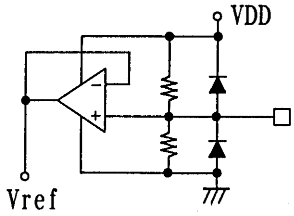
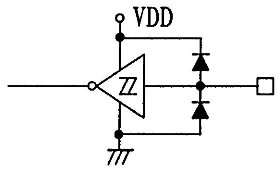
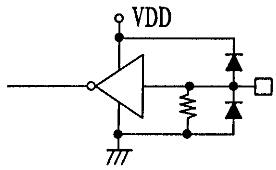
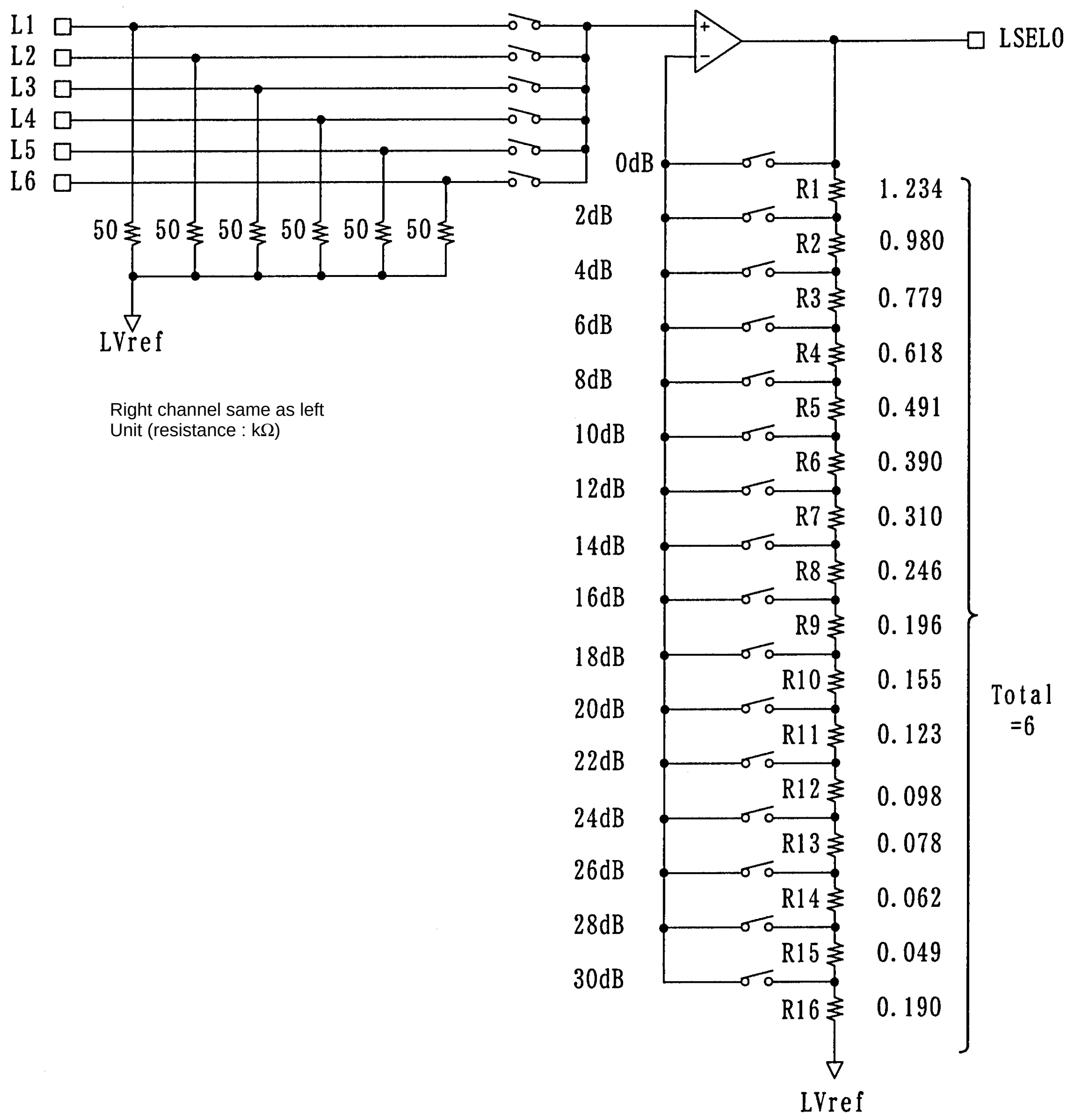
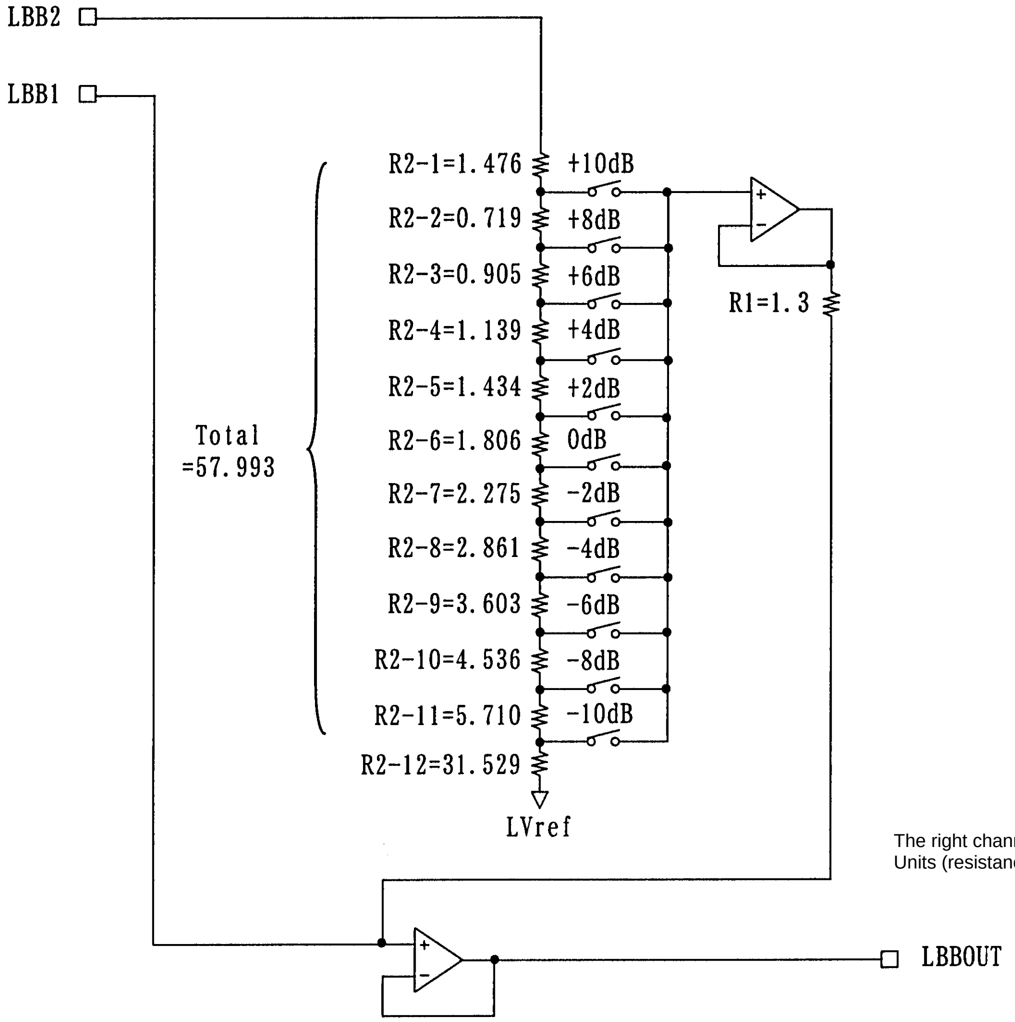
Pin No.	Pin	Function	Equivalent circuit
21	Vref	• A capacitor with a value of a few tens of µF must be inserted between Vref and AV_{SS} (V_{SS}) to reduce power supply ripple in the 0.5 × V_{DD} voltage generator block used for analog ground.	
56	V_{SS}	Ground	
26	V_{DD}	Power supply	
25	CE	• Chip enable When this pin goes from high to low, data is written to an internal latch and the analog switches operate. Data transfers are enables when this pin is at the high level.	
24 23	DI CL	• Serial data and clock inputs for chip control	
22	TEST	• Electronic volume control test pin. This pin must be held at the V_{SS} potential.	
16 17 20 27 28 29 57	NC	• Unused pins. These pins must either be left open or connected to V_{SS}.	

Equivalent Circuit Diagram

(1) Selector Control Block

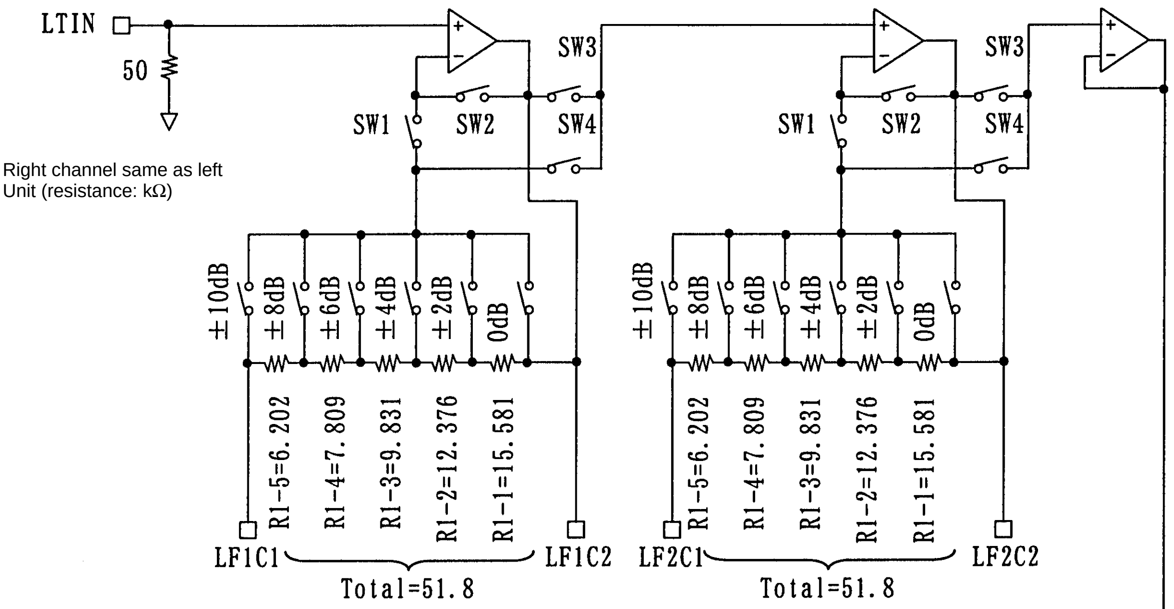


(2) Bass control block internal equivalent circuit



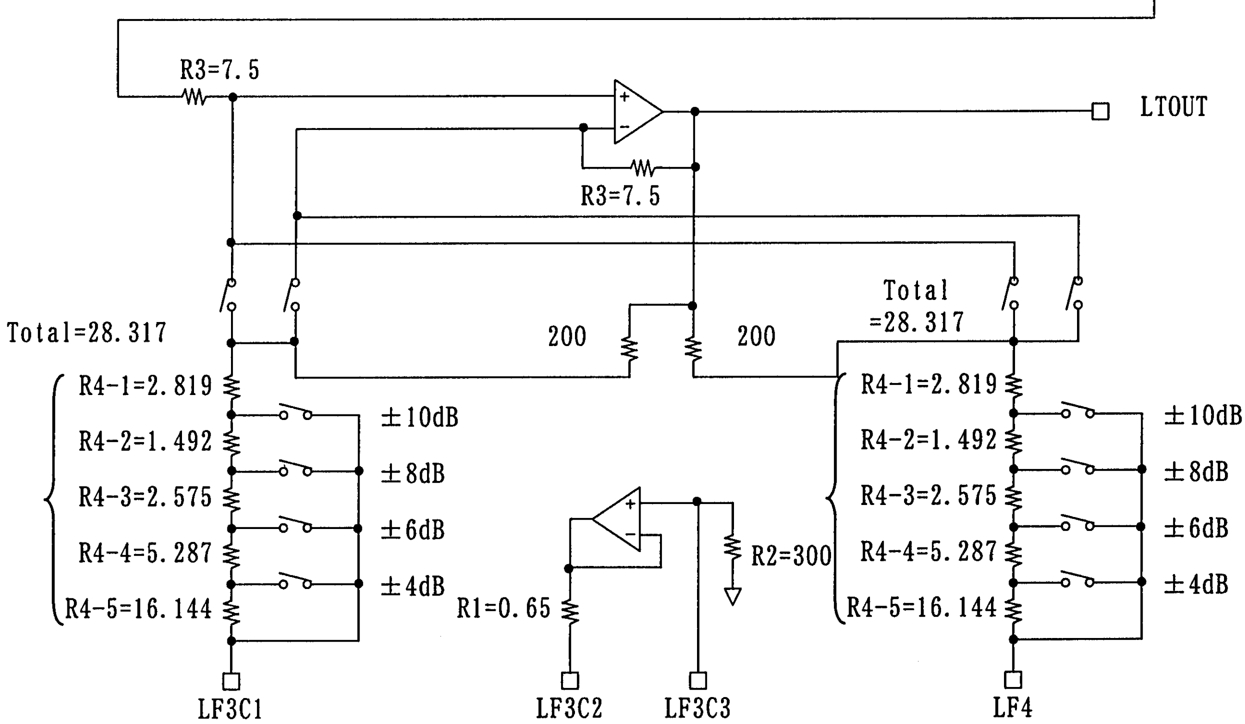
The right channel is identical.
Units (resistance: kΩ)

(3) F1/F2 band equalizer block internal equivalent circuit



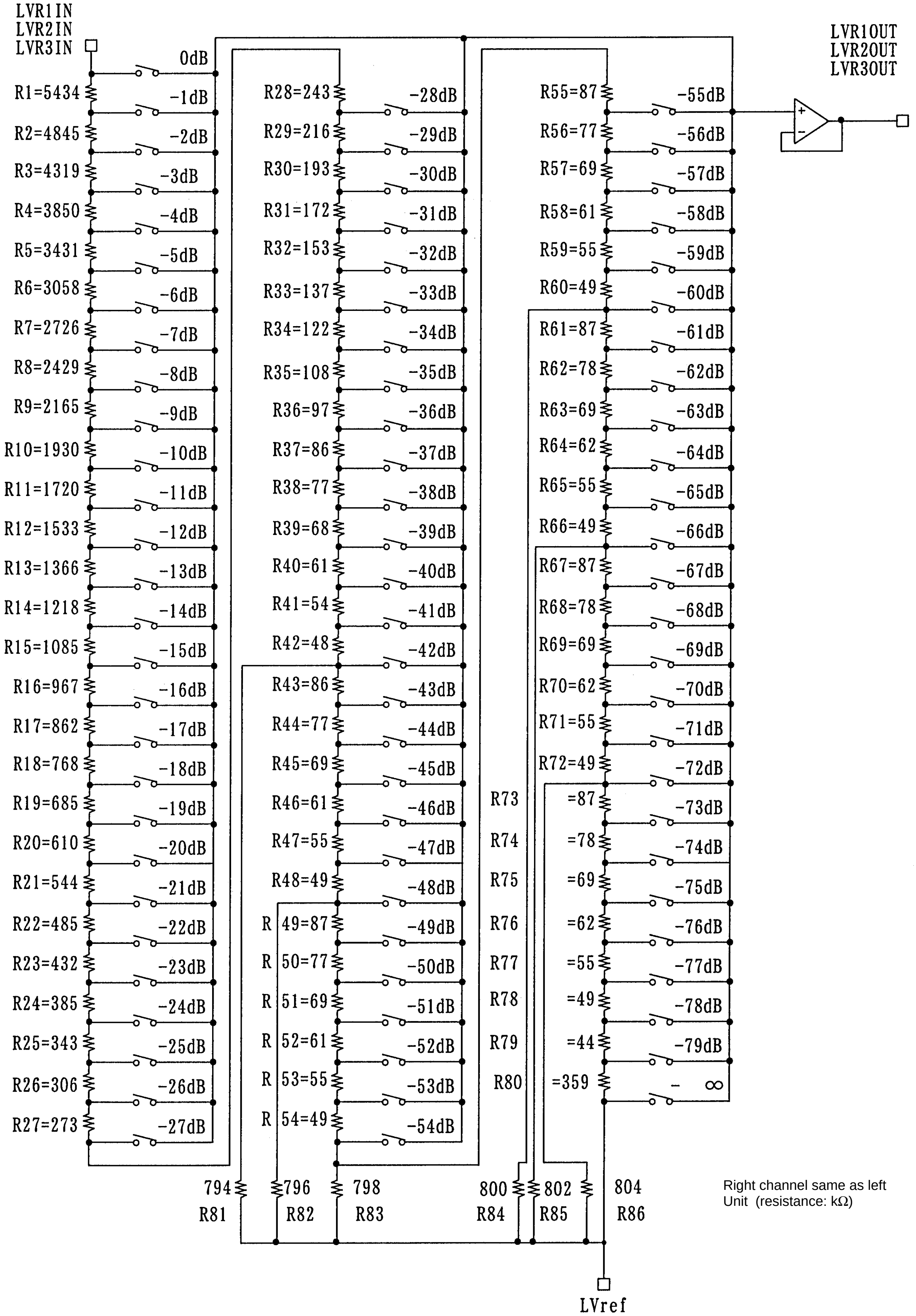
When providing boost, switches SW1 and SW3 are on, and when providing cut, switches SW2 and SW4 are on. In 0-dB mode (through), the 0-dB switch and switches SW2 and SW3 are on.

(4) F3/F4 band equalizer block internal equivalent circuit



Right channel same as left
Unit (resistance: kΩ)

Volume block internal equivalent circuit

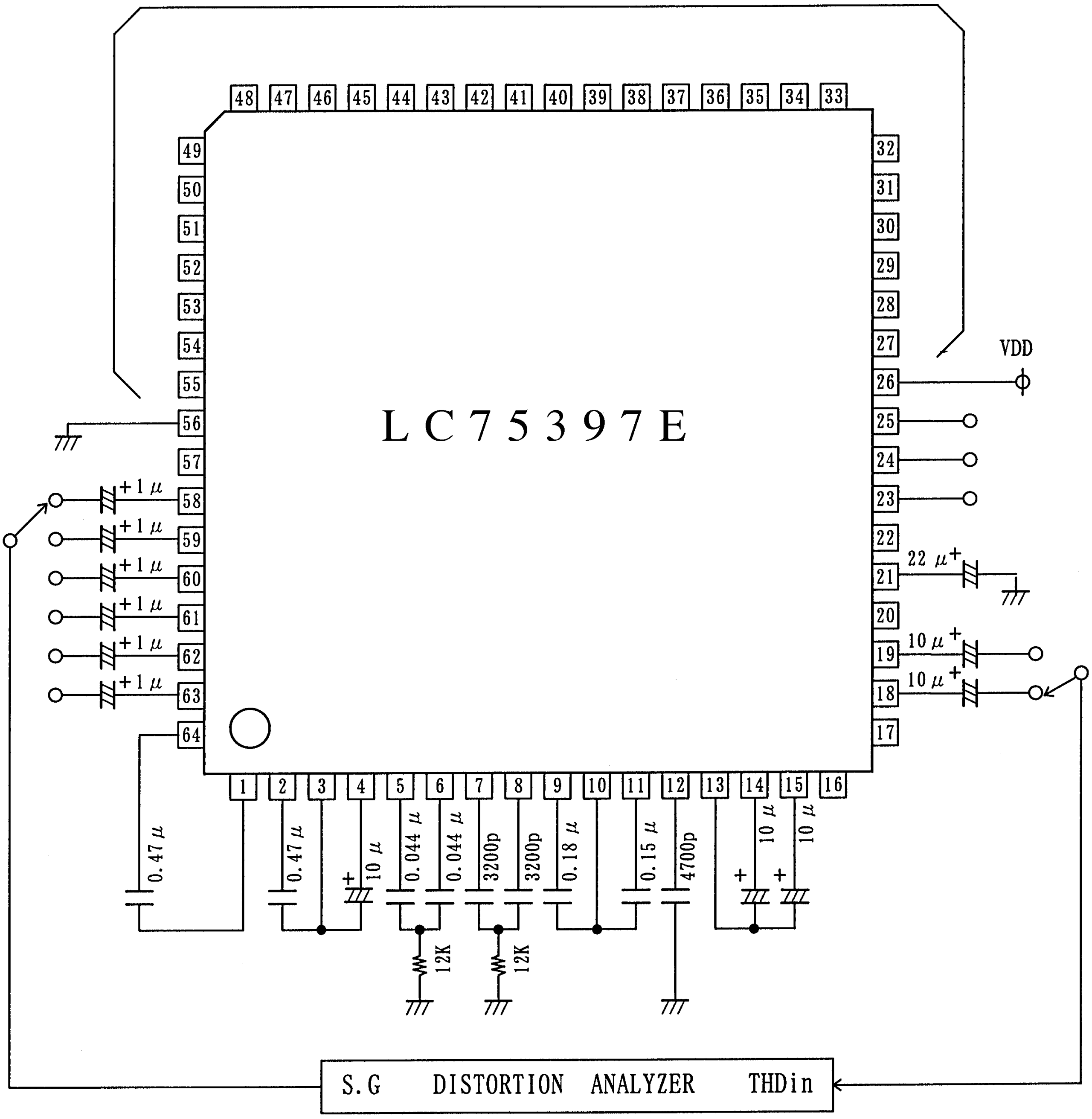


Right channel same as left
Unit (resistance: kΩ)

Test Circuits

Total Harmonic Distortion

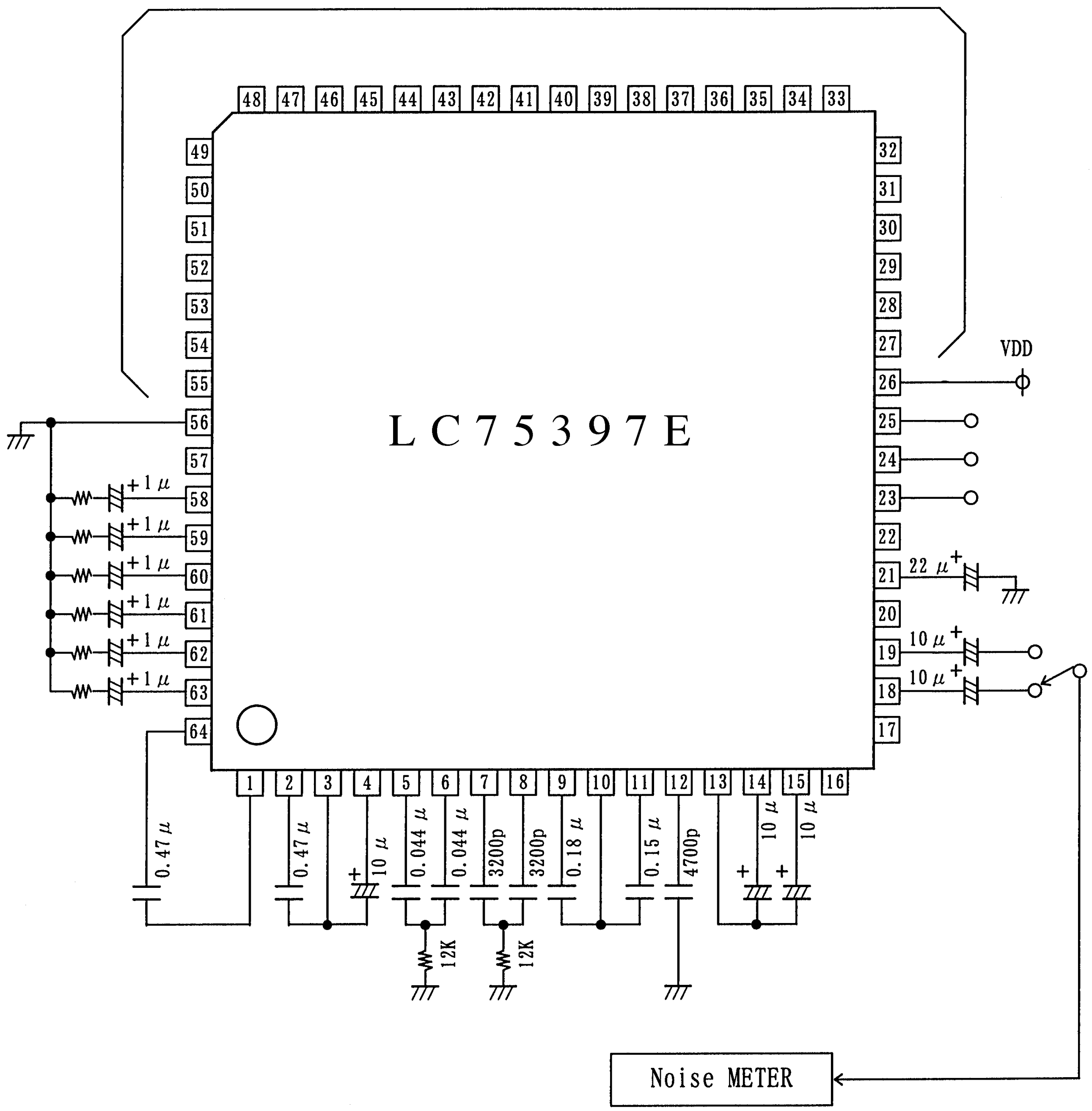
The left channel is identical



Unit (capacitance : F)

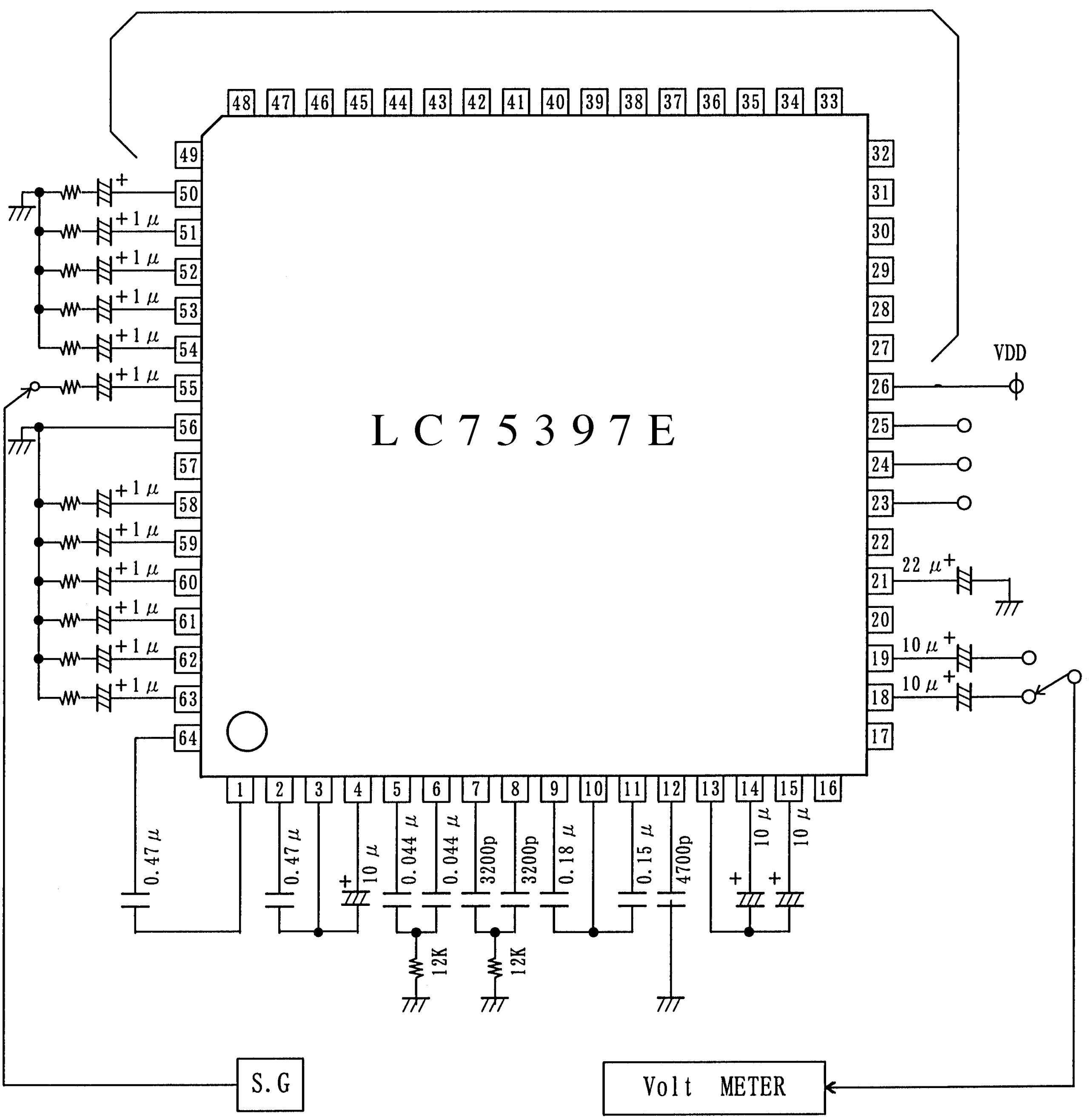
Output Noise Voltage

The left channel is identical



Unit (resistance : Ω, capacitance : F)

Crosstalk

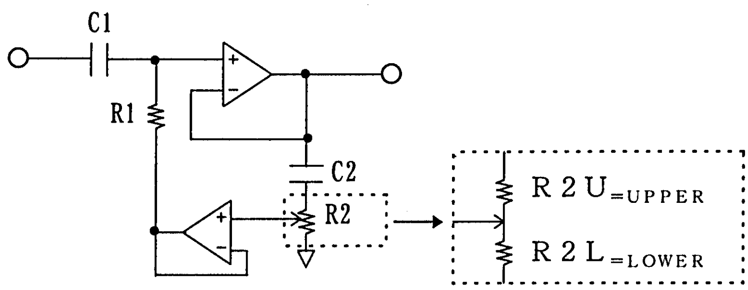


Unit (resistance : Ω, capacitance : F)

External Capacitor Calculations

1. Bass circuit

The value of the external capacitor used by the LC75397E bass control can be calculated as shown in the example below.



Sample calculation: For a center frequency f0 of 39 Hz
Substitute the LC75397E internal resistors R1 and R2 shown below into the above formula.
This allows the value of the capacitor, C, to be calculated.
R1 = 1.3 kΩ
R2 = 57.993 kΩ

Assume C1 = C2 = C.

$$C = \frac{1}{2\pi f0 \sqrt{R1R2}}$$

$$C = \frac{1}{2\pi \times 39 \times \sqrt{1300 \times 58000}} \neq 0.47\ \mu F$$

Formula for calculating the gain:

R1 = 1.3 kΩ
R2U = 1.476 kΩ
R2L = 56.517 kΩ

$$G = \sqrt{\left(\frac{R1}{R1 + R2U}\right)^2 + \left(\frac{R1\ (R2U + R2L)}{(R1 + R2U)\sqrt{R1\ (R2U + R2L)}}\right)^2} = 3.16 = 10\ dB$$

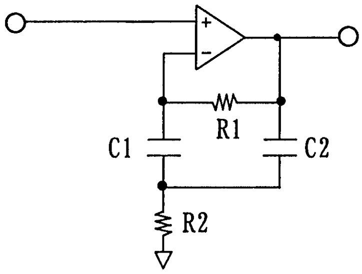
Formula for calculating Q:

$$Q = \sqrt{\frac{R1\ (R2U + R2L)}{(R1 + R2U)\sqrt{R1\ (R2U + R2L)}}} \neq G$$

2. F1/F2 band circuits

This section presents the equivalent circuit and the formulas used to calculate the external resistor and capacitor values to provide a center frequency of 148 Hz.

• F1/F2 band equivalent circuit



• Sample calculation

Specifications: Center frequency: f0 = 148 Hz
Gain at maximum boost: G_{+10dB} = 10 dB
Assume R1 = 51.8 kΩ and C1 = C2 = C.

(1) Determine R2 from the specification that G_{+10dB} = 10 dB.

$$G_{+10dB} = 20 \times LOG_{10}\left(1 + \frac{R1}{2R2}\right)$$

$$R2 = \frac{R1}{2\,(10^{G+10dB/20} - 1)} = \frac{51800}{2 \times (3.162 - 1)} = 11979.7 \neq 12\ k\Omega$$

(2) Determine C from the specification that the center frequency f0 = 148 Hz.

$$f0 = \frac{1}{2\pi f\sqrt{R1R2C1C2}}$$

$$C = \frac{1}{2\pi f0\sqrt{R1R2}} = \frac{1}{2\pi \times 148\sqrt{51800 \times 12000}} = 0.0431 \times 10^{-6} \neq 0.044\ \mu F$$

(3) Determine Q.

$$Q = \frac{C \cdot C \cdot R1}{2C} \cdot \frac{1}{\sqrt{R1R2CC}} = \frac{51800}{2\sqrt{51800 \times 12000}} = 1.039$$

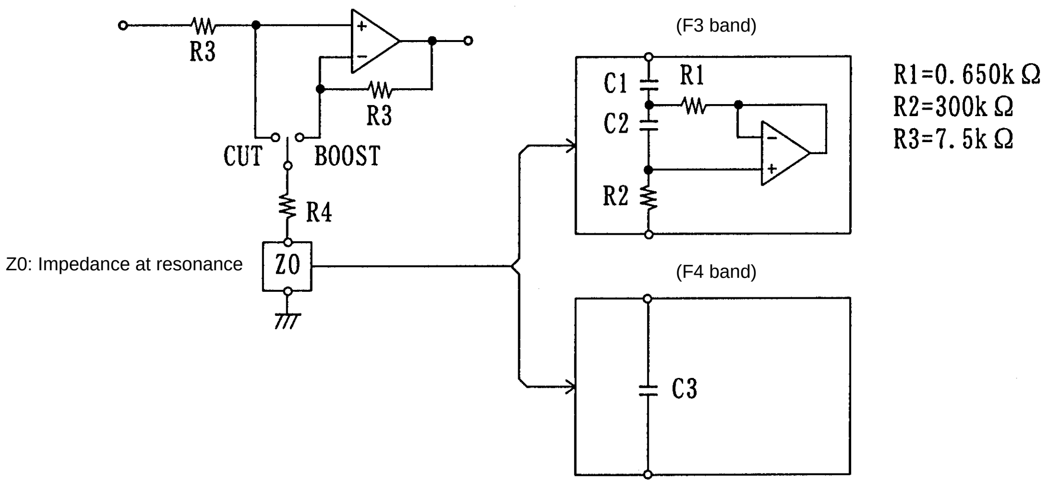
3. F3/F4 band circuits

The F3 band circuit supports peaking characteristics and the F4 band circuit supports shelving characteristics.

(1) Peaking characteristics (F3 band)

The external capacitor is used to construct a simulated inductor. This section presents the equivalent circuit and the formulas for determining the desired center frequency.

(a) Simulated inductor equivalent circuit



(b) Sample calculation

Specifications: 1) Center frequency: f0 = 107 Hz
2) Q at maximum boost: $Q_{+10dB} = 0.8$

(1) Determine the sharpness, Q0, of the simulated inductor itself.
$Q_0 = (R1 + R4) / R1 \times Q_{+10dB} \approx 4.270$

(2) Determine C1.
$C1 = 1/2\pi f0R1Q_0 \approx 0.536$ (µF)

(3) Determine C2.
$C2 = Q_0 / 2\pi f0R2 \approx 0.021$ (µF)

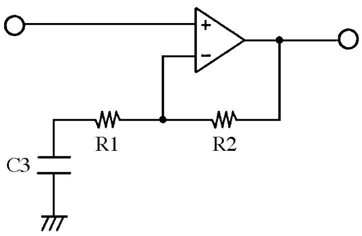
(c) Reference values for C1 and C2

Center frequency f0 (Hz)	C1 (F)	C2 (F)
107	0.536 µ	0.021 µ
340	0.169 µ	6663P
1070	0.054 µ	2117P
3400	0.017 µ	666P

(2) Shelving characteristics (F4 band)

Gains of ±10 dB (in 2-dB steps) with respect to a target frequency can be achieved by using an external capacitor C3 with a calculated according to the formula F shown below.

Equivalent circuit and formula when boosting.



Sample calculation

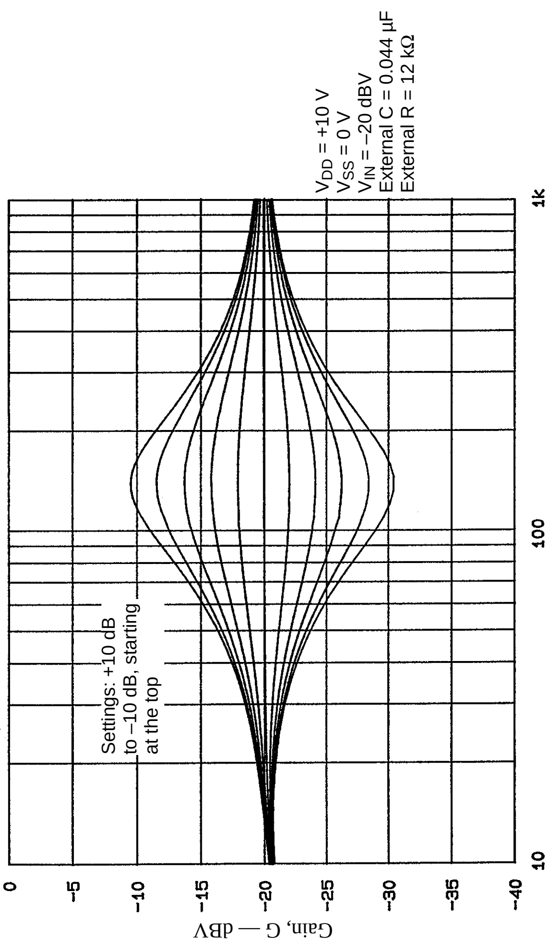
Specifications: 1) Target frequency: f = 17,000 Hz
2) R1= 2,819 kΩ, R2 = 7.5 kΩ

$$C = \frac{1}{2\pi f \sqrt{\left(\frac{R2}{10^{G/20} - 1}\right)^2 - R1^2}}$$

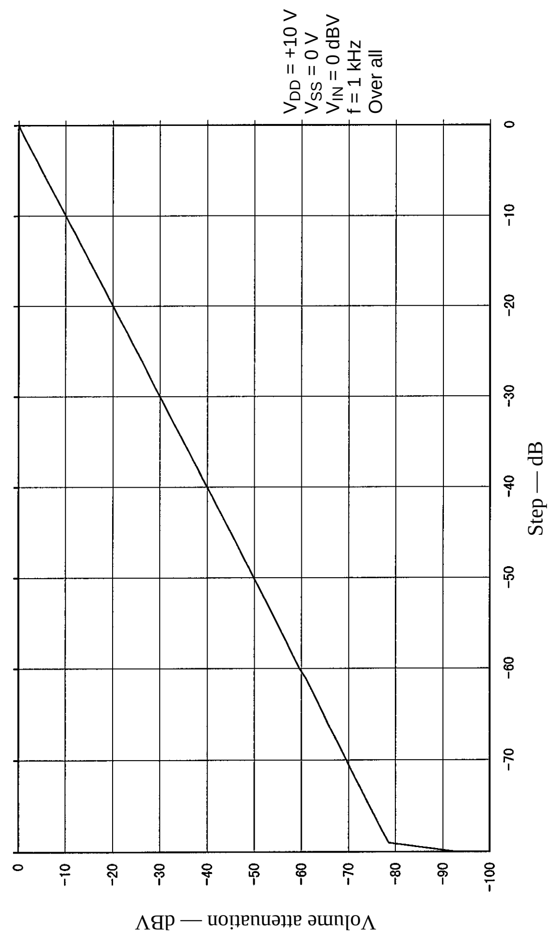
$$= \frac{1}{2\pi \times 17000 \sqrt{\left(\frac{7500}{3.16 - 1}\right)^2 - (2819)^2}}$$

$$\neq 4600 \text{ (pF)}$$

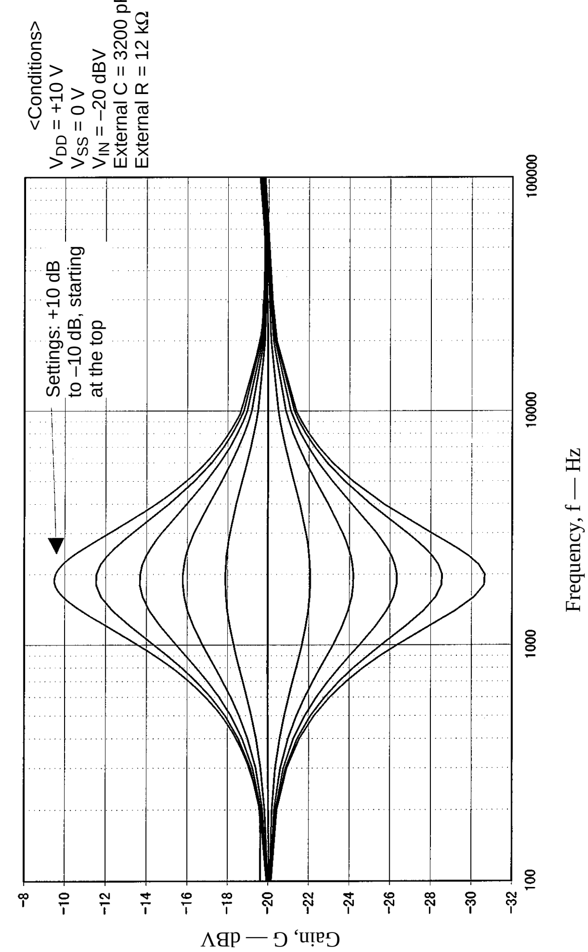
F1 Band Frequency Characteristics



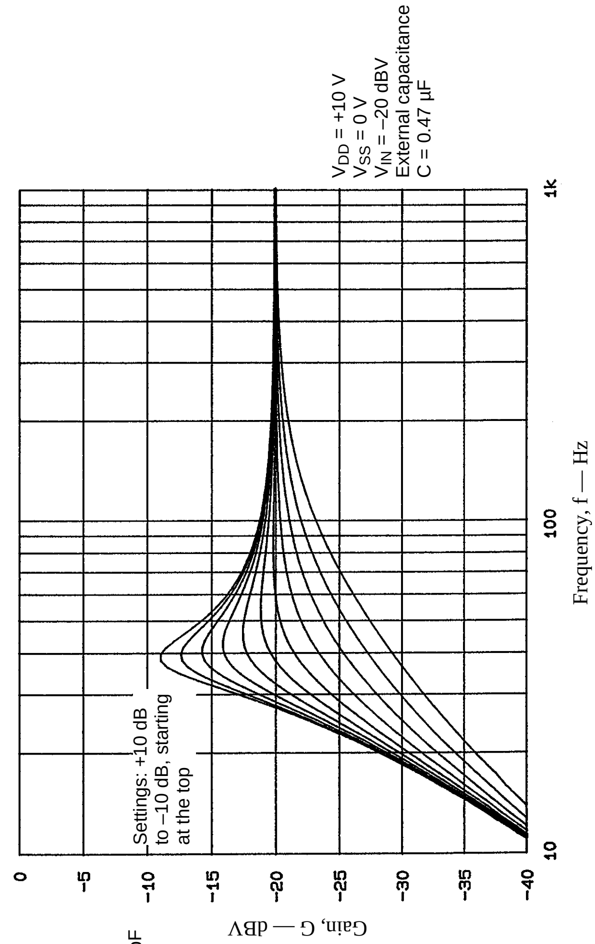
Volume Step Characteristics



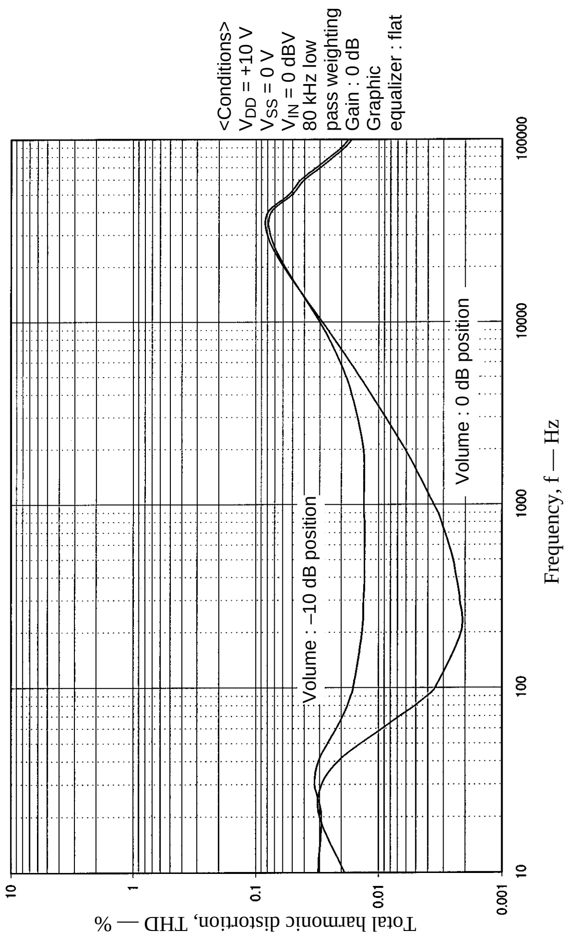
F2 Band Frequency Characteristics



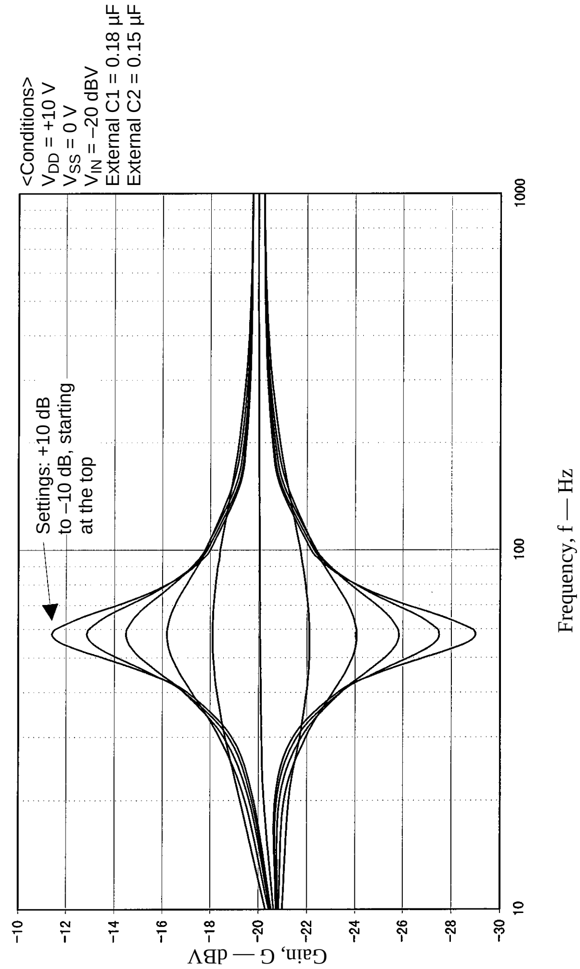
Bass Band Frequency Characteristics



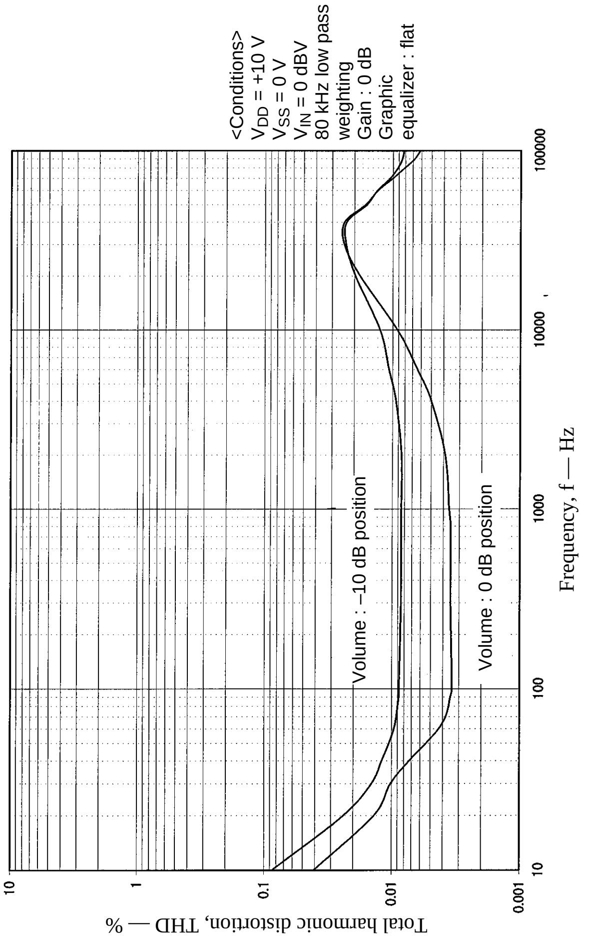
THD—Frequency Chapacteristics (1)



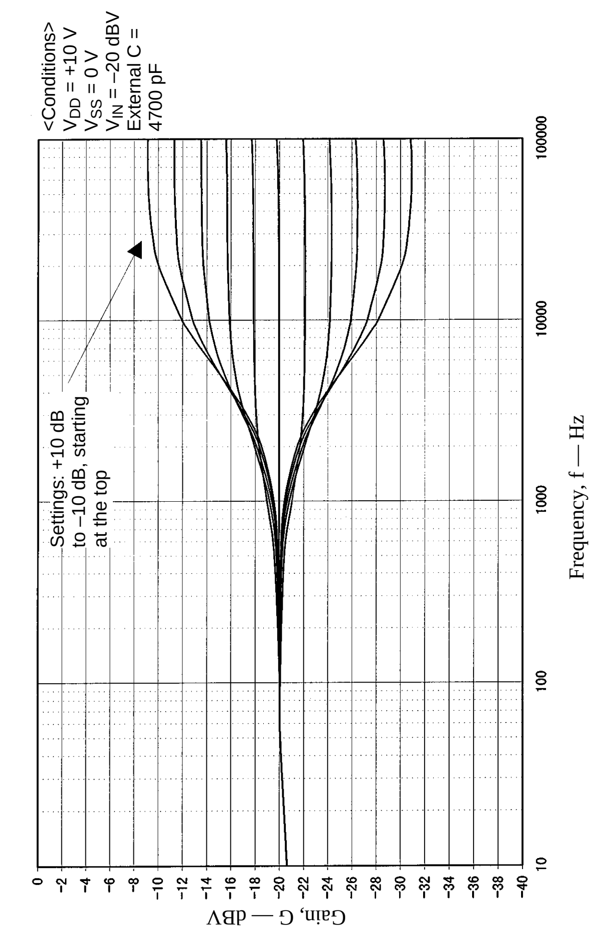
F3 Band Frequency Characteristics

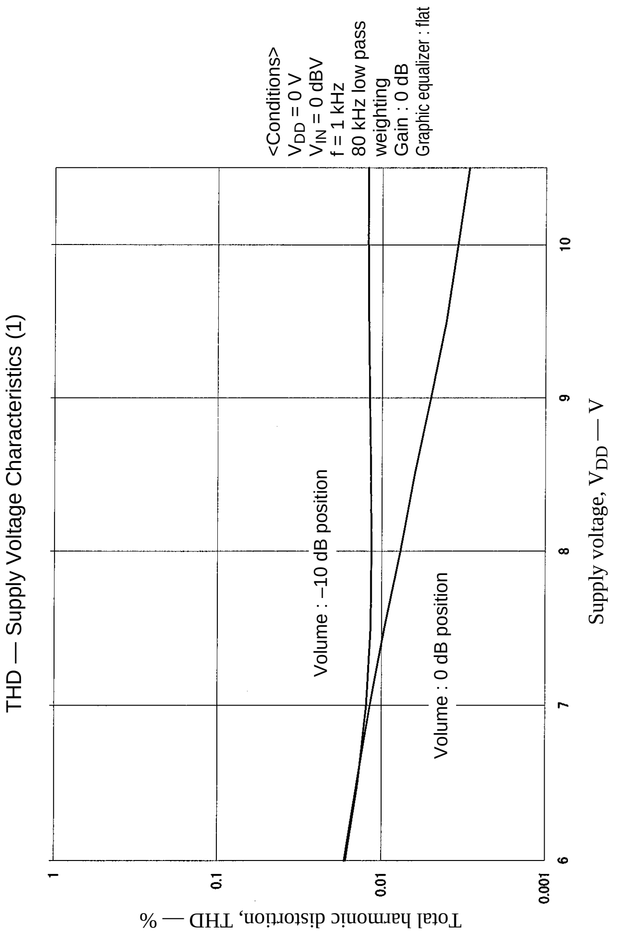


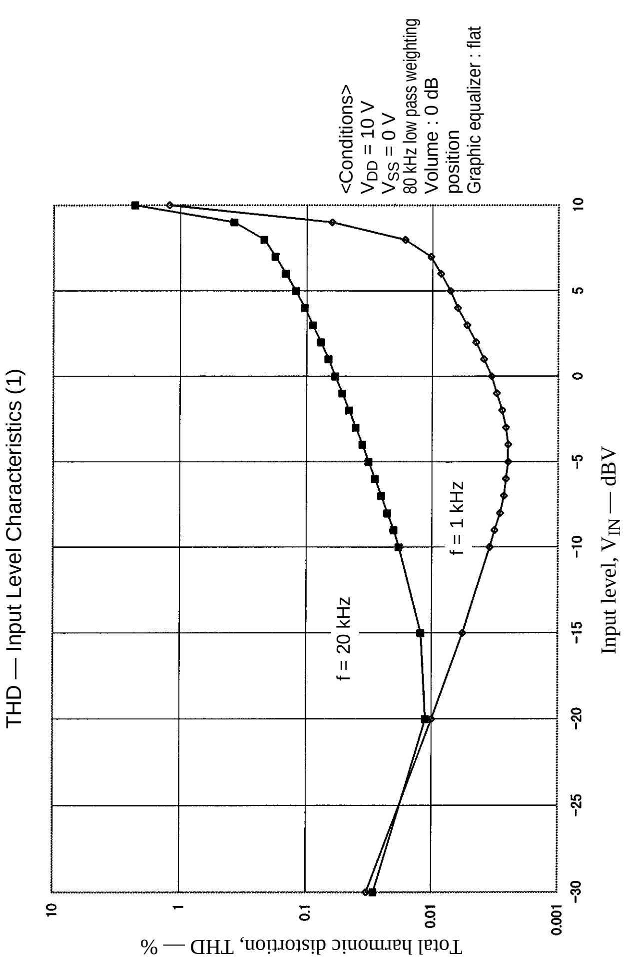
THD—Frequency Chapacteristics (2)

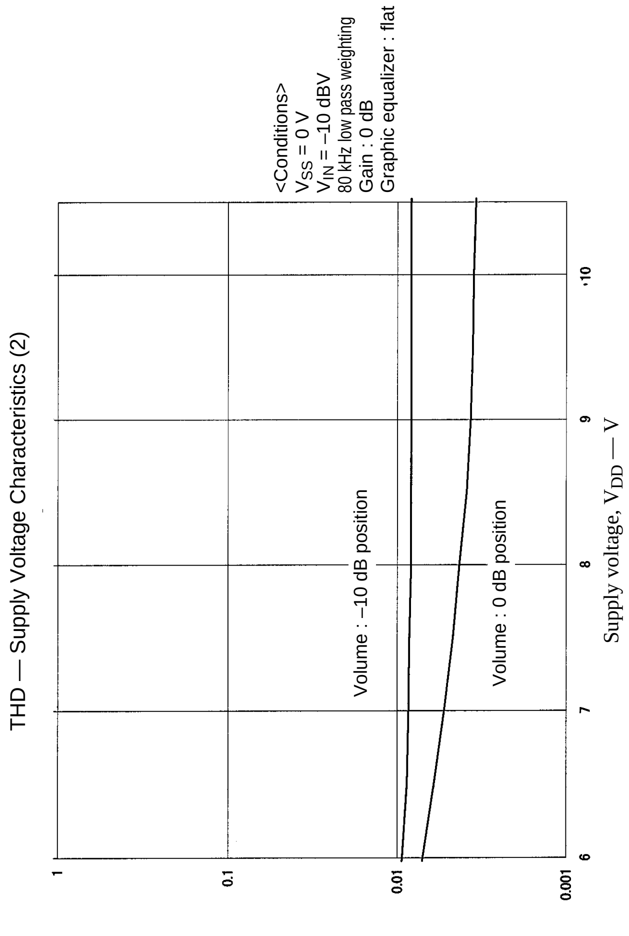


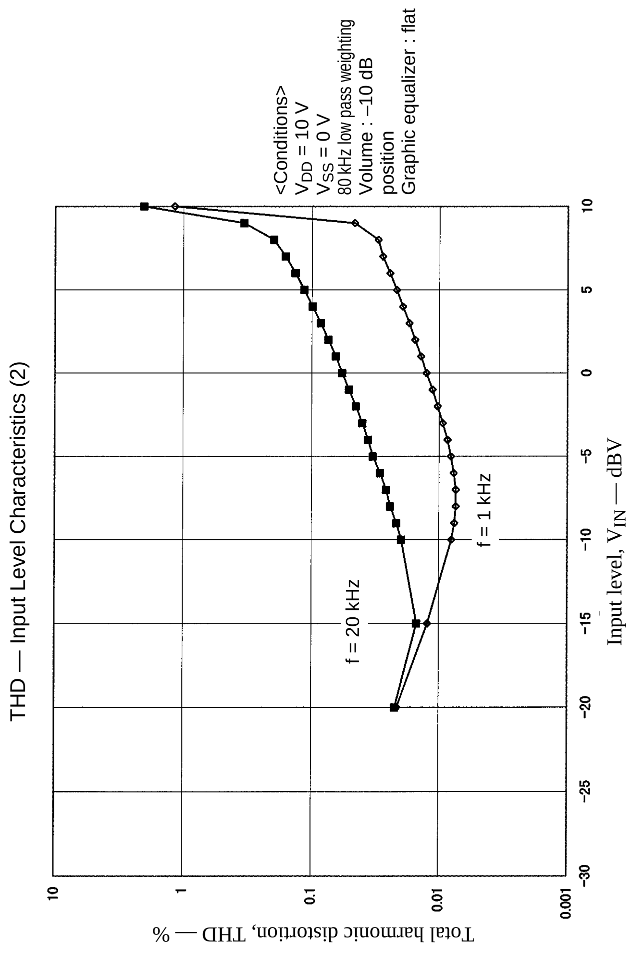
F4 Band Frequency Characteristics




THD — Supply Voltage Characteristics (1)
<Conditions>
VDD = 0 V
VIN = 0 dBV
f = 1 kHz
80 kHz low pass weighting
Gain : 0 dB
Graphic equalizer : flat
Volume : –10 dB position
Volume : 0 dB position
Total harmonic distortion, THD — %
Supply voltage, VDD — V
1
0.1
0.01
0.001
6
7
8
9
10


THD — Input Level Characteristics (1)
<Conditions>
VDD = 10 V
VSS = 0 V
80 kHz low pass weighting
Volume : 0 dB position
Graphic equalizer : flat
f = 20 kHz
f = 1 kHz
Total harmonic distortion, THD — %
Input level, VIN — dBV
10
1
0.1
0.01
0.001
–30
–25
–20
–15
–10
–5
0
5
10


THD — Supply Voltage Characteristics (2)
<Conditions>
VSS = 0 V
VIN = –10 dBV
80 kHz low pass weighting
Gain : 0 dB
Graphic equalizer : flat
Volume : –10 dB position
Volume : 0 dB position
Supply voltage, VDD — V
1
0.1
0.01
0.001
6
7
8
9
10


THD — Input Level Characteristics (2)
<Conditions>
VDD = 10 V
VSS = 0 V
80 kHz low pass weighting
Volume : –10 dB position
Graphic equalizer : flat
f = 20 kHz
f = 1 kHz
Total harmonic distortion, THD — %
Input level, VIN — dBV
10
1
0.1
0.01
0.001
–30
–25
–20
–15
–10
–5
0
5
10

Usage Notes

- When the power is first applied, the internal analog switches are in indeterminate states. The chip therefore requires muting or other external measures until it has received the proper data.
- After power is first applied, applications must initialize this chip by sending the initial data (1) and (2) described below.
- Provide grounding patterns or shielding for the lines to the CL, DI, and CE pins so as to prevent their high-frequency digital signals from interfering with the operation of nearby analog circuits.