Ordering number : EN5641A

CMOS LSI

LC4105V

Level Shifter

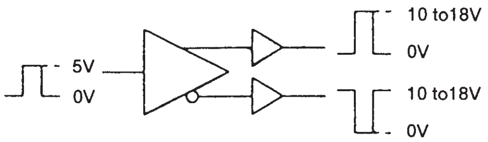
Overview

The LC4105V is a level shifter driver that converts 5-V signals into signals with amplitudes between 10 and 18 V.

Features

- Seven inputs and eleven outputs
  IN1 to IN3 produce only true outputs.
  IN4 to IN7 produce both true and inverted outputs.

- Slim SSOP-30 package

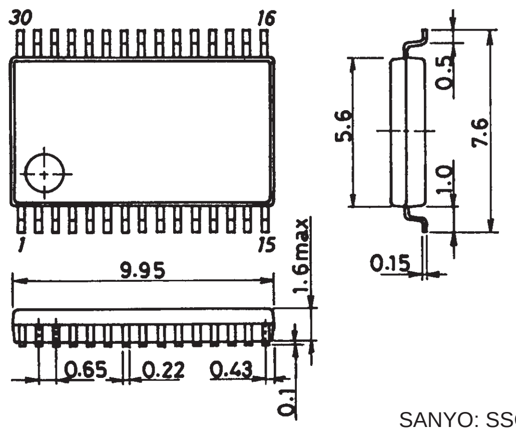


Package Dimensions

unit: mm

3191-SSOP30

[LC4105V]



SANYO: SSOP30

Specifications

Absolute Maximum Ratings at Ta = 25°C ± 2°C, all voltages are relative to V_{SS}, unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}		–0.3		20	V
	$V_{DD}1$		–0.3		20	V
	V_{CC}		–0.3		7	V
	$V_{SS}1$		–0.3		+0.3	V
Input voltage	V_{IN}	IN1 to IN7	–0.5		V_{CC} +0.5	V
Power dissipation	Pd	Ta ≤ 75°C			200	mW
Storage temperature	Tstg		–55		+125	°C

Allowable Operating Ranges at voltages relative to V_{SS}

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}	*	10		18	V
	$V_{DD}1$	*		V_{DD}		V
	V_{CC}	*	3.0		5.5	V
	$V_{SS}1$	*		V_{SS}		V
High-level input voltage	V_{IN}-H	IN1 to IN7 (V_{CC} = 4.5 to 5.5 V)	2.4		V_{CC}	V
		(V_{CC} = 3.0 to 4.5 V)	0.7 V_{CC}		V_{CC}	
Low-level input voltage	V_{IN}-L	IN1 to IN7 (V_{CC} = 4.5 to 5.5 V)	0		0.8	V
		(V_{CC} = 3.0 to 4.5 V)	0		0.1 V_{CC}	
Operating temperature	Topr		–10		+75	°C

Note: * Applications must observe the directions in the note on page 5 at power on and at power off.

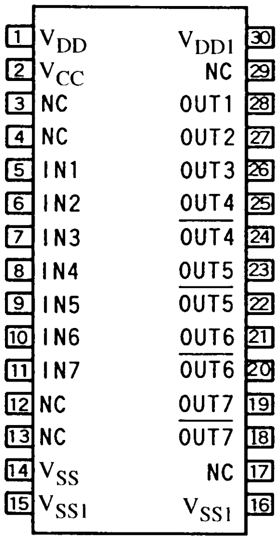
Electrical Characteristics

at Ta = 25°C ±2°C, V_{CC} = 5 V, and V_{DD} = 16 V, all voltages are relative to V_{SS}, unless othrewise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level input current	I_{ih}	Vin = V_{CC} IN1 to IN7			1	µA
Low-evel input current	I_{il}	Vin = V_{SS} IN1 to IN7	–1			µA
High-level output voltage	V_{oh}	Io = 1 mA	V_{DD}–1		V_{DD}	V
Low-level output voltage	V_{ol}	Io = –1 mA	V_{SS}		V_{SS}+1	V
Output on resistance	Rout	V_{DD} = $V_{DD}1$ = 10 V Io = ±1 mA		60		Ω
Current drain while idling	I_{CCI}	V_{DD} = $V_{DD}1$ = 18 V, V_{CC} = 5.5 V		0.01	10	µA
	I_{DDI}*	IN1 to IN7 = 0 V All outputs open.		0.10	10	µA
Current drain during operation	I_{CCa}	V_{DD} = $V_{DD}1$ = 15 V, V_{CC} = 5.5 V		16		µA
	I_{DDa}*	IN0 to IN6 = 0 V IN7 = 0 to 5.5 V/2 MHz Load 1		10		mA

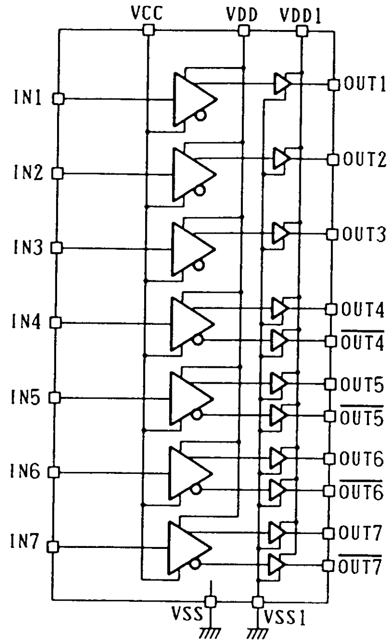
Note: * I_{DD}I and I_{DD}a are the total currents flowing into power supply pins V_{DD} and $V_{DD}1$.

Pin Assignment



Top view

Block Diagram



Pin Descriptions

Pin Name	I/O	Pin Number	Function
OUT1 OUT2 OUT3 OUT4 OUT4* OUT5 OUT5* OUT6 OUT6* OUT7 OUT7*	O	28 27 26 25 24 23 22 21 20 19 18	Level shifter outputs
IN1 IN2 IN3 IN4 IN5 IN6 IN7	I	5 6 7 8 9 10 11	Level shifter inputs
V_{DD}	—	1	Level shifter high-voltage power supply
$V_{DD}1$	—	30	Buffer high-voltage power supply
V_{CC}	—	2	Level shifter low-voltage power supply
$V_{SS}1$	—	15, 16	Buffer ground
V_{SS}	—	14	Level shifter ground
NC		3, 4, 12, 13, 17, 29	Do not connect anything to these pins.

Switching Characteristics at Ta = 25°C ±2°C, V_{CC} = 5 V ±10%, V_{DD} = 10 to 18 V

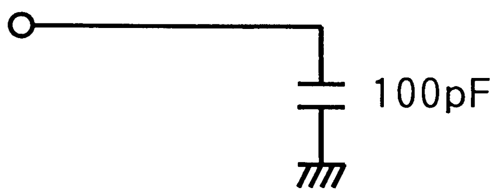
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Propagation delay	tpLH(1)	Load 1		33	60	ns
	tpHL(1)			35	60	ns
	tpLH(2)		tpHL(1)–10	36	tpHL(1)+20	ns
	tpHL(2)		tpLH(1)–20	20	tpLH(1)+10	ns
Rising time	tr	Load 1		24	50	ns
Falling time	tf	Load 1		24	50	ns

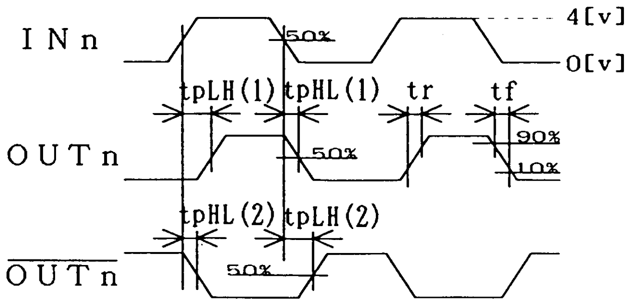
at Ta = 25°C ±2°C, V_{CC} = 3.0 to 4.5 V, V_{DD} = 10 to 18 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Propagation delay	tpLH(1)	Load 1			100	ns
	tpHL(1)				120	ns
	tpLH(2)				120	ns
	tpHL(2)				100	ns
Rising time	tr	Load 1			50	ns
Falling time	tf	Load 1			50	ns

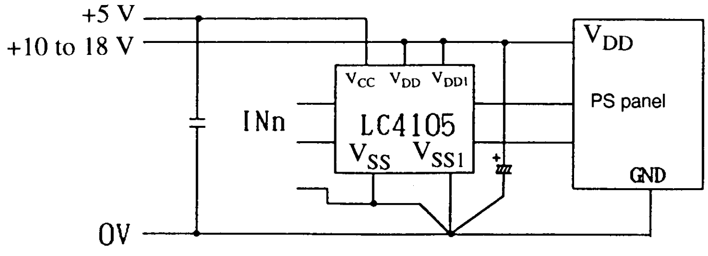
Note: The typical values are measured for OUT1 output with V_{CC} = 5.5 V and V_{DD} = 15 V.

Load 1





Power Supply Circuits

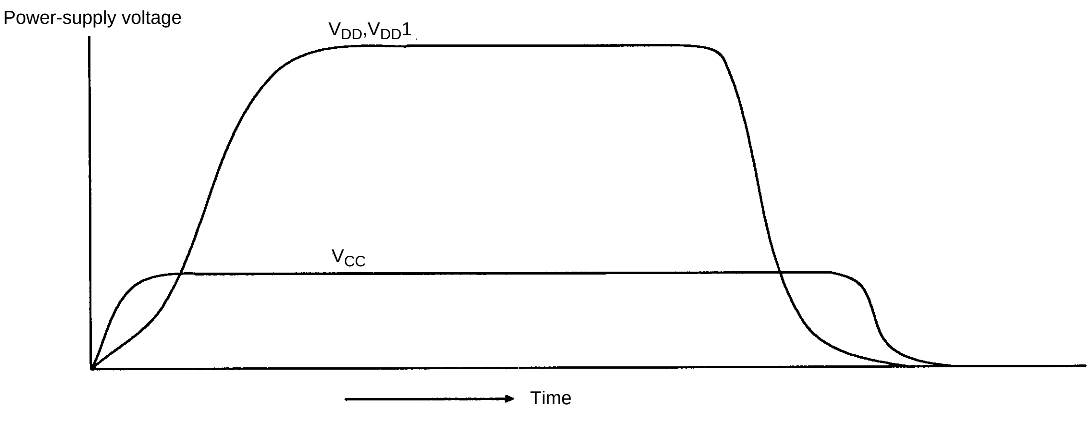


Keep the impedance of the V_{SS} and $V_{SS}1$ lines as low as possible. Connect a large electrolytic capacitor across the $V_{DD}1$ and $V_{SS}1$ pins and close to the IC. Wherever possible, keep the grounds for the power supply circuits and the signal circuits separate and connect the two at a single point.

Notes on Power-Supply Voltage Application

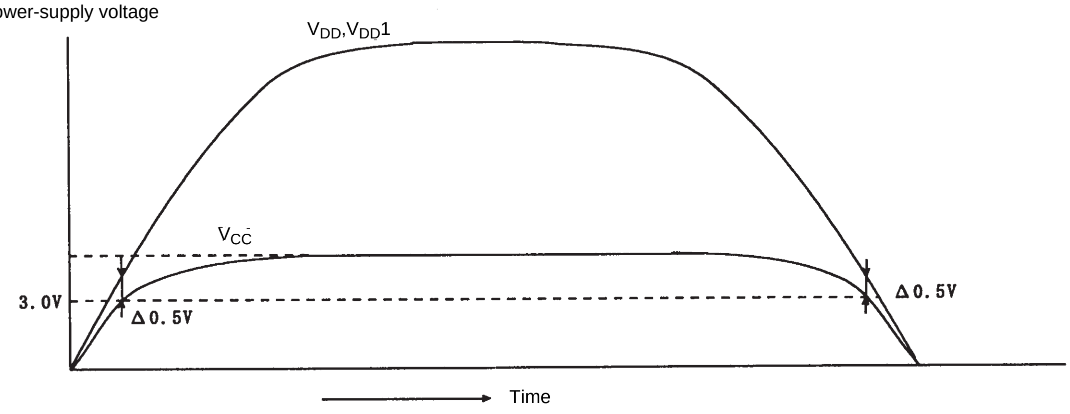
This IC has two power supply systems: V_{DD} ($V_{DD}1$) and V_{CC}, and requires that applications observe the notes provided here when applying or removing these voltages. In particular, if the V_{DD} ($V_{DD}1$) system power-supply voltage becomes higher than the V_{CC} system voltage while the V_{CC} system voltage is not yet established (i.e. is less than V_{CC}min), excessive currents may flow and the IC may be destroyed. To prevent destruction of the IC due to this phenomenon, applications must, basically, follow the sequence described in item 1 below when turning the power supplies on or off.

1. When turning the power on, first apply the V_{CC} voltage (bring this voltage to a value above V_{CC}min), and then apply the V_{DD} voltage. When turning the power off, first drop the V_{DD} voltage, and, after V_{DD} is below V_{CC}min, then drop the V_{CC} voltage.



However, there are many cases where it is not possible to control the power-supply voltage on/off sequence. This IC is actually capable of supporting the on/off sequence described in item 2 below.

2. If V_{DD} (V_{DD}1) and V_{CC} are turned on and off at essentially the same time, the difference between V_{DD} and V_{CC} (e.g. the distance in the figure marked as Δ0.5 V) must be held to be under 0.5 V while V_{CC} is less than or equal to 3.0 V.



Another point is that a certain amount of time is required to stabilize the V_{CC} system when V_{CC} is first applied and the IC is easily destroyed during this period. Inversely, when the power is removed, the V_{CC} system state is easily retained and as a result the device cannot be destroyed easily. In actual use, one can consider there to be a certain amount of margin for removing the V_{DD} (V_{DD}1) voltage even after V_{CC} has already been dropped. However, this margin varies with sample-to-sample variations in the IC itself and with the details of the application circuit, and careful analysis and consideration of the actual usage conditions is required to assure that the IC will not be destroyed if the sequences in items 1 or 2 are not observed.

3. Note that when power is turned off and then immediately turned back on again, many circuit designs may fail to meet the conditions for the sequences described in items 1 and 2 above. Be sure to take this into account when designing applications that use this IC.