

LC36256ALL, AMLL-70/85/10/12

256 K (32768 words \times 8 bits) SRAM

Overview

The LC36256ALL, AMLL are fully asynchronous silicon gate CMOS static RAMs with a 32768 words \times 8 bits configuration.

This series has CE chip enable pin for device select/nonselect control and an OE output enable pin for output control, and features high speed as well as low power dissipation.

Current dissipation is notably reduced during stand-by and data retention. For these reasons, this series is most suited for use in systems requiring high speed, low power consumption and long-term battery backup. Simple memory capacity expansion is also supported.

Features

• Access time

ns (max.): LC36256ALL-70, LC36256AMLL-70
ns (max.): LC36256ALL-85, LC36256AMLL-85
ns (max.): LC36256ALL-10, LC36256AMLL-10
ns (max.): LC36256ALL-12, LC36256AMLL-12

· Low current dissipation

During standby

0			
0.5	μA (max.)	/	$Ta = 25^{\circ}C$
1	μA (max.)	/	$Ta = 0$ to $+40^{\circ}C$

- 5 μ A (max.) / Ta = 0 to +70°C
- During data retention

0.3 μ A (max.) / Ta = 25°C	
--------------------------------	--

0.6	μA (max.)	/	$Ta = 0$ to $+40^{\circ}C$
3	μA (max.)	/	$Ta = 0$ to $+70^{\circ}C$

During operation (DC) 10 mA (max.)

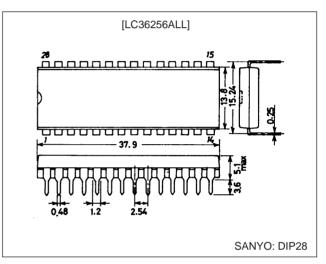
- Single 5 V power supply: $5 V \pm 10\%$
- Data retention power supply voltage: 2.0 to 5.5 V
- No clock required (Fully static memory)
- All input/output levels are TTL compatible
- Common input/output pins, with three output states
- Packages

DIP 28- pin (600 mil) plastic package	:	LC36256ALL
SOP 28-pin (450 mil) plastic package	:	LC36256AMLL

Package Dimensions

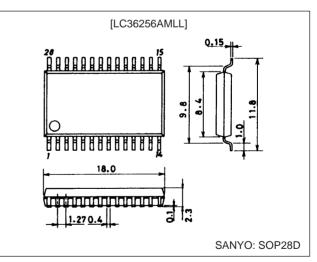
unit: mm

3012A-DIP28





3187-SOP28D

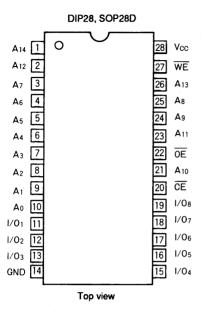


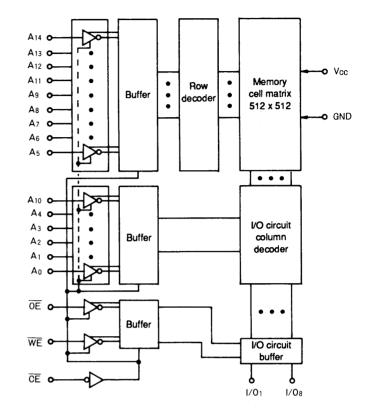
SANYO Electric Co., Ltd. Semiconductor Bussiness Headquarters TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

LC36256ALL, AMLL-70/85/10/12

Pin Assignment

Block Diagram





Pin Functions

A0 to A14	Address input
WE	Read/write control input
OE	Output enable input
CE	Chip enable input
I/O1 to I/O8	Data input/output
VCC, GND	Power supply pins

Functions

Mode	CE	OE	WE	I/O	Supply current
Read cycle	L	L	н	Data output	I _{CCA}
Write cycle	L	Х	L	Data input	I _{CCA}
Output disable	L	Н	Н	High impedance	I _{CCA}
Nonselect	Н	Х	Х	High impedance	I _{CCS}

X : H or L

Specifications

Absolute Maximum Ratings at Ta= $25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	Vcc max		7.0	V
Input pin voltage	Vin		-0.5* to Vcc+0.5	V
I/O pin voltage	Vi/o		-0.5* to Vcc+0.5	V
Allowable power dissipation	Pd max	LC36256ALL	1.0	W
	T d max	LC36256AMLL	0.7	W
Operating temperature range	Topr		0 to +70	°C
Storage temperature range	Tstg		-55 to +150	°C

* -3.0 V when pulse width is less than 50 ns

DC Recommended Operating Ranges at Ta = 0 to $+70^{\circ}C$

Parameter	Symbol	min	typ	max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input high level voltage	Vih	2.2		Vcc+0.3	V
Input low level voltage	VIL	-0.3*		+0.8	V

* -3.0 V when pulse width is less than 50 ns

DC Electrical Characteristics at Ta = 0 to $+70^{\circ}$ C, Vcc = 5 V $\pm 10\%$

Parameter	Symbol	Co	nditions		min	typ*	max	Unit	
Input leakage current	lu -	VIN = 0 to VCC			-0.5		+0.5	μA	
I/O leakage current	Ilo	VCE = VIH or VC VI/O = 0 to VCC	e = Vih,		-0.5		+0.5	μA	
Output high level voltage	Vон	Iон = -1.0mA						V	
Output low level voltage	Vol	IoL = 2.1mA				0.4	V		
Operating supply current (DC)				$CE \le 0.2V,$ IN $\le 0.2V$ or $VIN \ge VCC-0.2V$			5	mA	
current (DO)	ICCA2	VCE = VIL, II/O=0)mA			3	10	mA	
	Іссаз	min cycle Duty = 100% I _{I/O} = 0mA	Access time	70ns		30	50	- mA	
Average operating				85ns		25	50		
supply current				100ns		23	50		
				120ns		20	50		
				0 to +70°C			5		
Standby supply	ICCS1	V _{CE} ≥V _{CC} -0.2V		0 to +40°C			1	μA	
current				25°C		0.2	0.5	1	
	ICCS2	VCE = VIH				0.4	2	mA	

* Reference values at VCC = 5 V, Ta = 25° C

Input/Output Capacitance at Ta = 25° C, f = 1 MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Input/output capacitance	Ci/O	VI/O = 0V			8	pF
Input capacitance	CIN	VIN = 0V			6	pF

Note: These parameters were obtained through sampling, and not full-lot measurement.

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V $\pm 10\%$

AC testing conditions

6		
Input pulse voltage level	:	0.8 V, 2.2 V
Input rise and fall time	:	5 ns
Input - output timing level	:	1.5 V
Output load	:	1 TTL gate + $CL = 100 \text{ pF} (85 \text{ ns}/100 \text{ ns}/120 \text{ ns})$
		1 TTL gate + $CL = 30 \text{ pF} (70 \text{ ns})$
		(including scope and jig capacitance)

Read Cycle

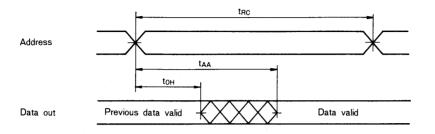
		LC36256ALL, AMLL								
Parameter	Symbol	-	70	-	85	-	10	-	·12	Unit
		min	max	min	max	min	max	min	max	
Read cycle time	t _{RC}	70		85		100		120		ns
Address access time	t _{AA}		70		85		100		120	ns
CE access time	t _{CA}		70		85		100		120	ns
OE access time	t _{OA}		35		45		50		60	ns
Output hold time	t _{OH}	20		20		20		20		ns
CE output enable time	t _{COE}	10		10		10		10		ns
OE output enable time	t _{OOE}	5		5		5		5		ns
OE output disable time	t _{COD}	0	30	0	30	0	30	0	30	ns
OE output disable time	t _{OOD}	0	30	0	30	0	30	0	30	ns

Write Cycle

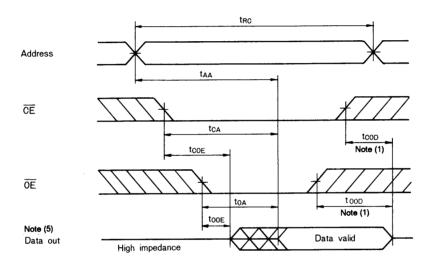
		LC36256ALL, AMLL								
Parameter		-70		-85		-10		-12		Unit
		min	max	min	max	min	max	min	max	
Write cycle time	t _{WC}	70		85		100		120		ns
Address valid to end of write	t _{AW}	65		75		80		100		ns
Address setup time	t _{AS}	0		0		0		0		ns
Write pulse width	t _{WP}	50		50		60		70		ns
CE setup time	t _{CW}	65		75		80		100		ns
Write recovery time (WE)	t _{WR}	0		0		0		0		ns
Write recovery time (CE)	t _{WR} 1	0		0		0		0		ns
Data setup time	t _{DS}	30		30		35		40		ns
Data hold time	t _{DH}	0		0		0		0		ns
WE output enable time	t _{WOE}	10		10		10		10		ns
WE output disable time	t _{WOD}	0	25	0	25	0	25	0	25	ns

Timing Chart

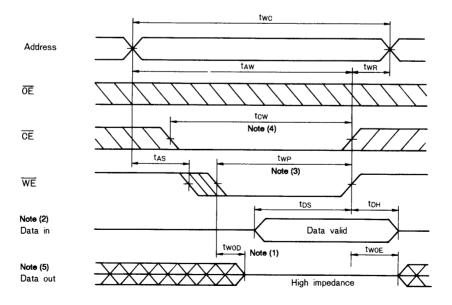
• Read Cycle (1): CE = OE = VIL, WE = VIH



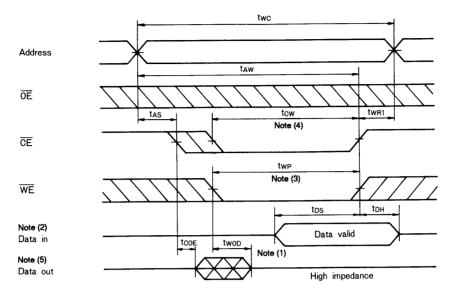
• Read Cycle (2): WE = VIH



• Write Cycle (1): WE Control Note (6)



• Write Cycle (2): CE Control Note (6)



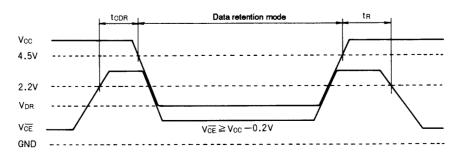
- Notes (1) t_{COD}, t_{OOD}, and t_{WOD} are defined as the time at which the outputs becomes the high impedance state and are not referred to output voltage levels.
 - (2) An external antiphase signal must not be applied when DOUT is in the output state.
 - (3) t_{WP} is the time interval that CE and WE are low-level and is defined as the interval from the falling of \overline{WE} to the rising of CE or WE whichever is earlier.
 - (4) t_{CW} is the time interval that CE and WE are low-level and is defined as the time from the falling of \overline{CE} to the rising of CE or WE whichever is earlier.
 - (5) DOUT goes to the high-impedance state when either OE is high-level, CE is high-level, or WE is low-level.
 - (6) When OE is high-level during the write cycle, DOUT goes to the high-impedance state.

Parameter	Symbol	Conditions			typ*	max	Unit
Data retention supply voltage	supply voltage VDR VCE ≥ VCC-0.2V			2.0		5.5	V
Data retention supply current	ICCDR1	Vcc = 3.0V, Vcε ≥ 2.8V	0 to +70°C			З	μA
			0 to +40°C			0.6	
			25°C		0.1	0.3	
	ICCDR2	Vcc = 2.0 to 5.5V,				5	
		Vce≥Vcc–0.2V			0.2		μA
CE setup time	t _{CDR}			0			ns
CE hold time	t _R			t _{RC**}			ns

Data Retention Characteristics at Ta = 0 to $+70^{\circ}C$

* Reference values at VCC = 5V, Ta = 25° C ** t_{RC} = Read Cycle time

Data Retention Waveform



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of March, 1996. Specifications and information herein are subject to change without notice.