



LC3564B, BS, BM, BT-70/10

64K (8192-word × 8-bit) SRAM with \overline{OE} , $\overline{CE1}$, and CE2 Control Pins

Overview

The LC3564B, LC3564BS, LC3564BM, and LC3564BT are 8192-word × 8-bit asynchronous silicon gate CMOS SRAMs. These are full CMOS type SRAMs that adopt a six-transistor memory cell and feature fast access times, low operating power dissipation, and an ultralow standby current. These SRAMs provide three control signal inputs: an \overline{OE} input for high-speed memory access, and two chip enable lines, $\overline{CE1}$ and CE2, for low power mode and device selection. These means that these SRAMs are ideal for systems that require low power and battery backup, and that they support easy memory expansion. The ultralow standby current that is a feature of these SRAMs allows them to be used with capacitor backup as well. Since these SRAMs support 3-V operation, they are also appropriate for use in portable battery operated systems.

Features

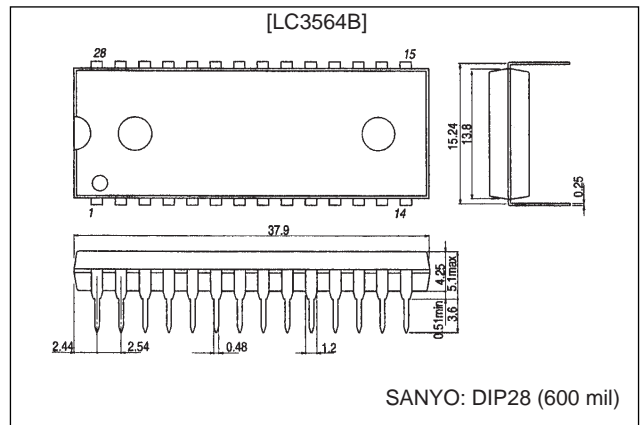
- Supply voltage range: 2.7 to 5.5 V
 - In 5-V operation mode: 5.0 V ±10%
 - In 3-V operation mode: 3.0 V ±10%
- Address access time (t_{AA})
 - In 5-V operation mode:
 - LC3564B, BS, BM, and BT-70: 70 ns (max)
 - LC3564B, BS, BM, and BT-10: 100 ns (max)
 - In 3-V operation mode:
 - LC3564B, BS, BM, and BT-70: 200 ns (max)
 - LC3564B, BS, BM, and BT-10: 500 ns (max)
- Ultralow standby current
 - In 5-V operation mode: 1.0 μ A ($T_a \leq 70^\circ\text{C}$),
3.0 μ A ($T_a \leq 85^\circ\text{C}$)
 - In 3-V operation mode: 0.8 μ A ($T_a \leq 70^\circ\text{C}$),
2.5 μ A ($T_a \leq 85^\circ\text{C}$)
- Operating temperature range
 - In 5-V operation mode: -40 to 85°C
 - In 3-V operation mode: -40 to 85°C
- Data retention supply voltage: 2.0 to 5.5 V
- All input and output levels:
 - In 5-V operation mode: TTL compatible levels
 - In 3-V operation mode: $V_{CC} - 0.2$ V/0.2 V

- Three control inputs: \overline{OE} , $\overline{CE1}$, and CE2
- Shared input and output pins, three-state outputs
- No clock required
- Packages
 - 28-pin DIP (600 mil) plastic package: LC3564B
 - 28-pin DIP (300 mil) plastic package: LC3564BS
 - 28-pin SOP (450 mil) plastic package: LC3564BM
 - 28-pin TSOP (8 × 13.4 mm) plastic package: LC3564BT

Package Dimensions

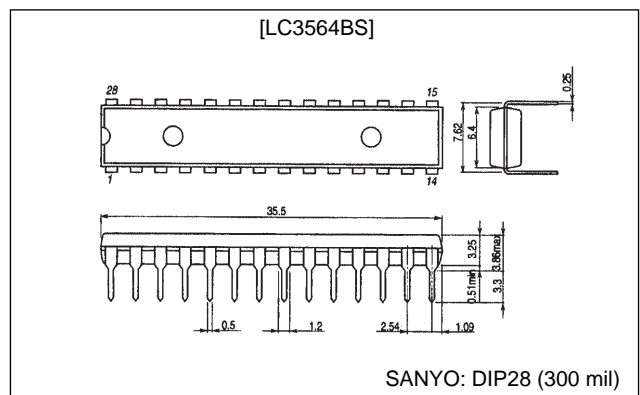
unit: mm

3012A-DIP28 (600 mil)



unit: mm

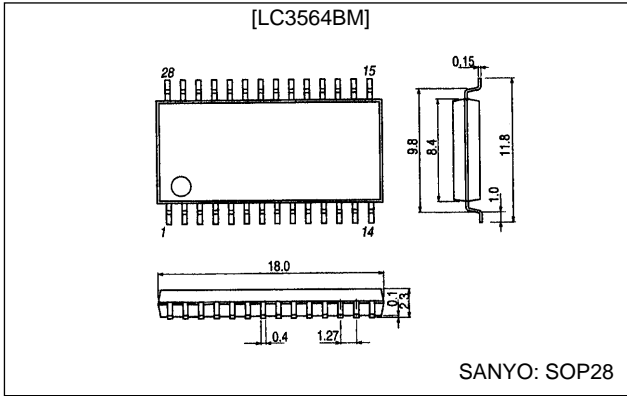
3133-DIP28 (300 mil)



LC3564B, BS, BM, BT-70/10

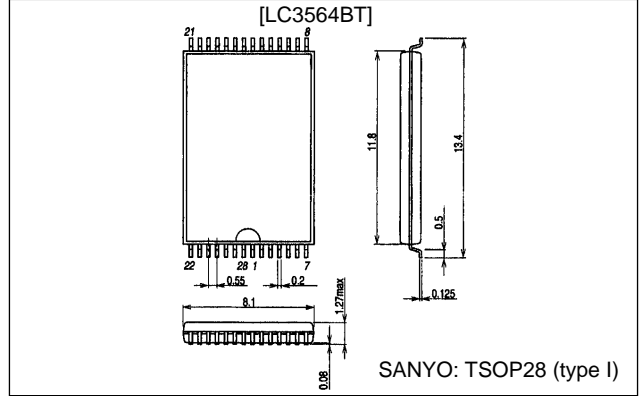
unit: mm

3187-SOP28

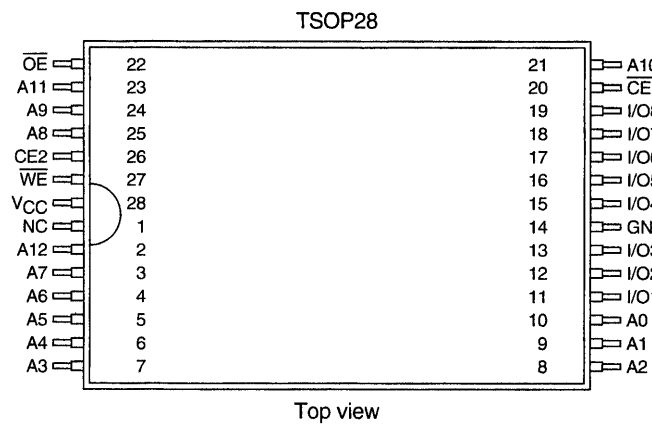
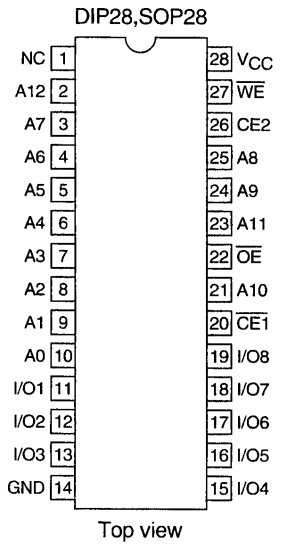


unit: mm

3221-TSOP28 (type I)

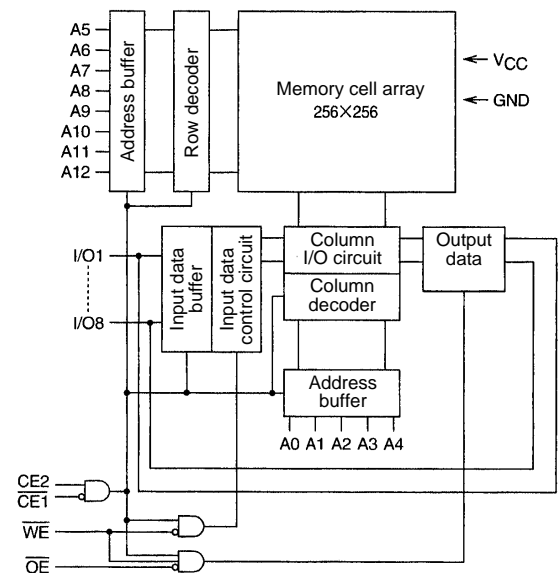


Pin Assignments



A09262

Block Diagram



A09263

Pin Functions

A0 to A12	Address inputs
\overline{WE}	Read/write control input
\overline{OE}	Output enable input
$\overline{CE1}$, $\overline{CE2}$	Chip enable inputs
I/O1 to I/O8	Data I/O
V _{CC} , GND	Power supply and ground

Function Table

Mode	$\overline{CE1}$	$\overline{CE2}$	\overline{OE}	\overline{WE}	I/O	Supply current
Read cycle	L	H	L	H	Data output	I _{CCA}
Write cycle	L	H	X	L	Data input	I _{CCA}
Output disable	L	H	H	H	High impedance	I _{CCA}
Not selected	H	X	X	X	High impedance	I _{CCS}
	X	L	X	X	High impedance	I _{CCS}

X : H or L

LC3564B, BS, BM, BT-70/10

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Input voltage	V_{IN}		-0.3^* to $V_{CC} + 0.3$	V
I/O voltage	V_{IO}		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}		-40 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to $+125$	$^\circ\text{C}$

Note: For pulse widths less than 30 ns: -3.0 V

Input and Output Capacitances at $T_a = 25^\circ\text{C}$, $f = 1$ MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0$ V		6	10	pF
Input pin capacitance	C_{IN}	$V_{IN} = 0$ V		6	10	pF

Note: These parameters are sampled, and are not measured for every unit.

[5-V Operation]

DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		4.5	5.0	5.5	V
Input voltage	V_{IH}		2.2		$V_{CC} + 0.3$	V
	V_{IL}		-0.3^*		$+0.8$	V

Note: For pulse widths less than 30 ns: -3.0 V

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ *	max		
Input leakage current	I_{LI}	$V_{IN} = 0$ to V_{CC}	-1.0		$+1.0$	μA	
I/O leakage current	I_{LO}	$V_{\overline{CE}1} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$, $V_{I/O} = 0$ to V_{CC}	-1.0		$+1.0$	μA	
Output high-level voltage	V_{OH}	$I_{OH} = -1.0$ mA	2.4			V	
Output low-level voltage	V_{OL}	$I_{OL} = 2.0$ mA			0.4	V	
Operating supply current	$V_{CC} - 0.2$ V/0.2 V inputs	I_{CCA1}	$V_{\overline{CE}1} \leq 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V, $I_{I/O} = 0$ mA, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V	$T_a \leq 70^\circ\text{C}$	0.01	1.0	μA
			$T_a \leq 85^\circ\text{C}$		3.0		
		I_{CCA4}	$V_{\overline{CE}1} \leq 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V, $I_{I/O} = 0$ mA, DUTY = 100%	min cycle	LC3564B,BS,BM,BT-70		35
	1 μs cycle			LC3564B,BS,BM,BT-10		30	
	TTL inputs	I_{CCA2}	$V_{\overline{CE}1} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O} = 0$ mA, $V_{IN} = V_{IH}$ or V_{IL}			7	mA
						7	
I_{CCA3}		$V_{\overline{CE}1} = V_{IL}$, $V_{CE2} = V_{IH}$, $I_{I/O} = 0$ mA, DUTY = 100%	min cycle	LC3564B,BS,BM,BT-70		40	mA
1 μs cycle	LC3564B,BS,BM,BT-10		35				
Standby mode supply current	$V_{CC} - 0.2$ V/0.2 V inputs	I_{CCS1}	$V_{CE2} \leq 0.2$ V or $V_{\overline{CE}1} \geq V_{CC} - 0.2$ V, $V_{CE2} \geq V_{CC} - 0.2$ V	$T_a \leq 70^\circ\text{C}$	0.01	1.0	μA
			$T_a \leq 85^\circ\text{C}$		3.0		
	TTL inputs	I_{CC2}	$V_{CE2} = V_{IL}$ or $V_{\overline{CE}1} = V_{IH}$, $V_{IN} = 0$ to V_{CC}			2.0	mA

Note *: Reference values at $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$

LC3564B, BS, BM, BT-70/10

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 4.5$ to 5.5 V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	$V_{IH} = 2.4$ V, $V_{IL} = 0.6$ V
Input rise and fall times	5 ns
Input and output timing level	1.5 V
Output load	LC3564B, BS, BM, and BT-70: 30 pF + 1 TTL gate (Including the jig capacitance.)
	LC3564B, BS, BM, and BT-10: 100 pF + 1 TTL gate (Including the jig capacitance.)

Read Cycle

Parameter	Symbol	LC3564B, BS, BM, BT				Unit
		-70		-10		
		min	max	min	max	
Read cycle time	t_{RC}	70		100		ns
Address access time	t_{AA}		70		100	ns
$\overline{CE1}$ access time	t_{CA1}		70		100	ns
CE2 access time	t_{CA2}		70		100	ns
\overline{OE} access time	t_{OA}		35		50	ns
Output hold time	t_{OH}	10		10		ns
$\overline{CE1}$ output enable time	t_{COE1}	10		10		ns
CE2 output enable time	t_{COE2}	10		10		ns
\overline{OE} output enable time	t_{OOE}	5		5		ns
$\overline{CE1}$ output disable time	t_{COD1}		30		35	ns
CE2 output disable time	t_{COD2}		30		35	ns
\overline{OE} output disable time	t_{OOD}		25		25	ns

Write Cycle

Parameter	Symbol	LC3564B, BS, BM, BT				Unit
		-70		-10		
		min	max	min	max	
Write cycle time	t_{WC}	70		100		ns
Address setup time	t_{AS}	0		0		ns
Write pulse width	t_{WP}	50		55		ns
$\overline{CE1}$ setup time	t_{CW1}	60		65		ns
CE2 setup time	t_{CW2}	60		65		ns
Write recovery time	t_{WR}	0		0		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		ns
CE2 write recovery time	t_{WR2}	0		0		ns
Data setup time	t_{DS}	35		40		ns
Data hold time	t_{DH}	0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		ns
CE2 data hold time	t_{DH2}	0		0		ns
\overline{WE} output enable time	t_{WOE}	5		5		ns
\overline{WE} output disable time	t_{WOD}		30		35	ns

LC3564B, BS, BM, BT-70/10

[3-V Operation]

DC Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		2.7	3.0	3.3	V
Input voltage	V_{IH}		$V_{CC} - 0.2$		V_{CC}	V
	V_{IL}		0		0.2	V

DC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3 V

Parameter	Symbol	Conditions	Ratings			Unit		
			min	typ *	max			
Input leakage current	I_{LI}	$V_{IN} = 0$ to V_{CC}	-1.0		+1.0	μA		
I/O leakage current	I_{LO}	$\overline{V_{CE1}} = V_{IH}$ or $V_{CE2} = V_{IL}$ or $\overline{V_{OE}} = V_{IH}$ or $\overline{V_{WE}} = V_{IL}$, $V_{I/O} = 0$ to V_{CC}	-1.0		+1.0	μA		
Output high-level voltage	V_{OH}	$I_{OH} = -0.5$ mA	$V_{CC} - 0.2$			V		
Output low-level voltage	V_{OL}	$I_{OL} = 1.0$ mA			0.2	V		
Operation supply current	I_{CCA1}	$\overline{V_{CE1}} \leq V_{IL}$, $V_{CE2} \geq V_{IH}$, $I_{I/O} = 0$ mA, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$	$T_a \leq 70^\circ\text{C}$		0.01	0.8	μA	
			$T_a \leq 85^\circ\text{C}$			2.5		
	I_{CCA4}	$\overline{V_{CE1}} \leq V_{IL}$, $V_{CE2} \geq V_{IH}$, $I_{I/O} = 0$ mA, DUTY = 100%	min cycle	LC3564B,BS, BM, BT-70			20	mA
			1 μs cycle	LC3564B,BS, BM, BT-10			10	
Standby mode supply current	I_{CCS1}	$V_{CE2} \leq 0.2$ V or $\overline{V_{CE1}} \geq V_{IH}$ $V_{CE2} \geq V_{IH}$	$T_a \leq 70^\circ\text{C}$		0.01	0.8	μA	
			$T_a \leq 85^\circ\text{C}$			2.5		

Note *: Reference values at $V_{CC} = 3$ V, $T_a = 25^\circ\text{C}$

LC3564B, BS, BM, BT-70/10

AC Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 2.7$ to 3.3 V

Parameter	Conditions
[AC Test Conditions]	
Input pulse voltage	$V_{IH} = V_{CC} - 0.2$ V, $V_{IL} = 0.2$ V
Input rise and fall times	10 ns
Input and output timing level	1.5 V
Output load	LC3564B, BS, BM, BT-70 : 30pF (Including the jig capacitance.)
	LC3564B, BS, BM, BT-10 : 100pF (Including the jig capacitance.)

Read Cycle

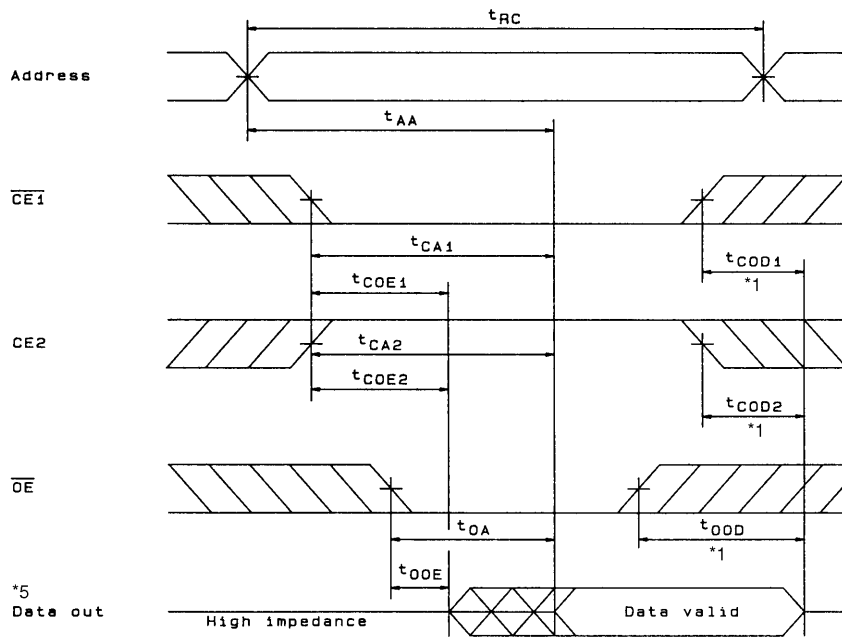
Parameter	Symbol	LC3564B, BS, BM, BT				Unit
		-70		-10		
		min	max	min	max	
Read cycle time	t_{RC}	200		500		ns
Address access time	t_{AA}		200		500	ns
$\overline{CE1}$ access time	t_{CA1}		200		500	ns
CE2 access time	t_{CA2}		200		500	ns
\overline{OE} access time	t_{OA}		100		250	ns
Output hold time	t_{OH}	20		20		ns
$\overline{CE1}$ output enable time	t_{COE1}	20		20		ns
CE2 output enable time	t_{COE2}	20		20		ns
\overline{OE} output enable time	t_{OOE}	10		10		ns
$\overline{CE1}$ output disable time	t_{COD1}		60		120	ns
CE2 output disable time	t_{COD2}		60		120	ns
\overline{OE} output disable time	t_{OOD}		50		100	ns

Write Cycle

Parameter	Symbol	LC3564B, BS, BM, BT				Unit
		-70		-10		
		min	max	min	max	
Write cycle time	t_{WC}	200		500		ns
Address setup time	t_{AS}	0		0		ns
Write pulse width	t_{WP}	140		200		ns
$\overline{CE1}$ setup time	t_{CW1}	150		250		ns
CE2 setup time	t_{CW2}	0		250		ns
Write recovery time	t_{WR}	0		0		ns
$\overline{CE1}$ write recovery time	t_{WR1}	0		0		ns
CE2 write recovery time	t_{WR2}	130		0		ns
Data setup time	t_{DS}	0		180		ns
Data hold time	t_{DH}	0		0		ns
$\overline{CE1}$ data hold time	t_{DH1}	0		0		ns
CE2 data hold time	t_{DH2}	10		0		ns
\overline{WE} output enable time	t_{WOE}			10		ns
\overline{WE} output disable time	t_{WOD}		60		120	ns

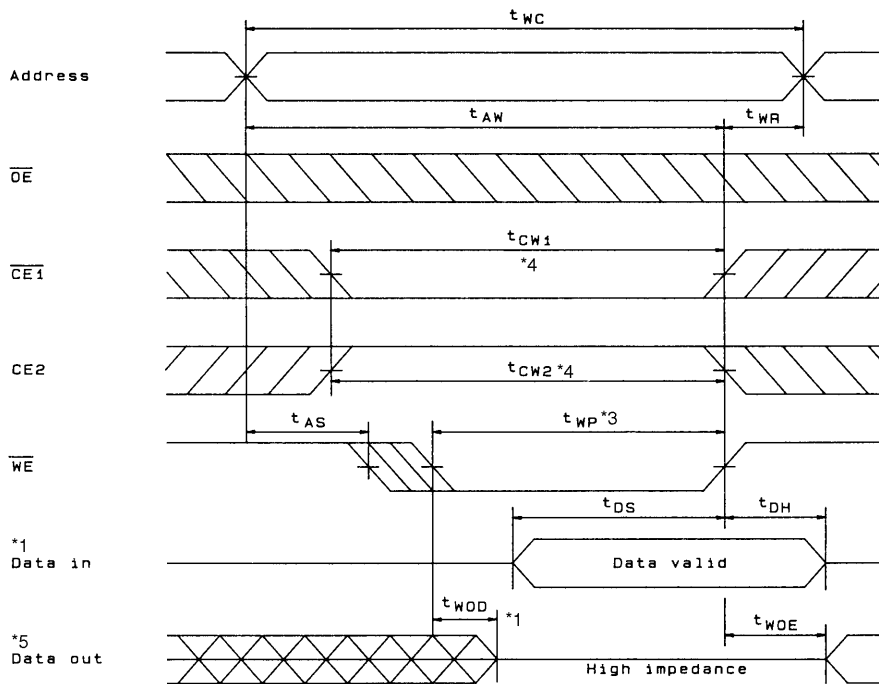
Timing Charts

Read Cycle *1



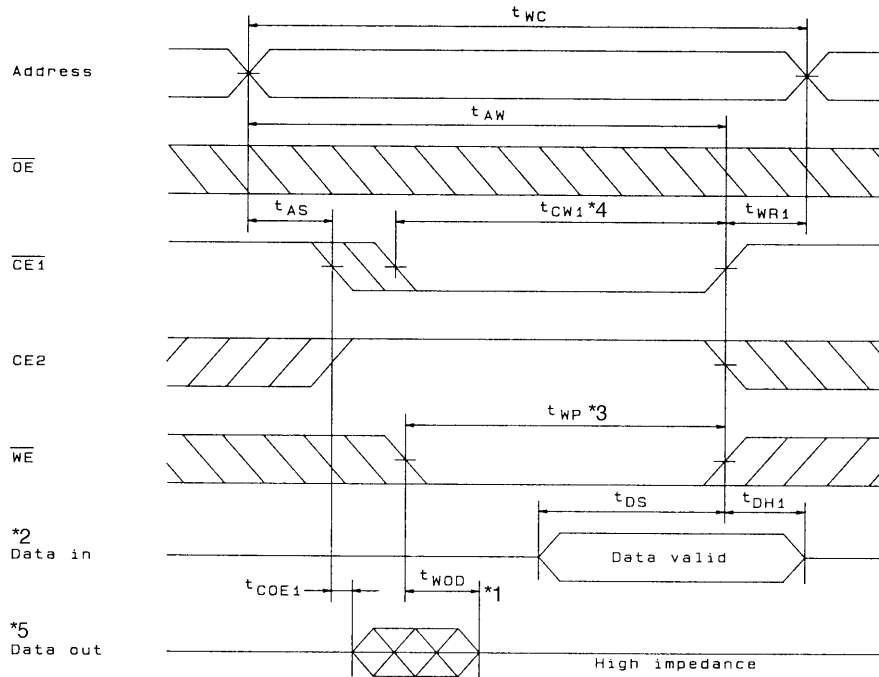
A05775

Write Cycle (1): \overline{WE} Write *6



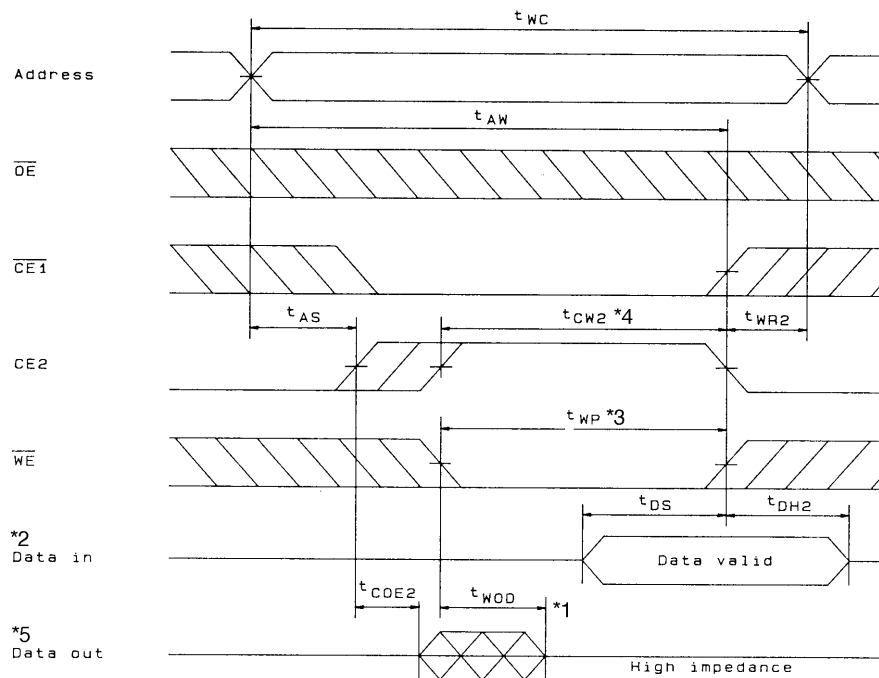
A05776

Write Cycle (2): $\overline{\text{CE1}}$ Write *6



A05777

Write Cycle (3): $\overline{\text{CE2}}$ Write *6



A05778

- Notes:
1. Hold $\overline{\text{WE}}$ high during the read cycle.
 2. Applications must not apply reverse phase signals to the D_{OUT} pins when those pins are in the output state.
 3. The time t_{WP} is the period when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low and CE2 is high, and is defined as the time from the fall of $\overline{\text{WE}}$ until either $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ rises, or CE2 falls, whichever occurs first.
 4. The times t_{CW1} and t_{CW2} are periods when $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are low and CE2 is high. They are defined as the times from the fall of $\overline{\text{CE1}}$ or the rise of CE2 to the rise of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$, or the fall of CE2, whichever occurs first.
 5. The D_{OUT} pins will be in the high-impedance state if either $\overline{\text{OE}}$ is high, $\overline{\text{CE1}}$ is high, CE2 is low, or $\overline{\text{WE}}$ is low.
 6. $\overline{\text{OE}}$ must be held either at V_{IH} or V_{IL} during the write cycle.
 7. The D_{OUT} pins have the same phase as the write cycle write data.

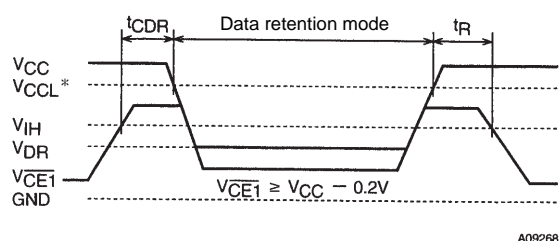
LC3564B, BS, BM, BT-70/10

Data Retention Characteristics at $T_a = -40$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Data retention supply voltage	V_{DR}	$V_{CE2} \leq 0.2\text{ V}$ or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$, $V_{CE2} \geq V_{CC} - 0.2\text{ V}$	2.0		5.5	μA
Data retention supply current	I_{CCDR}	$V_{CC} = 3\text{ V}$, $V_{CE2} \leq 0.2\text{ V}$, or $V_{CE1} \geq V_{CC} - 0.2\text{ V}$, $V_{CE2} \geq V_{CC} - 0.2\text{ V}$			0.8	μA
		$T_a \leq 70^\circ\text{C}$			2.5	
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}^*			ns

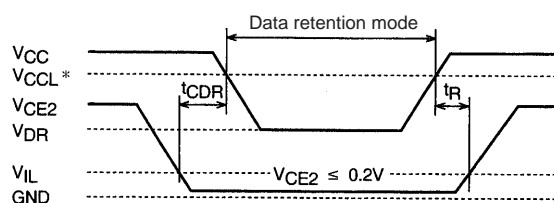
Note *: t_{RC} is the read cycle time.

Data Retention Waveforms (1): CE1 Control



A09268

Data Retention Waveforms (2): CE2 Control



A09269

Note *: In 5-V operation: 4.5 V
In 3-V operation: 2.7 V

Notes on Circuit Design

When actually design a circuit using these devices, take the following points into consideration and design the circuit so that none of the maximum rating items are ever exceeded.

- Variations in the supply voltage
- Variations in the electrical characteristics of components such as semiconductor devices, resistors, and capacitors.
- Ambient temperature
- Variations in input and clock signals
- Possible application of abnormal pulses

Also, these devices must be operated within the ranges stipulated in the allowable operating ranges.

If CMOS IC input pins are left open, intermediate potential input voltages may occur leading to incorrect operation due to through currents or other phenomenon. Applications must handle unused input pins appropriately.

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of May, 1998. Specifications and information herein are subject to change without notice.