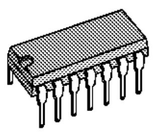
L3281

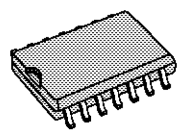
LOW VOLTAGE TELEPHONE SPEECH CIRCUITS

PRELIMINARY DATA

- OPERATION DOWN TO 1.6V / 6.5mA
- DTMF & BEEP TONE INPUTS
- EXTERNAL MUTING FOR EARPHONE AND MICROPHONE
- SUITABLE FOR DYNAMIC EARPHONE AND DYNAMIC OR ELECTRET MICROPHONE
- AGC CONTROL ON BOTH SENDING AND RECEIVING



DIP14



SO14

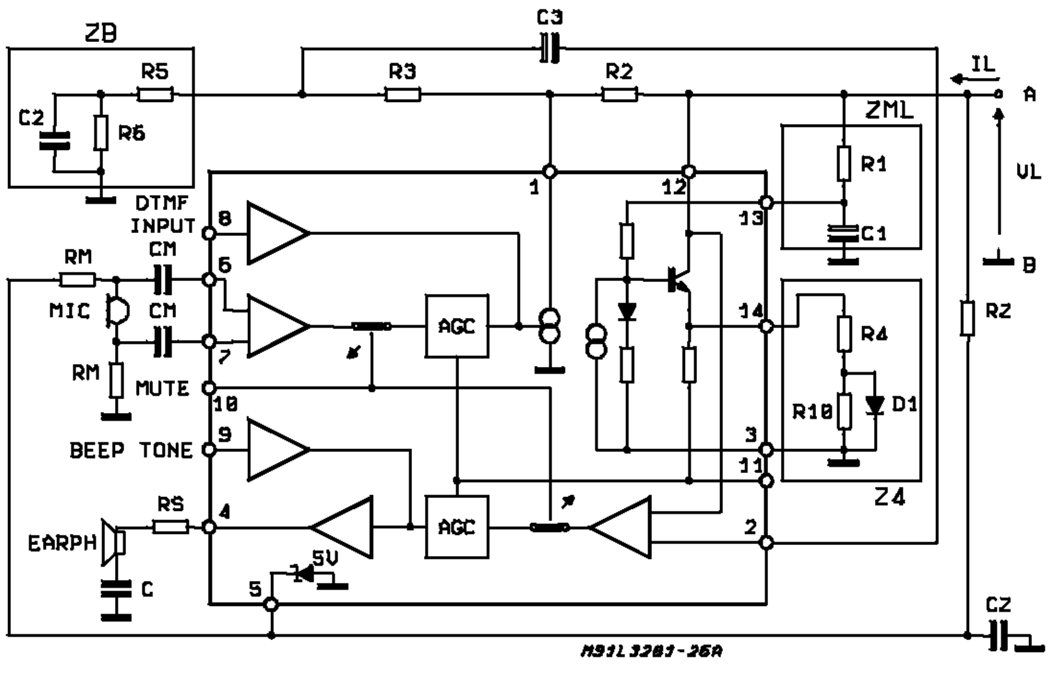
ORDERING NUMBERS:

L3281AB L3281AD1

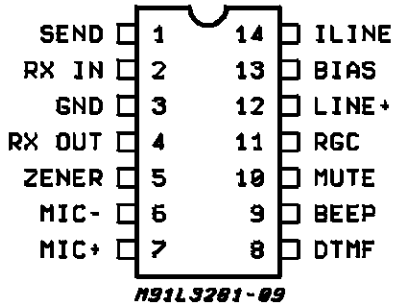
DESCRIPTION

The L3281 is an electronic speech circuit developed to replace hybrid circuits in telephone sets that can be operated in parallel with other phones.

BLOCK DIAGRAM



PIN CONNECTION (top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		DIP-14	SO-14	
V_L	Line Voltage (3 ms pulse)	15		V
I_L	Line Current	150		mA
P_{tot}	Total Power Dissipation, T_{amb} = 55°C	1.0	0.6	W
T_{op}	Operating Temperature	– 20 to 55		°C
T_j	Junction Temperature	– 65 to 150		°C

THERMAL DATA

Symbol	Parameter	Value		Unit
		DIP-14	SO-14	
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction Ambient Max	90	130	°C/W

TEST CIRCUITS

Figure 1.

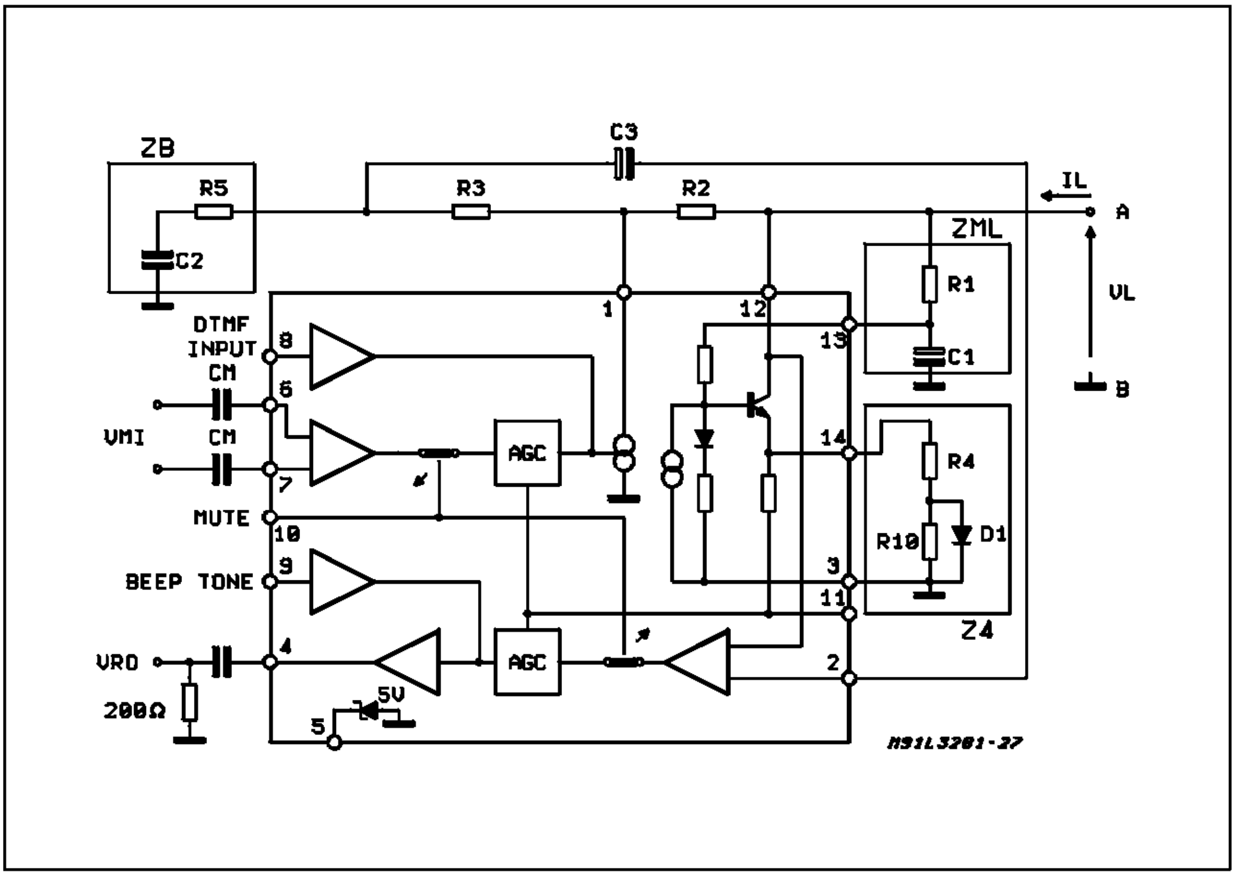


Figure 2.

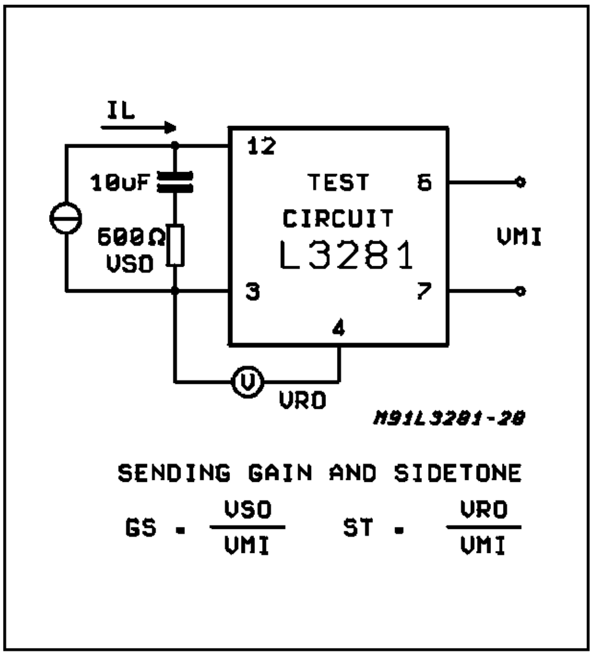
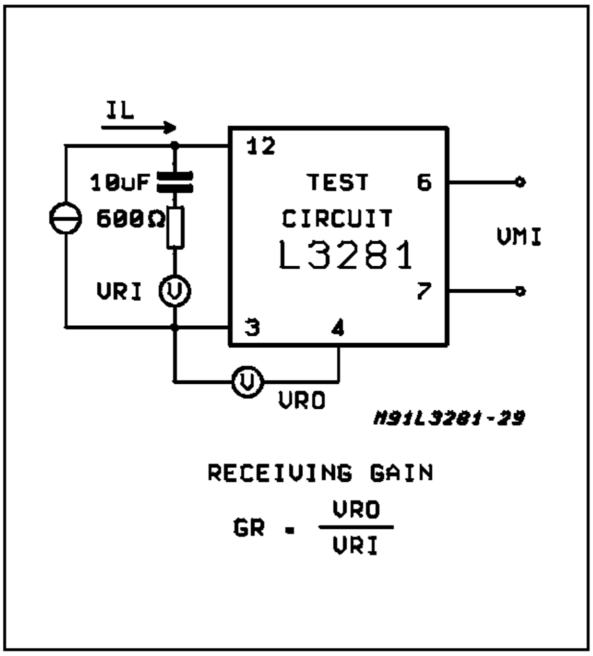


Figure 3.



ELECTRICAL CHARACTERISTICS I_L = 20 to 100mA; R4 =(51Ω // diode) + 33Ω;
T = 25°C; f = 1kHz; Unless Otherwise Specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_l	Line Voltage	I_L = 6.5mA I_L = 20mA I_L = 50mA I_L = 80mA		1.65 3.4 6.0 8	 3.7 6.5 9.5	V V V V
CMRR	Common Mode Rej. Ratio		50			dB
G_{tx}	Sending Gain	V_{mi} = 10mV; I_L = 20mA	30	31.5	33	dB
DG_{tx}	Delta Sending Gain	V_{mi} = 10mV; I_L = 70mA	– 7.2	–5.7	–4.2	dB
THD_{tx}	Sending Distortion	V_{so} = 700mV; I_L = 20mA			5	%
N_{tx}	Sending Noise	V_{mi} = 0V; I_L = 50mA		– 70		dB
Z_{ml}	Mic. Input Impedance	V_{mi} = 10mV	40			kΩ
G_{rx}	Receiving Gain	I_L = 20mA; V_{ri} = 0.2V	– 10.7	– 9.2	– 7.7	dB
DG_{rx}	Delta Receiving Gain	I_L = 70mA; V_{ri} = 0.2V	– 7.2	– 5.7	– 4.2	dB
THD_{rx}	Receiving Distortion	V_{ro} = 350mV; Load = 350Ω V_{ro} = 300mV; I_L = 10 mA			5 5	% %
N_{rx}	Receiving Noise	V_{ri} = 0V		100		µV
Z_{ro}	Rec. Output Impedance	Load = 200Ω; V_{ro} = 50V		10		Ω
	Sidetone	V_{mi} = 10mV		10	20	dB
Z_m	Line Match. Impedance	V_{ri} = 0.2V	500	600	700	Ω
V_{so}	Sending Output Voltage	I_L = 6.5mA; THD = 5%	100			mV
I_{ro}	Receiving Output Current	I_L = 6.5mA; THD = 5%	0.5			mAp
MU_{lo}	Mute Input Low	Dialing Mode		50	100	µA
MU_{hl}	Mute Input Open	Speaking Mode			1	µA
G_{mf}	DTMF Gain	$V_{mf\ IN}$ = 10mV	14.5	16	17.5	dB
R_{mf}	DTMF Input Impedance		5	10		kΩ
THD_{mf}	DTMF Distortion	$V_{mf\ LN}$ = 140mV			5	%
G_{beep}	Beeptone Gain	$V_{beep\ IN}$ = 25mV		8.5		dB
R_{beep}	Beeptone Input Impedance		5.5	8		kΩ
THD_{beep}	Beeptone Distortion	$V_{beep\ IN}$ = 100mV; I_L = 20mA		0.5	5	%
V_z	Zener Voltage (Pin 5)	I_z = 1 mA	4.2	5.1	6.2	V
I_{leak}	Leakage Current,V_{pin5} = 3V			20		µA

LOGIC OF MUTE SWITCHING

MUTE	DTMF	BEEP	MIC IMP	RX IMP
LOW (DIAL)	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	MUTED	MUTED
OPEN (SPEECH)	ACTIVE TO LINE OUTPUT	ACTIVE TO EARPHONE OUTPUT	ACTIVE	ACTIVE

CIRCUIT DESCRIPTION

TWO TO FOUR WIRE CONVERSION

The L3281AB is based on a Wheastone bridge configuration. To balance the bridge the following relation must be satisfied:

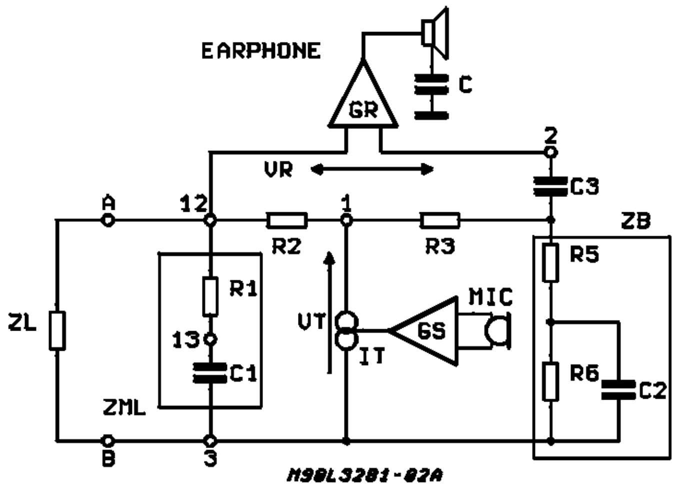
$$\frac{Zl\ //\ Zm}{Zb} = \frac{R2}{R3}$$

The AC signal from the microphone is sent to one diagonal of the bridge (pins 1 and 3). A small percentage of the signal power is lost on Zb (being Zb > (Zm//Zi)); the main part is sent to the line via R2.

In receiving mode, the AC signal coming from the LINE is sensed across the second diagonal of the bridge (pins 12 and 2).

The impedance Zm and Zb can be complex.

Figure 4: 2/4 Wire Conversion



DC CHARACTERISTIC

The fig.5 shows the equivalent simplified circuit of the DC regulator that provides to give the opportune DC impedance Zdc.

$$VL = \left[\frac{Idc \cdot Z4}{RB} \cdot (RA + RB)\right] + VD + VR1$$

$$VL = \left[(Idc \cdot Z4) \cdot \left(\frac{RA}{RB} + 1\right)\right] + VD + VR1$$

since RA = RB

$$VL = (Idc \cdot Z4 \cdot 2) + VD + VR1$$

When IL 18 mA and considering neglectible the VD + VR1 variation versus line current :

$$ZDC = \frac{\Delta\ VL}{\Delta\ Idc} = 2 \cdot Z4$$

At IL = 6.5 mA no current flows through Z4 but only in the rest of the circuit for internal biasing (Io;Ia). The bias current Io is fixed by the resistor R2. The line voltage in this case is :

$$VL = Ia\ RA + VR1 = 1.6\ V$$

The Fig.6 shows the DC characteristic (voltage between pin 12 and pin 3 versus line current). The device own an equivalent zener voltage at pin 5 that can be used as supply voltage for electret microphone (see Block Diagram).

The value of the resistor R2 and the capacitor C2 should be chosen in order to not affect the AC line inpedance. The Fig.7 shows the zener equivalent.

The zener voltage will be:

$$Vz = \left(\frac{70K}{13.6K} + 1\right) \cdot Vbe$$

It is possible to supply 1mA to the electrete voltage if VL > (1mA + Iz) · Rz + Vz

Figure 6: Low Voltage Speech Circuit.

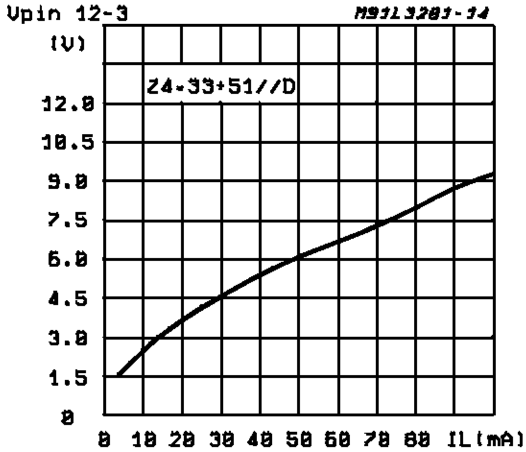


Figure 7: Zener Equivalent.

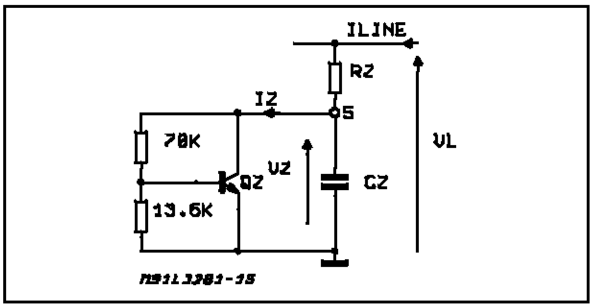
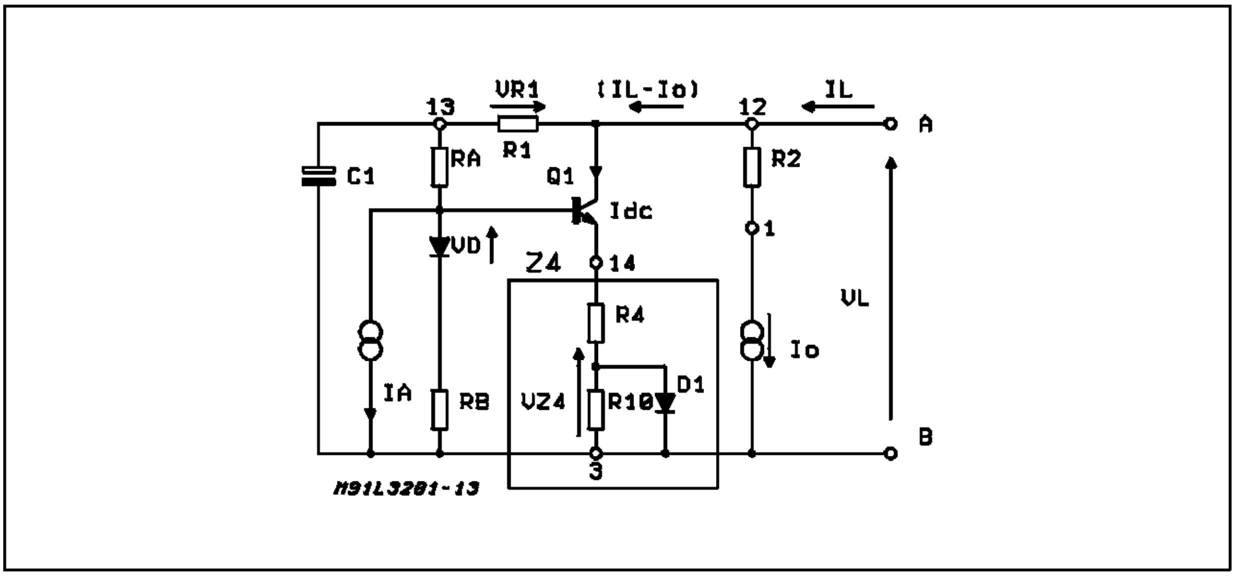


Figure 5: Equivalent Simplified Circuit



AC CHARACTERISTIC

The AC Impedance measured at line terminals is equal to:

$$Zm = (R1 + \frac{1}{jwC1}) // (R2 + R3 + Zb)$$

The value of the capacitor C1 must be In the range of 22 µF to 100 µF.

The external resistor R1 can be replaced by a resistor/capacitor network in order to realize a complex Impedance Zm.

TRANSMITTING CIRCUIT

The first block of the TX stage is basically a differential amplifier which converts voltage to current. The inputs are internally polarized at 300 mVdc. The differential Input impedance is 60 KΩ to allow a good matching to microphone. The AGC in TX is function of voltage at pin 14 in order to decrease to max gain of 5.5dB to 6.0dB when the line current increases.

RECEIVING CIRCUIT

Fig.9 shows the equivalent receiving circuit. The differential input of RX signal across R2+R3 is transferred to the AGC block when the mute signal (pin 10) is not active.

The AGC in RX is a function of the voltage at pin 14 and decreases the gain when the line current increases (5.5dB to 6.0dB).

The final stage is a single ended amplifier with low output impedance optimized to drive magnetic/dynamic transducers.

Figure 8: Equivalent Transmitting Circuit.

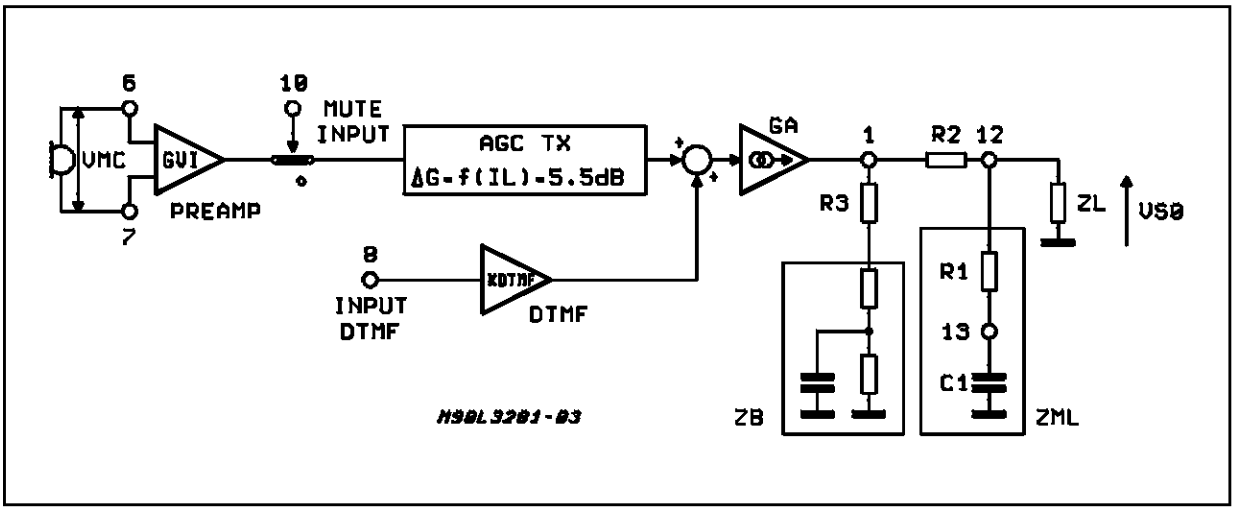
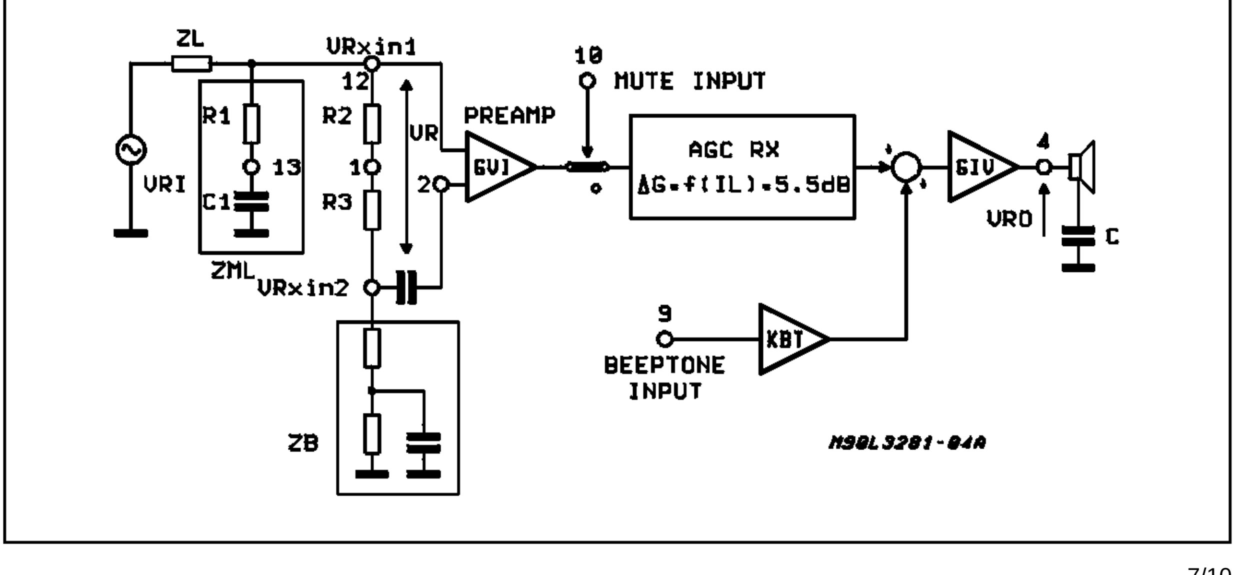
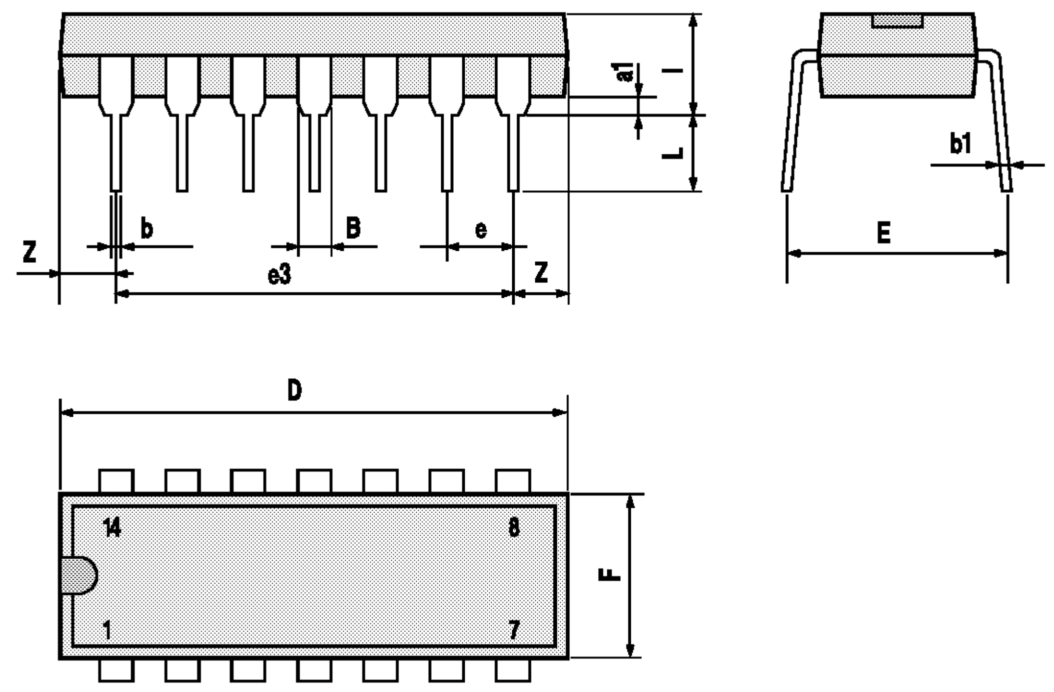


Figure 9: Equivalent Receiving Circuit.



DIP14 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



SO14 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.15		0.157
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)