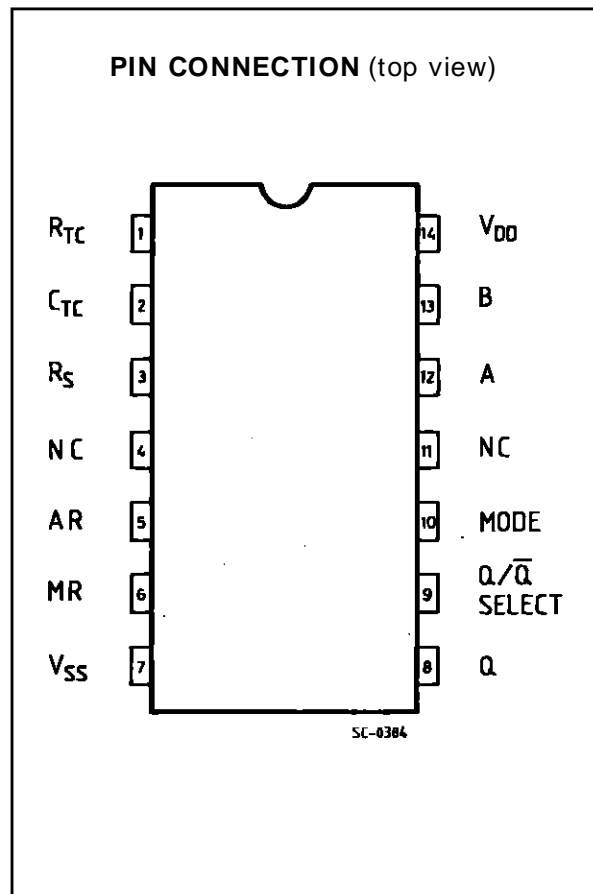
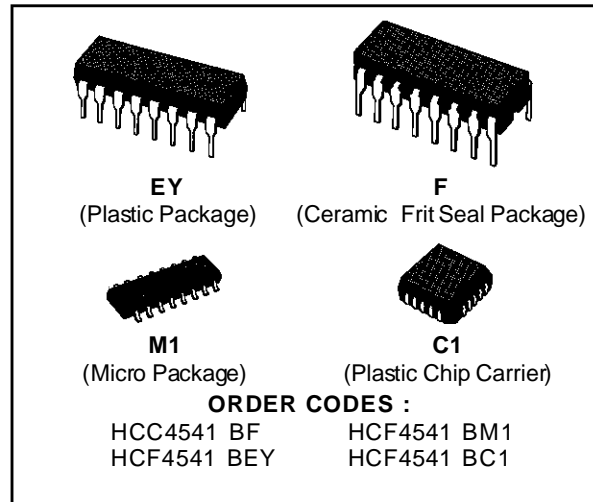


## PROGRAMMABLE TIMER

- 16 STAGE BINARI COUNTER
- LOW SYMMETRICAL OUTPUT RESISTANCE, TYPICALLY 100 OHM AT  $V_{DD} = 15V$
- OSCILLATOR FREQUENCY RANGE : DC TO 100kHz
- AUTO OR MASTER RESET DISABLES OSCILLATOR DURING RESET TO REDUCE POWER DISSIPATION
- OPERATES WITH VERY SLOW CLOCK RISE AND FALL TIMES
- BUILT-IN LOW-POWER RC OSCILLATOR
- EXTERNAL CLOCK (applied to pin 3) CAN BE USED INSTEAD OF OSCILLATOR
- OPERATES AS  $2^N$  FREQUENCY DIVIDER OR AS A SINGLE-TRANSITION TIMER
- $Q/\bar{Q}$  SELECT PROVIDES OUTPUT LOGIC LEVEL FLEXIBILITY
- CAPABLE OF DRIVING SIX LOW POWER TTL LOADS, THREE LOW-POWER SCHOTTKY LOADS, PR SIX HTL LOADS OVER THE RATED TEMPERATURE RANGE
- SYMMETRICAL OUTPUT CHARACTERISTICS
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- 5-10-15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF 'B' SERIES CMOS DEVICES"

### DESCRIPTION

The **HCC/HCF4541B** Programmable Timer is composed of a 16-stage binary counter, an oscillator controlled by 2 external resistors and a capacitor, an output control logic and an automatic power-on reset circuit. The counter varies on positive-edge clock transition and it can be cleared by the MASTER RESET input. The output from this timer is the Q or  $\bar{Q}$  output from the 8th, 13th, or 16th counter stage. The choice of the stage depends on the time-select inputs A or B (see frequency selection table). The output is available in one of the two modes that can be selected via the MODE input, pin 10 (see truth table). The output turns out as a continuous square wave, with a frequency equal to the oscillator frequency divided by  $2^N$ . When this MODE input is



## HCC/HCF4541B

a logic "1", when it is a logic "0" and after a MASTER RESET is started, and Q output has been selected, the output goes up to a high state after  $2^{N-1}$  counts. It remains in that state till another MASTER RESET pulse is apply or the mode input is a logic "1". The process starts by setting the AUTO RESET input (pin 5) to logic "0" and switching power on. If pin 5 is set to logic "1", the AUTO RESET circuit is not enabled and counting cannot start till a positive MASTER RESET pulse is applied, returning to a low level. The AUTO RESET consumes a remarkable

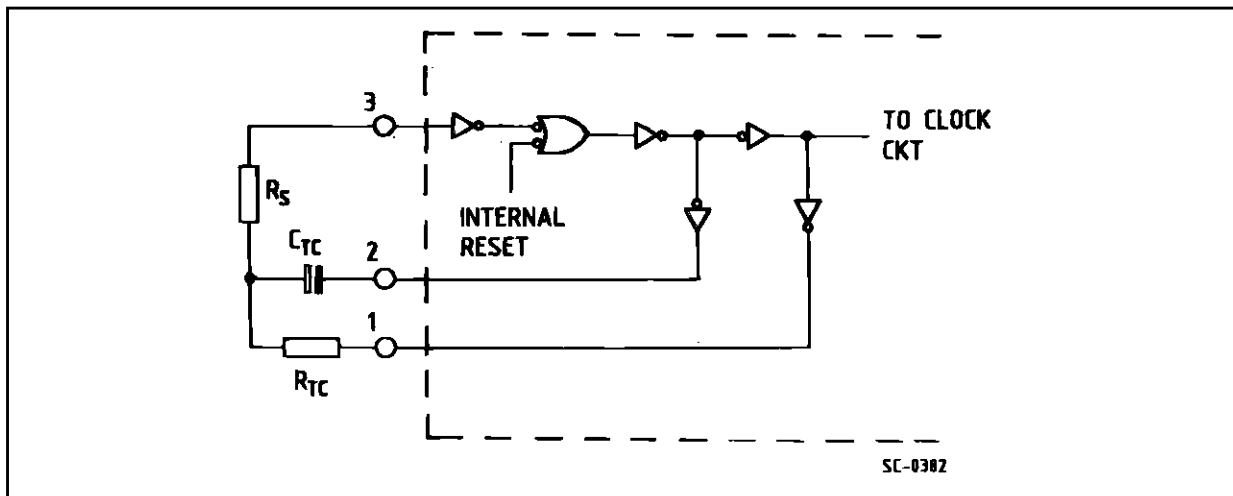
RC Oscillator Circuit.

amount of power and should not be used if low-power operation is wanted.

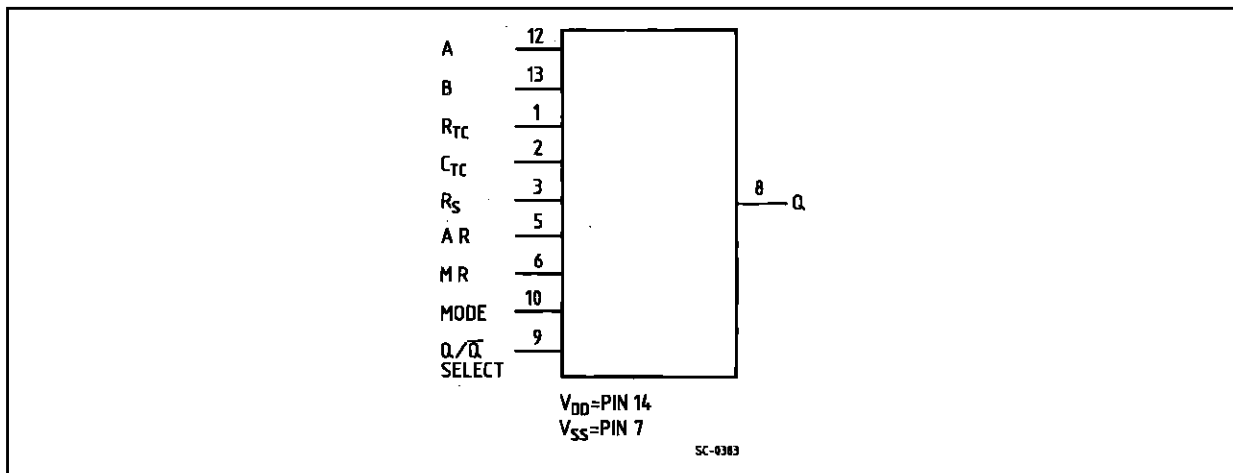
The frequency of the oscillator depends on the RC network. It can be calculated using the following formula:

$$f = \frac{1}{2.3 R_{TC} C_{TC}}$$

where f is between 1 kHz and 100 kHz  
and  $R_S \geq 10 \text{ k}\Omega$  and  $\approx 2 R_{TC}$



## FUNCTIONAL DIAGRAM





STATIC ELECTRICAL

Symbol	Parameter		Test Conditions				Value						Unit	
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub> ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>Low</sub>		25°C			T <sub>High</sub>		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	HCC Types	0/5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000		
		HCF Types	0/5			5		5		0.04	5		150	
			0/10			10		10		0.04	10		300	
0/15				15		20		0.04	20		600			
V <sub>OH</sub>	Output High Voltage	0/5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V <sub>OL</sub>	Output Low Voltage	5/0		< 1	5		0.05			0.05		0.05	V	
		10/0		< 1	10		0.05			0.05		0.05		
		15/0		< 1	15		0.05			0.05		0.05		
V <sub>IH</sub>	Input High Voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V <sub>IL</sub>	Input Low Voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I <sub>OH</sub>	Output Drive Current	HCC Types	0/5	4.6		5	-1.9		-1.55	-3.1		-1.08	mA	
			0/5	2.5		5	-6.2		-5	-10		-3		
			0/10	9.5		10	-5.0		-4	-8		-2.8		
			0/15	13.5		15	-12.6		-10	-20		-7.2		
		HCF Types	0/5	4.6		5	-1.85		-1.55	-3.1		-1.26		
			0/5	2.5		5	-6.0		-5	-10		-4.1		
			0/10	9.5		10	-4.8		-4	-8		-3.3		
0/15	13.5		15	-12		-10	-20		-8.4					
I <sub>OL</sub>	Output Sink Current	HCC Types	0/5	0.4		5	1.9		1.55	3.1		1.08	mA	
			0/10	0.5		10	5.0		4	8		2.8		
			0/15	1.5		15	12.6		10	20		7.2		
		HCF Types	0/5	0.4		5	1.85		1.55	3.1		1.26		
			0/10	0.5		10	4.8		4	8		3.3		
			0/15	1.5		15	12		10	20		8.4		
I <sub>IH</sub> , I <sub>IL</sub>	Input Leakage Current		0/18	Any Input	18		$\pm 0.1$		$\pm 0.1$ <sub>5</sub>	$\pm 0.1$		$\pm 1$	$\mu$ A	
C <sub>I</sub>	Input Capacitance			Any Input					5	7.5			pF	

\* T<sub>Low</sub> = - 55C for HCC device : - 40C for HCF device.

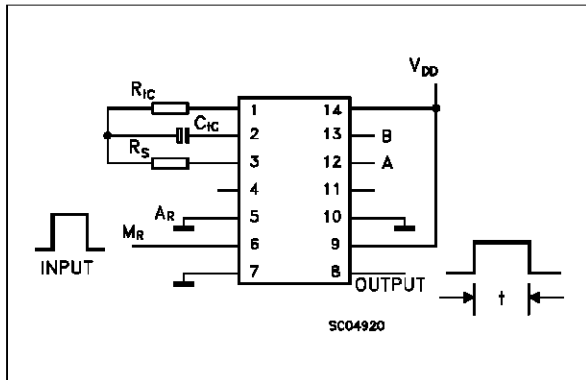
\* T<sub>High</sub> = + 125C for HCC device : + 85C for HCF device.

The Noise Margin for both " 1 " and " 0 " level is : 1V min. with V<sub>DD</sub> = 5V 2V min. with V<sub>DD</sub> = 10V 2.5V min. with V<sub>DD</sub> = 15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$ , typical temperature coefficient for all  $V_{DD}$  values is  $0.3\%/^{\circ}\text{C}$ , all input rise and fall time =  $20\text{ns}$ )

Symbol	Parameter	VDD (V)	Values			Unit
			Min.	Typ.	Max.	
$(2^8)$ $t_{PHL}$ $t_{PLH}$	Propagation Delay Time Clock to Q	5		3.5	10.5	$\mu\text{s}$
		10		1.25	3.8	
		15		0.9	2.9	
$(2^{16})$ $t_{PHL}$ $t_{PLH}$		5		6	18	$\mu\text{s}$
		10		3.5	10	
		15		2.5	7.5	
$t_{THL}$	Transition Time	5		100	200	ns
		10		50	100	
		15		40	80	
$t_{TLH}$		5		180	360	ns
		10		90	180	
		15		65	130	
	Master Reset, Clock Pulse Width	5	900	300		ns
		10	300	100		
		15	225	85		
$f_{CL}$	Maximum Clock Pulse Input Frequency	5		1.5		MHz
		10		4		
		15		6		
$t_r, t_f$	Maximum Clock Pulse Input Rise or Fall Time	5	Unlimited			$\mu\text{s}$
		10				
		15				

DIGITAL TIMER APPLICATION



A positive MASTER RESET pulse clears the counters and latch. The output goes high and keeps up till the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If a more accurate circuit is desired, an external clock can be used on pin 3. A set-up time equal to the width of the one shot output is required immediately following initial power up, during which time the output will be high.

FREQUENCY SELECTION TABLE

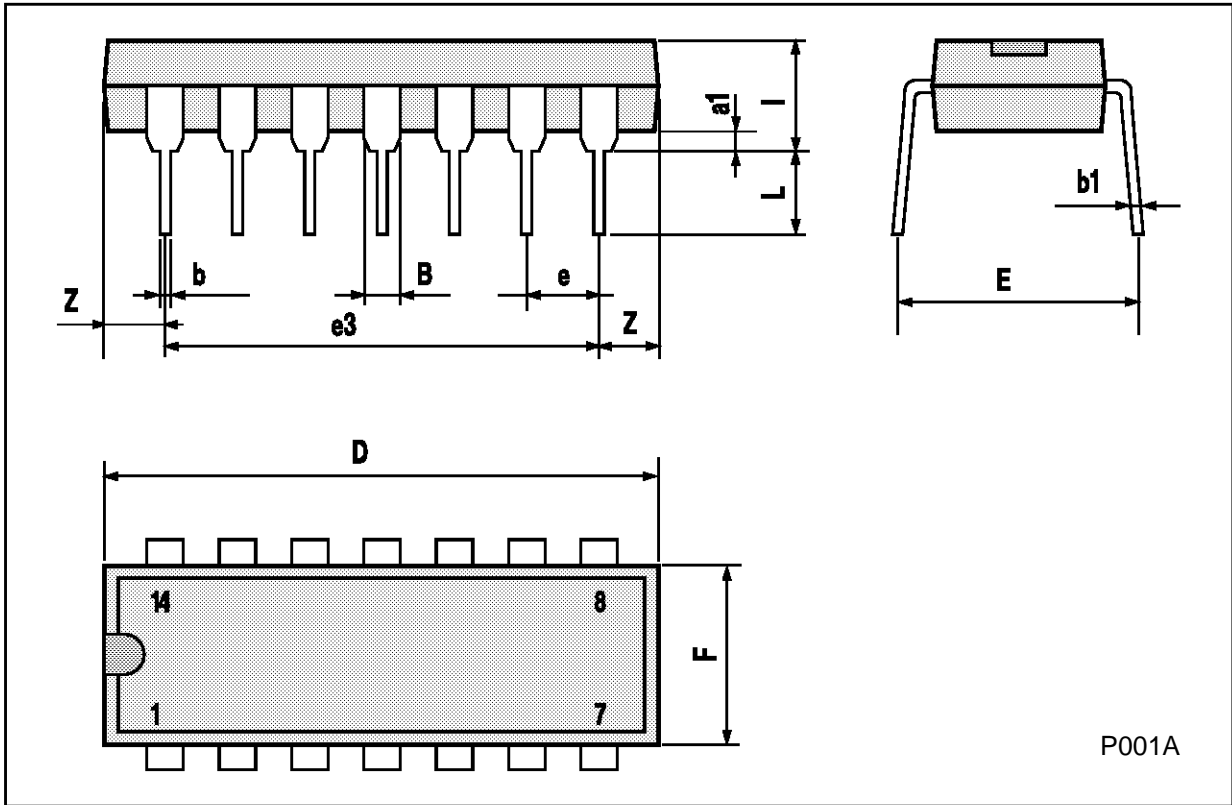
A	B	N° of Stages N	Count 2 <sup>N</sup>
0	0	13	8192
0	1	10	1024
1	0	18	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset ( $\bar{Q}$ )
10	Single Transition Mode	Recycle Mode

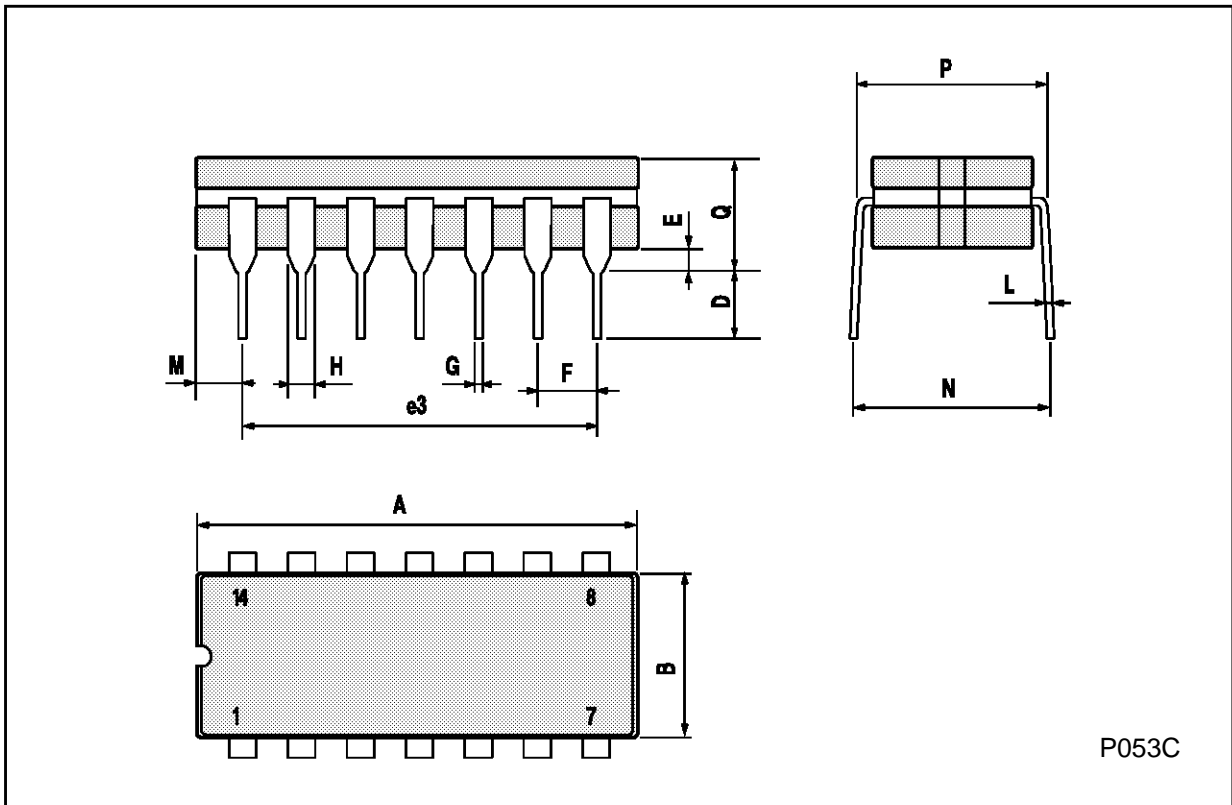
**Plastic DIP14 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



**Ceramic DIP14/1 MECHANICAL DATA**

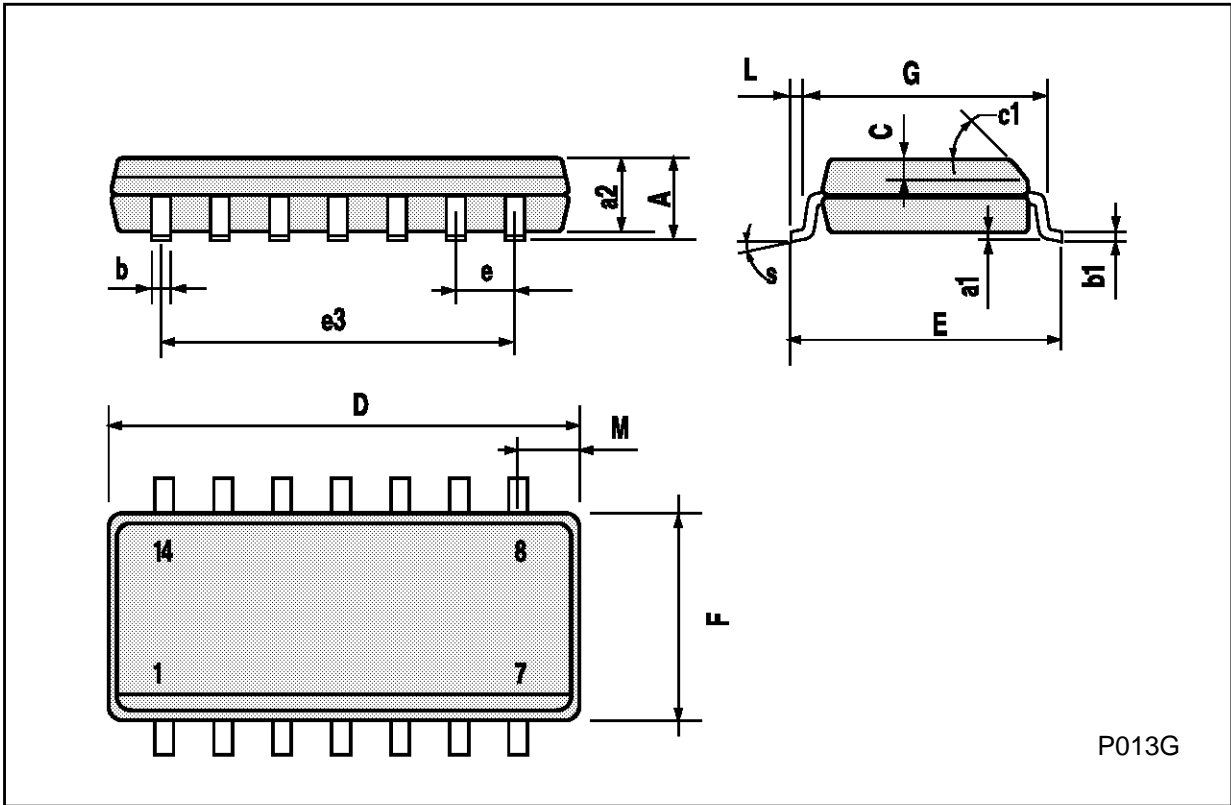
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200





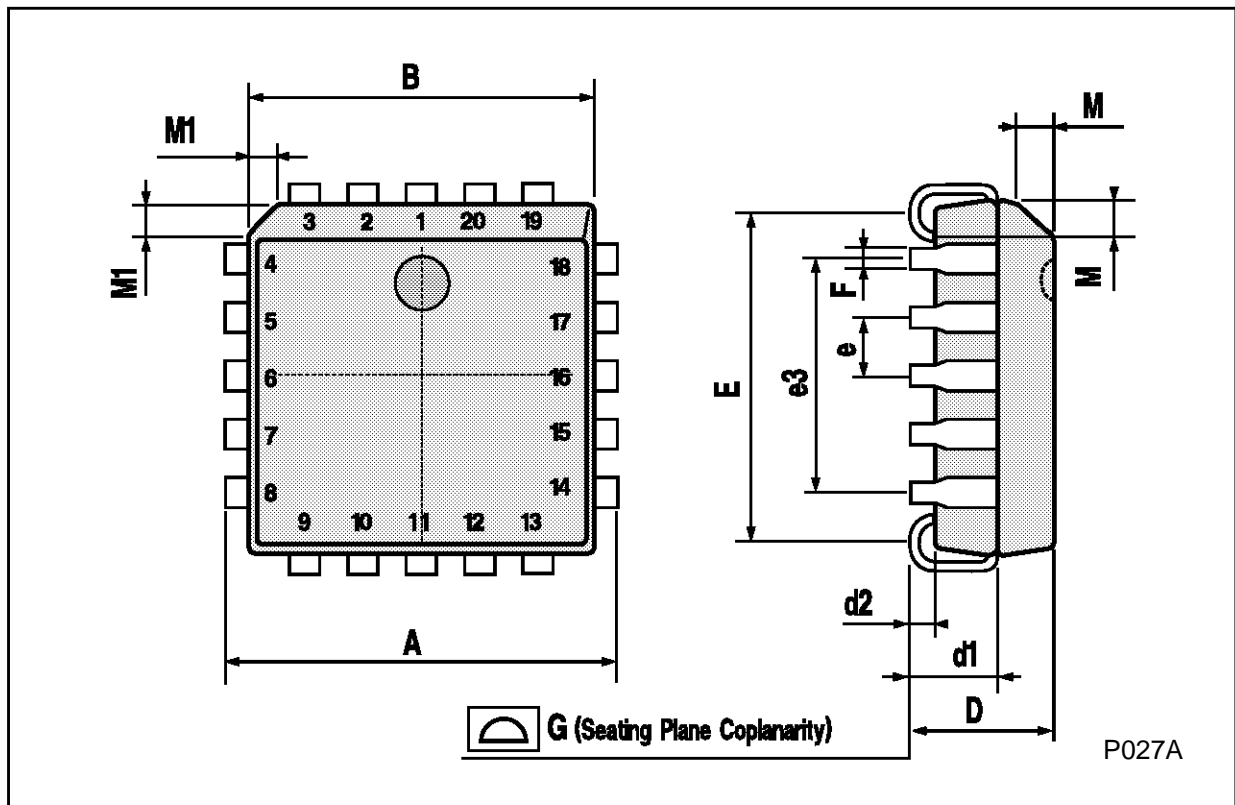
**SO14 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



**PLCC20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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